Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	112
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-UFBGA
Supplier Device Package	144-UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4r9zij6

Table 4. STM32L4R5xx modes overview (continued)

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA & Peripherals[2]	Wakeup source
Stop 0[5]	Range 1 Range 2	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DACx (x=1,2) OPAMPx (x=1,2) USARTx (x=1...5)[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2) *** All other peripherals are frozen	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...5)[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2) OTG_FS[8]
Stop 1	LPR	No	Off	ON	LSE LSI	BOR, PVD, PVM RTC, IWDG COMPx (x=1,2) DACx (x=1,2) OPAMPx (x=1,2) USARTx (x=1...5)[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2) *** All other peripherals are frozen	Reset pin, all I/Os BOR, PVD, PVM RTC, IWDG COMPx (x=1..2) USARTx (x=1...5)[6] LPUART1[6] I2Cx (x=1...4)[7] LPTIMx (x=1,2) OTG_FS[8]

3.10.6 VBAT operation

The VBAT pin allows to power the device VBAT domain from an external battery, an external supercapacitor, or from V_{DD} when there is no external battery and when an external supercapacitor is present. The VBAT pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in VBAT mode.

The VBAT operation is automatically activated when V_{DD} is not present. An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from VBAT, neither external interrupts nor RTC alarm/events exit the microcontroller from the VBAT operation.

3.11 Interconnect matrix

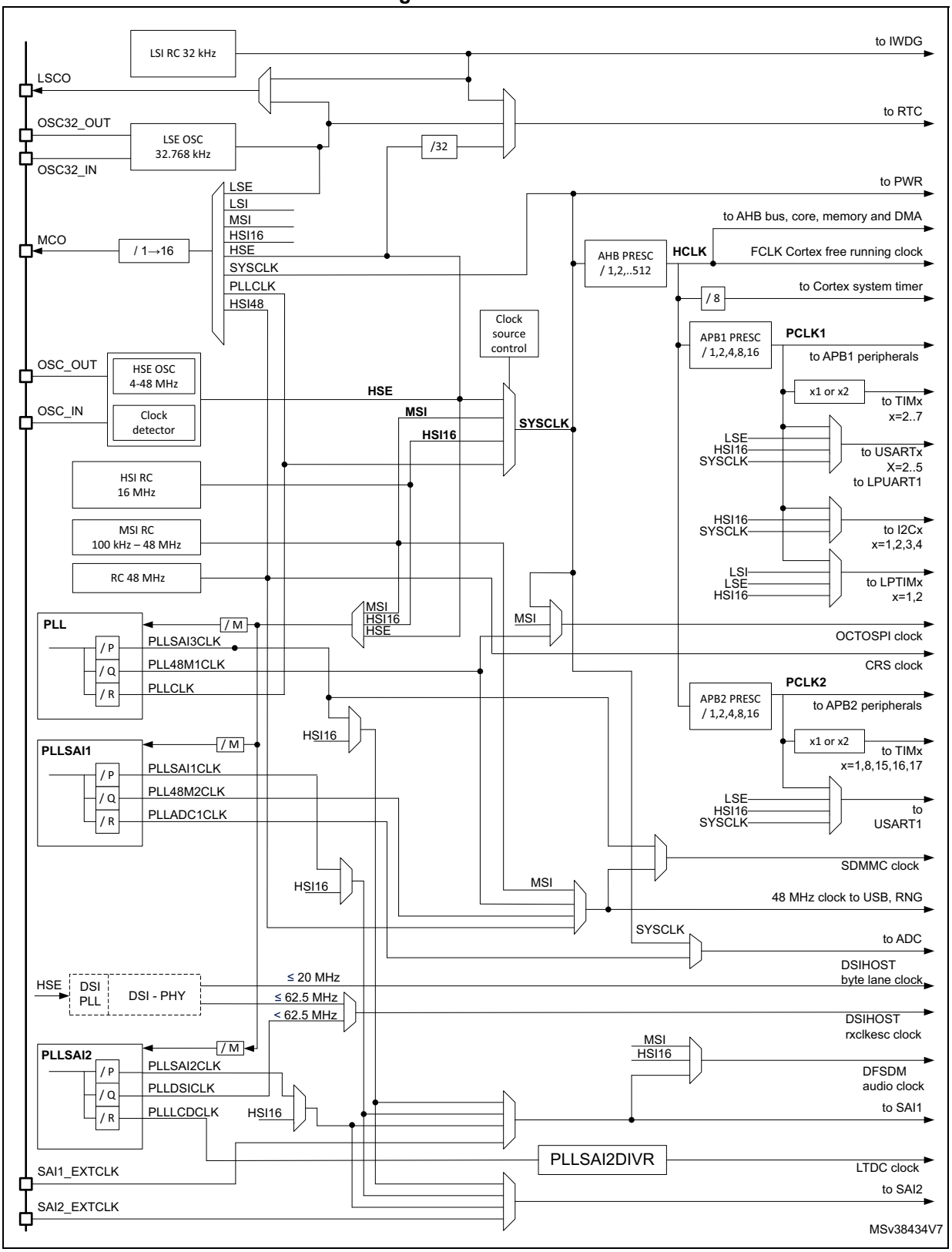
Several peripherals have direct connections between them, which allow autonomous communication between them and support the saving of CPU resources (thus power supply consumption). In addition, these hardware connections allow fast and predictable latency.

Depending on the peripherals, these interconnections can operate in Run, Sleep, Low-power run and Sleep, Stop 0, Stop 1 and Stop 2 modes. See *Table 6* for more details.

Table 6. STM32L4R5xx, STM32L4R7xx and STM32L4R9xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop 0 / Stop 1	Stop 2
TIMx	TIMx	Timers synchronization or chaining	Y	Y	Y	Y	-	-
	ADC DACx DFSDM1	Conversion triggers	Y	Y	Y	Y	-	-
	DMA	Memory to memory transfer trigger	Y	Y	Y	Y	-	-
	COMPx	Comparator output blanking	Y	Y	Y	Y	-	-
COMPx	TIM1, 8 TIM2, 3	Timer input channel, trigger, break from analog signals comparison	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by analog signals comparison	Y	Y	Y	Y	Y	Y (1)
ADCx	TIM1, 8	Timer triggered by analog watchdog	Y	Y	Y	Y	-	-
RTC	TIM16	Timer input channel from RTC events	Y	Y	Y	Y	-	-
	LPTIMERx	Low-power timer triggered by RTC alarms or tampers	Y	Y	Y	Y	Y	Y (1)
All clocks sources (internal and external)	TIM2 TIM15, 16, 17	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-	-

Figure 7. Clock tree



- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.21 Voltage reference buffer (VREFBUF)

The STM32L4Rxxx devices embed a voltage reference buffer which can be used as voltage reference for ADC, DACs and also as voltage reference for external components through the VREF+ pin.

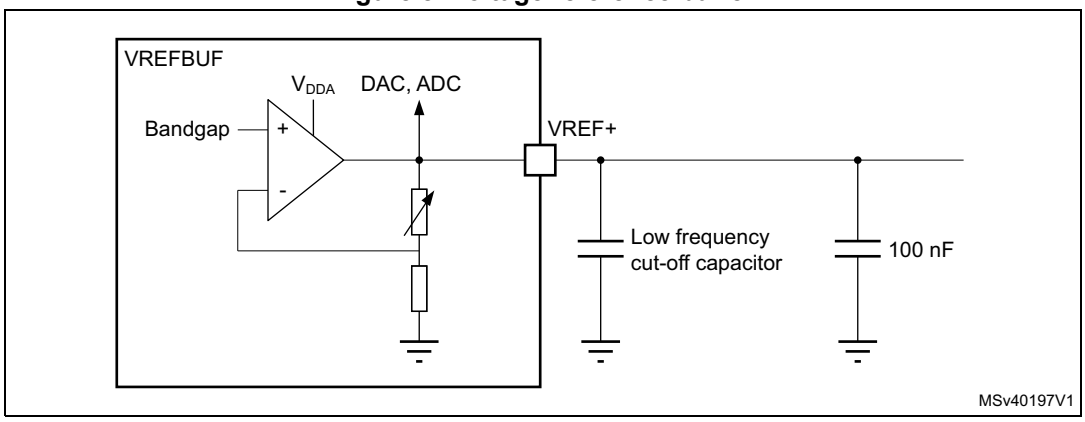
The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

Figure 8. Voltage reference buffer



3.22 Comparators (COMP)

The STM32L4Rxxx devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can also be combined into a window comparator.

- Break signal generation on analog watchdog event or on short circuit detector event
- Extremes detector:
  - Storage of minimum and maximum values of final conversion data
  - Refreshed by software
- DMA capability to read the final conversion data
- Interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence
- “Regular” or “injected” conversions:
  - “Regular” conversions can be requested at any time or even in continuous mode without having any impact on the timing of “injected” conversions
  - “Injected” conversions for precise timing and with high conversion priority

3.28 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.29 Digital camera interface (DCMI)

The STM32L4Rxxx devices embed a camera interface that can connect with any camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface in order to receive video data.

The camera interface can sustain a data transfer rate up to 54 Mbytes/s at 54 MHz. It features:

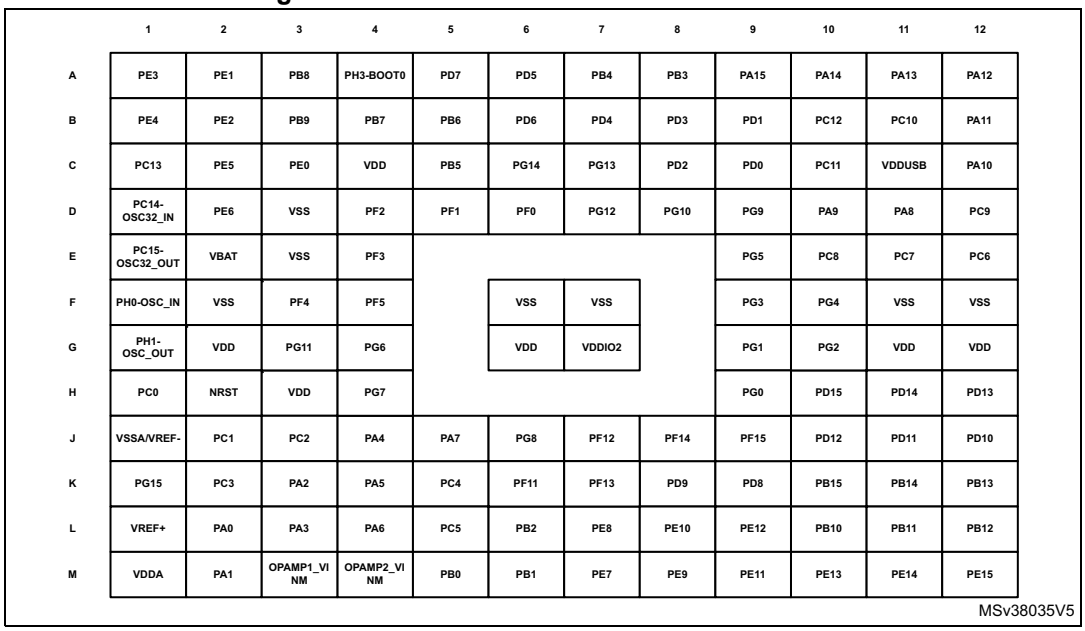
- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication of 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image.

3.30 Timers and watchdogs

The STM32L4Rxxx devices include two advanced control timers, up to nine general-purpose timers, two basic timers, two low-power timers, two watchdog timers and a SysTick timer.

The *Table 10* below compares the features of the advanced control, general-purpose and basic timers.

Figure 19. STM32L4R5xx UFBGA132 ballout(1)

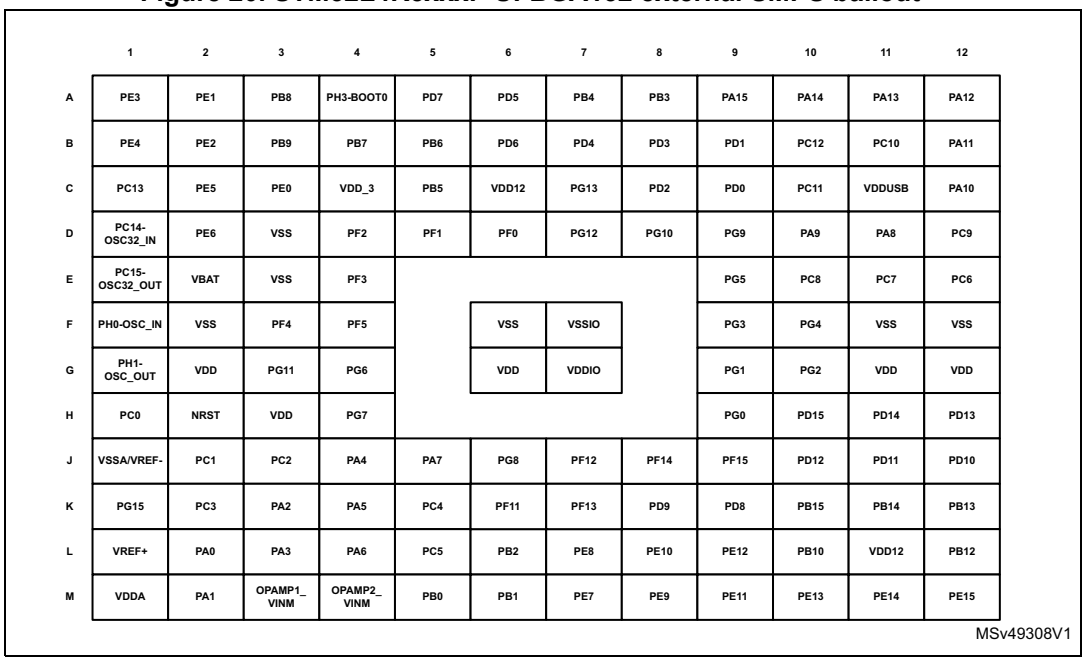


	1	2	3	4	5	6	7	8	9	10	11	12
A	PE3	PE1	PB8	PH3-BOOT0	PD7	PD5	PB4	PB3	PA15	PA14	PA13	PA12
B	PE4	PE2	PB9	PB7	PB6	PD6	PD4	PD3	PD1	PC12	PC10	PA11
C	PC13	PE5	PE0	VDD	PB5	PG14	PG13	PD2	PD0	PC11	VDDUSB	PA10
D	PC14-OSC32_IN	PE6	VSS	PF2	PF1	PF0	PG12	PG10	PG9	PA9	PA8	PC9
E	PC15-OSC32_OUT	VBAT	VSS	PF3					PG5	PC8	PC7	PC6
F	PH0-OSC_IN	VSS	PF4	PF5		VSS	VSS		PG3	PG4	VSS	VSS
G	PH1-OSC_OUT	VDD	PG11	PG6		VDD	VDDIO2		PG1	PG2	VDD	VDD
H	PC0	NRST	VDD	PG7					PG0	PD15	PD14	PD13
J	VSSA/VREF-	PC1	PC2	PA4	PA7	PG8	PF12	PF14	PF15	PD12	PD11	PD10
K	PG15	PC3	PA2	PA5	PC4	PF11	PF13	PD9	PD8	PB15	PB14	PB13
L	VREF+	PA0	PA3	PA6	PC5	PB2	PE8	PE10	PE12	PB10	PB11	PB12
M	VDDA	PA1	OPAMP1_VINM	OPAMP2_VINM	PB0	PB1	PE7	PE9	PE11	PE13	PE14	PE15

MSv38035V5

1. The above figure shows the package top view.

Figure 20. STM32L4R5xxxP UFBGA132 external SMPS ballout(1)



	1	2	3	4	5	6	7	8	9	10	11	12
A	PE3	PE1	PB8	PH3-BOOT0	PD7	PD5	PB4	PB3	PA15	PA14	PA13	PA12
B	PE4	PE2	PB9	PB7	PB6	PD6	PD4	PD3	PD1	PC12	PC10	PA11
C	PC13	PE5	PE0	VDD_3	PB5	VDD12	PG13	PD2	PD0	PC11	VDDUSB	PA10
D	PC14-OSC32_IN	PE6	VSS	PF2	PF1	PF0	PG12	PG10	PG9	PA9	PA8	PC9
E	PC15-OSC32_OUT	VBAT	VSS	PF3					PG5	PC8	PC7	PC6
F	PH0-OSC_IN	VSS	PF4	PF5		VSS	VSSIO		PG3	PG4	VSS	VSS
G	PH1-OSC_OUT	VDD	PG11	PG6		VDD	VDDIO		PG1	PG2	VDD	VDD
H	PC0	NRST	VDD	PG7					PG0	PD15	PD14	PD13
J	VSSA/VREF-	PC1	PC2	PA4	PA7	PG8	PF12	PF14	PF15	PD12	PD11	PD10
K	PG15	PC3	PA2	PA5	PC4	PF11	PF13	PD9	PD8	PB15	PB14	PB13
L	VREF+	PA0	PA3	PA6	PC5	PB2	PE8	PE10	PE12	PB10	VDD12	PB12
M	VDDA	PA1	OPAMP1_VINM	OPAMP2_VINM	PB0	PB1	PE7	PE9	PE11	PE13	PE14	PE15

MSv49308V1

1. The above figure shows the package top view.

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
36	M6	M6	47	47	H7	L5	L5	33	43	J5	H7	H7	L5	PB1	I/O	FT_a	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN0, USART3_RTS_DE, LPUART1_RTS_DE, OCTOSPIM_P1_IO0, LPTIM2_IN1, EVENTOUT	COMP1_INM, ADC1_IN16
37	L6	L6	48	48	J7	N5	N5	34	44	H5	J7	J7	N5	PB2	I/O	FT_a	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, DFSDM1_CKIN0, OCTOSPIM_P1_DQS, LCD_B1, EVENTOUT	COMP1_INP
-	K6	K6	49	49	K7	M5	M5	-	45	K6	K7	K7	M5	PF11	I/O	FT	-	LCD_DE, DCMI_D12, DSI_TE, EVENTOUT	-
-	J7	J7	50	50	L8	N6	N6	-	46	G5	L8	L8	N6	PF12	I/O	FT	-	OCTOSPIM_P2_DQS, LCD_B0, FMC_A6, EVENTOUT	-
-	-	-	51	51	M8	-	-	-	47	M1	M8	M8	-	VSS	S	-	-	-	-
-	-	-	52	52	L7	N7	N7	-	48	M6	L7	L7	N7	VDD	S	-	-	-	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
42	M9	M9	64	64	L5	N8	N8	39	60	H7	L5	L5	N8	PE11	I/O	FT	-	TIM1_CH2, DFSDM1_CKIN4, TSC_G5_IO2, OCTOSPIM_P1_NCS, LCD_G4, FMC_D8, EVENTOUT	-
43	L9	L9	65	65	M5	M8	M8	40	61	M9	M5	M5	M8	PE12	I/O	FT	-	TIM1_CH3N, SPI1_NSS, DFSDM1_DATIN5, TSC_G5_IO3, OCTOSPIM_1_IO0, LCD_G5, FMC_D9, EVENTOUT	-
44	M10	M10	66	66	J5	L8	L8	41	62	J8	J5	J5	L8	PE13	I/O	FT	-	TIM1_CH3, SPI1_SCK, DFSDM1_CKIN5, TSC_G5_IO4, OCTOSPIM_P1_IO1, LCD_G6, FMC_D10, EVENTOUT	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
86	A6	A6	119	119	A5	D7	D7	88	121	D7	A5	A5	D7	PD5	I/O	FT	-	USART2_TX, OCTOSPIM_P1_IO5, FMC_NWE, EVENTOUT	-
-	-	-	120	120	B6	M3	M3	-	122	-	B6	B6	M3	VSS	S	-	-	-	-
-	-	-	121	121	A6	A8	A8	-	123	-	A6	A6	A8	VDD	S	-	-	-	-
87	B6	B6	122	122	E7	E7	E7	89	124	B7	E7	E7	E7	PD6	I/O	FT	-	SAI1_D1, DCMI_D10, SPI3_MOSI, DFSDM1_DATIN1, USART2_RX, OCTOSPIM_P1_IO6, LCD_DE, FMC_NWAIT, SAI1_SD_A, EVENTOUT	-
88	A5	A5	123	123	D7	F7	F7	90	125	E7	D7	D7	F7	PD7	I/O	FT	-	DFSDM1_CKIN1, USART2_CK, OCTOSPIM_P1_IO7, FMC_NCE/FMC_NE1, EVENTOUT	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
-	-	-	-	-	-	A2	A2	-	-	-	-	-	A2	PH2	I/O	FT	-	OCTOSPIM_P1_IO4, EVENTOUT	-
-	-	-	-	-	-	B2	B2	-	-	-	-	-	B2	PI7	I/O	FT	-	TIM8_CH3, DCMI_D7, EVENTOUT	-
-	-	-	-	-	-	B1	B1	-	-	-	-	-	B1	PI9	I/O	FT	-	OCTOSPIM_P2_IO2, CAN1_RX, EVENTOUT	-
-	-	-	-	-	-	A1	A1	-	-	-	-	-	A1	PI10	I/O	FT	-	OCTOSPIM_P2_IO1, EVENTOUT	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (for example to drive a LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0432 reference manual.
3. NC (not-connected) balls must be left unconnected. However, non connected (NC) GPIOS are not bonded. They must be configured by software to output push-pull and forced to 0 in the output data register to avoid extra current consumption in low-power modes.
4. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.

Table 16. Alternate function AF0 to AF7[1] (continued)

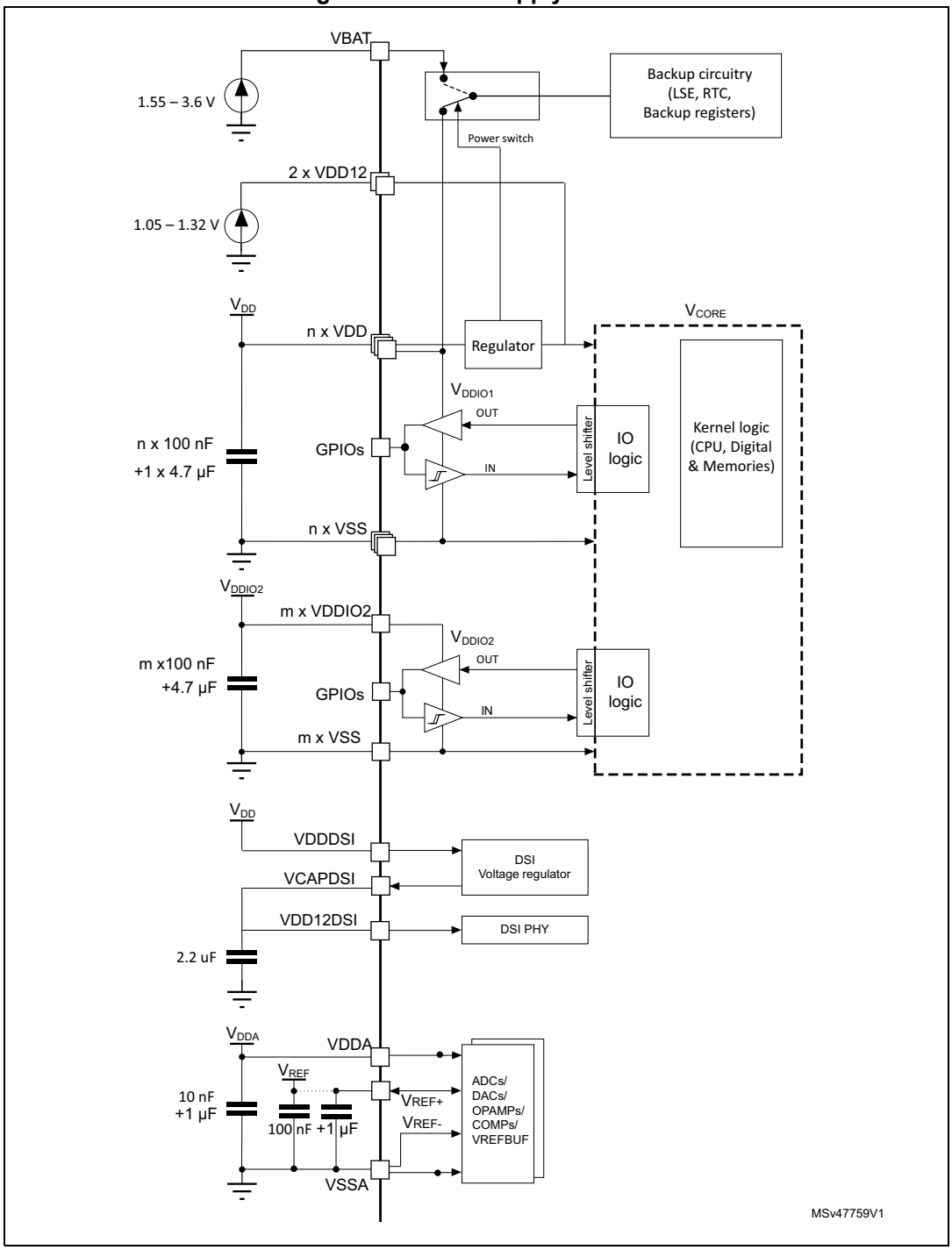
Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port D	PD0	-	-	-	-	-	SPI2_NSS	DFSDM1_DATIN7	-
	PD1	-	-	-	-	-	SPI2_SCK	DFSDM1_CKIN7	-
	PD2	TRACED2	-	TIM3_ETR	-	-	-	-	USART3_RTS_DE
	PD3	-	-	-	SPI2_SCK	DCMI_D5	SPI2_MISO	DFSDM1_DATIN0	USART2_CTS_NSS
	PD4	-	-	-	-	-	SPI2_MOSI	DFSDM1_CKIN0	USART2_RTS_DE
	PD5	-	-	-	-	-	-	-	USART2_TX
	PD6	-	-	-	SAI1_D1	DCMI_D10	SPI3_MOSI	DFSDM1_DATIN1	USART2_RX
	PD7	-	-	-	-	-	-	DFSDM1_CKIN1	USART2_CK
	PD8	-	-	-	-	-	-	-	USART3_TX
	PD9	-	-	-	-	-	-	-	USART3_RX
	PD10	-	-	-	-	-	-	-	USART3_CK
	PD11	-	-	-	-	I2C4_SMBA	-	-	USART3_CTS_NSS
	PD12	-	-	TIM4_CH1	-	I2C4_SCL	-	-	USART3_RTS_DE
	PD13	-	-	TIM4_CH2	-	I2C4_SDA	-	-	-
	PD14	-	-	TIM4_CH3	-	-	-	-	-
	PD15	-	-	TIM4_CH4	-	-	-	-	-

Table 16. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		OTG_FS/SYS_AF	TIM1/2/5/8/LPTIM1	TIM1/2/3/4/5	SPI2/SAI1/I2C4/USART2/OTG_FS/TIM1/8/OCTOSPIM_P1	I2C1/2/3/4/DCMI	SPI1/2/3/I2C4/DFSDM1/DCMI/OCTOSPIM_P1/2	SPI3/I2C3/DFSDM1/COMP1/OCTOSPIM_P2	USART1/2/3
Port G	PG0	-	-	-	-	-	OCTOSPIM_P2_IO4	-	-
	PG1	-	-	-	-	-	OCTOSPIM_P2_IO5	-	-
	PG2	-	-	-	-	-	SPI1_SCK	-	-
	PG3	-	-	-	-	-	SPI1_MISO	-	-
	PG4	-	-	-	-	-	SPI1_MOSI	-	-
	PG5	-	-	-	-	-	SPI1_NSS	-	-
	PG6	-	-	-	OCTOSPIM_P1_DQS	I2C3_SMBA	-	-	-
	PG7	-	-	-	SAI1_CK1	I2C3_SCL	OCTOSPIM_P2_DQS	DFSDM1_CKOUT	-
	PG8	-	-	-	-	I2C3_SDA	-	-	-
	PG9	-	-	-	-	-	OCTOSPIM_P2_IO6	SPI3_SCK	USART1_TX
	PG10	-	LPTIM1_IN1	-	-	-	OCTOSPIM_P2_IO7	SPI3_MISO	USART1_RX
	PG11	-	LPTIM1_IN2	-	OCTOSPIM_P1_IO5	-	-	SPI3_MOSI	USART1_CTS_NSS
	PG12	-	LPTIM1_ETR	-	-	-	OCTOSPIM_P2_NCS	SPI3_NSS	USART1_RTS_DE
	PG13	-	-	-	-	I2C1_SDA	-	-	USART1_CK
	PG14	-	-	-	-	I2C1_SCL	-	-	-
	PG15	-	LPTIM1_OUT	-	-	I2C1_SMBA	OCTOSPIM_P2_DQS	-	-

6.1.6 Power supply scheme

Figure 26. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Table 43. Current consumption in Sleep and Low-power sleep modes, Flash ON and power supplied by external SMPS

Symbol	Parameter	Conditions(1)			TYP					Unit
		-	VDD12	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Sleep)	Supply current in Sleep mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12=1.20V	120 MHz	1.68	1.89	2.51	3.37	4.81	mA
			VDD12=1.10V	80 MHz	1.01	1.17	1.67	2.37	3.59	
				72 MHz	0.92	1.08	1.58	2.30	3.54	
				64 MHz	0.83	0.99	1.51	2.21	3.45	
				48 MHz	0.77	0.93	1.44	2.16	3.40	
				32 MHz	0.56	0.72	1.22	1.92	3.16	
				26 MHz	0.47	0.63	1.10	1.79	3.02	
				16 MHz	0.33	0.50	0.97	1.64	2.87	
				8 MHz	0.22	0.38	0.84	1.53	2.74	
				4 MHz	0.16	0.32	0.80	1.47	2.70	
				2 MHz	0.14	0.27	0.75	1.45	2.65	
				1 MHz	0.12	0.26	0.75	1.42	2.63	
				100 KHz	0.11	0.25	0.73	1.40	2.63	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%.

Table 51. Current consumption in VBAT mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{BAT}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD(VBAT)	Backup domain supply current	RTC disabled	1.8 V	3.00	27.0	165	495	1350	8.0	67.0	390	1200	3000	nA
			2.4 V	4.00	31.0	190	560	1550	10.0	76.0	440	1300	3300	
			3 V	6.00	43.0	255	750	2000	13.0	91.0	510	1500	3800	
			3.6 V	14.0	83.0	485	1450	4050	34.0	200	1100	3100	8300	
		RTC enabled and clocked by LSE bypassed at 32768 Hz	1.8 V	215	240	390	730	-	-	-	-	-	-	
			2.4 V	305	340	510	900	-	-	-	-	-	-	
			3 V	415	455	680	1200	-	-	-	-	-	-	
			3.6 V	540	595	925	1900	-	-	-	-	-	-	
		RTC enabled and clocked by LSE quartz(2)	1.8 V	305	345	510	865	1600	-	-	-	-	-	
			2.4 V	395	440	625	1050	1800	-	-	-	-	-	
			3 V	510	565	805	1350	2300	-	-	-	-	-	
			3.6 V	650	740	1200	2200	4450	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.17*. However, the recommended clock input waveform is shown in *Figure 29: High-speed external clock source AC timing diagram*.

Table 56. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	Voltage scaling Range 1	-	8	48	MHz
		Voltage scaling Range 2	-	8	26	
V_{HSEH}	OSC_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	Voltage scaling Range 1	7	-	-	ns
		Voltage scaling Range 2	18	-	-	

1. Guaranteed by design.

Figure 29. High-speed external clock source AC timing diagram

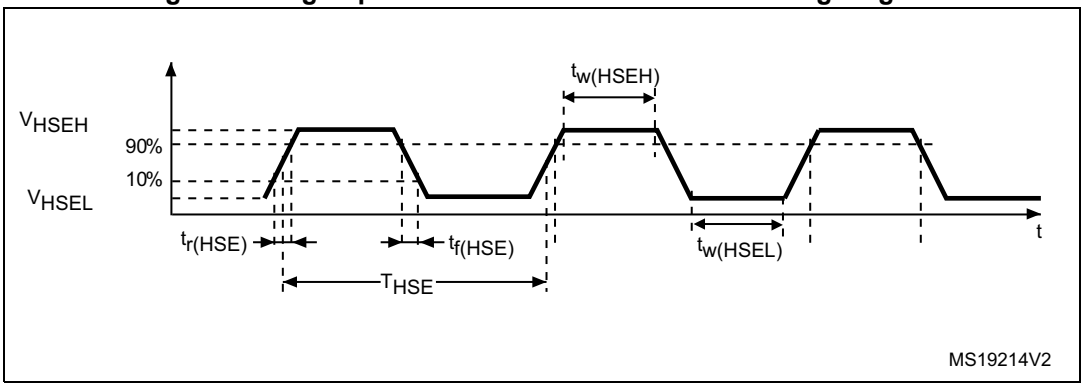


Table 76. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH} (1)	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	0.7xV_{DDIOx} (2)	-	-	V
	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	0.49xV_{DDIOX}+0.26 (3)	-	-	
	I/O input high level voltage except BOOT0	1.08 V<V_{DDIOx}<1.62 V	0.61xV_{DDIOX}+0.05 (3)	-	-	
	BOOT0 I/O input high level voltage	1.62 V<V_{DDIOx}<3.6 V	0.77xV_{DDIOX} (3)	-	-	
V_{hys} (3)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	200	-	mV
	FT_sx	1.08 V<V_{DDIOx}<1.62 V	-	150	-	
	BOOT0 I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	200	-	
I_{lkg}	FT_xx input leakage current(3)	V_{IN} ≤ Max(V_{DDXXX})(4)	-	-	±100	nA
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX})+1 V(4)(5)	-	-	650(3)(6)	
		Max(V_{DDXXX})+1 V < VIN ≤ 5.5 V(3)(5)	-	-	200(6)	
	FT_lu, FT_u, PB2 and PC3 IO	V_{IN} ≤ Max(V_{DDXXX}) (4)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX})+1 V(4)	-	-	2500(3)(7)	
		Max(V_{DDXXX})+1 V < VIN ≤ 5.5 V(4)(5)(7)	-	-	250(7)	
	TT_xx input leakage current	V_{IN} ≤ Max(V_{DDXXX})(6)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} < 3.6 V(6)	-	-	2000(3)	
	OPAMPx_VINM (x=1,2) dedicated input leakage current	-	-	-	(8)	
R_{PU}	Weak pull-up equivalent resistor (9)	V_{IN} = V_{SS}	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(9)	V_{IN} = V_{DDIOx}	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 39* and *Table 78*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 78. I/O AC characteristics(1)(2)

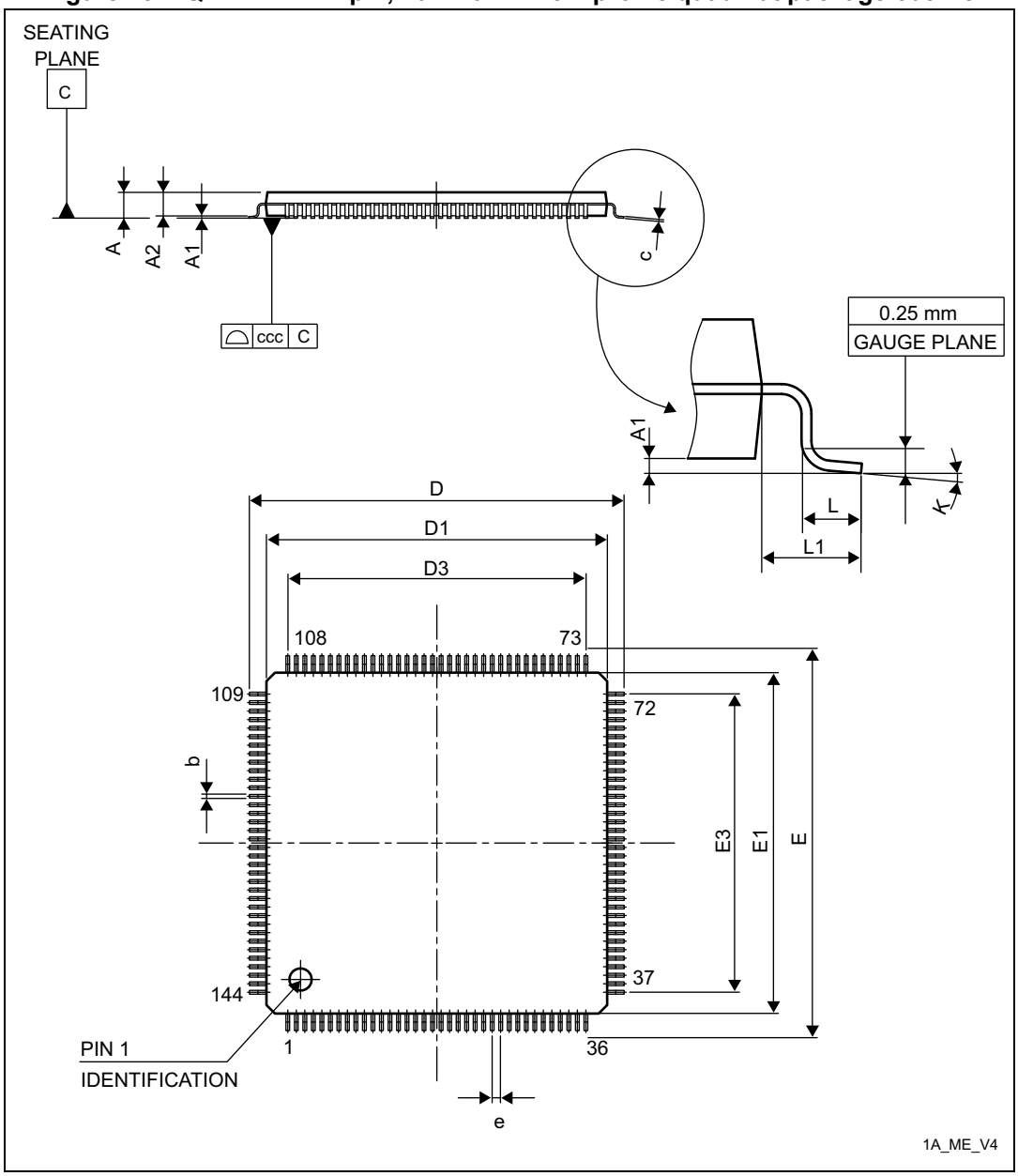
Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	0.1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1.5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	0.1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	52	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	140	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	17	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	110	
01	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	10	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	15	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	9	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	16	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	40	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	4.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	9	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	21	

Table 92. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
GM	Gain margin	Normal mode		-	13	-	dB
		Low-power mode		-	20	-	
t_{WAKEUP}	Wake up time from OFF state.	Normal mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 4 kΩ follower configuration	-	5	10	µs
		Low-power mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 20 kΩ follower configuration	-	10	30	
I_{bias}	OPAMP input bias current	General purpose input (all packages except UFBGA132 and UFBGA169 only)		-	-	(3)	nA
		Dedicated input (UFBGA132 and UFBGA169 only)	T_J ≤ 75 °C	-	-	1	
			T_J ≤ 85 °C	-	-	3	
			T_J ≤ 105 °C	-	-	8	
			T_J ≤ 125 °C	-	-	15	
PGA gain(2)	Non inverting gain value	-		-	2	-	-
				-	4	-	
				-	8	-	
				-	16	-	
$R_{network}$	R2/R1 internal resistance values in PGA mode(4)	PGA Gain = 2		-	80/80	-	kΩ/kΩ
		PGA Gain = 4		-	120/ 40	-	
		PGA Gain = 8		-	140/ 20	-	
		PGA Gain = 16		-	150/ 10	-	
Delta R	Resistance variation (R1 or R2)	-		-15	-	15	%
PGA gain error	PGA gain error	-		-1	-	1	%
PGA BW	PGA bandwidth for different non inverting gain	Gain = 2	-	-	GBW/ 2	-	MHz
		Gain = 4	-	-	GBW/ 4	-	
		Gain = 8	-	-	GBW/ 8	-	
		Gain = 16	-	-	GBW/ 16	-	

7.3 LQFP144 package information

Figure 78. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



1. Drawing is not to scale.