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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	112
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-UFBGA, WLCSP
Supplier Device Package	144-WLCSP (5.24x5.24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4r9ziy6ptr

Table 10. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced control	TIM1, TIM8	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TIM2, TIM5	32-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM3, TIM4	16-bit	Up, down, Up/down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.30.1 Advanced-control timer (TIM1, TIM8)

The advanced-control timers can each be seen as a three-phase PWM multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers.

The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled in order to turn off any power switches driven by these outputs.

Many features are shared with the general-purpose TIMx timers (described in *Section 3.30.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
3	B1	B1	3	3	C12	D1	D1	3	3	D3	C12	C12	D1	PE4	I/O	FT	-	TRACED1, TIM3_CH2, SAI1_D2, DFSDM1_DATIN3, TSC_G7_IO3, DCMI_D4, LCD_B0, FMC_A20, SAI1_FS_A, EVENTOUT	-
4	C2	C2	4	4	D9	E4	E4	4	4	C2	D9	D9	E4	PE5	I/O	FT	-	TRACED2, TIM3_CH3, SAI1_CK2, DFSDM1_CKIN3, TSC_G7_IO4, DCMI_D6, LCD_G0, FMC_A21, SAI1_SCK_A, EVENTOUT	-
5	D2	D2	5	5	D10	E3	E3	5	5	D4	D10	D10	E3	PE6	I/O	FT	-	TRACED3, TIM3_CH4, SAI1_D1, DCMI_D7, LCD_G1, FMC_A22, SAI1_SD_A, EVENTOUT	RTC_TAMP3,WKUP3
6	E2	E2	6	6	E10	E2	E2	6	6	B1	E10	E10	E2	VBAT	S	-	-	-	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
82	B9	B9	115	115	C5	C8	C8	84	117	B8	C5	C5	C8	PD1	I/O	FT	-	SPI2_SCK, DFSDM1_CKIN7, CAN1_TX, LCD_B5, FMC_D3, EVENTOUT	-
83	C8	C8	116	116	B5	D8	D8	85	118	D8	B5	B5	D8	PD2	I/O	FT	-	TRACED2, TIM3_ETR, USART3_RTS_DE, UART5_RX, TSC_SYNC, DCMI_D11, SDMMC1_CMD, EVENTOUT	-
84	B8	B8	117	117	D6	E8	E8	86	119	A8	D6	D6	E8	PD3	I/O	FT	-	SPI2_SCK, DCMI_D5, SPI2_MISO, DFSDM1_DATIN0, USART2_CTS_NSS, OCTOSPIM_P2_NCS, LCD_CLK, FMC_CLK, EVENTOUT	-
85	B7	B7	118	118	C6	C7	C7	87	120	C7	C6	C6	C7	PD4	I/O	FT	-	SPI2_MOSI, DFSDM1_CKIN0, USART2_RTS_DE, OCTOSPIM_P1_IO4, FMC_NOE, EVENTOUT	-

3. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
4. Positive injection (when $V_{IN} > V_{DDIOx}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 19: Voltage characteristics* for the minimum allowed input voltage values.
6. When several inputs are submitted to a current injection, the maximum $\sum|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 22. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	120	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	120	
f_{PCLK2}	Internal APB2 clock frequency	-	0	120	
V_{DD}	Standard operating voltage	-	1.71 (1)	3.6	V
V_{DD12}	Standard operating voltage	Up to 120 MHz	1.14	1.32	
		Up to 80 MHz	1.08	1.32	
		Up to 26 MHz	1.05 (2)	1.32	
V_{DDIO2}	PG[15:2] I/Os supply voltage	At least one I/O in PG[15:2] used	1.08	3.6	
		PG[15:2] not used	0	3.6	
V_{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6	
		DAC or OPAMP used	1.8		
		VREFBUF used	2.4		
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0		
V_{BAT}	Backup operating voltage	-	1.55	3.6	

Table 39. Typical current consumption in Run and Low-power run modes with different codes running from Flash, ART disable and power supplied by external SMPS

Symbol	Parameter	Conditions[1]				TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	VDD12	f_{HCLK}	Code	25°C	25°C		25°C	25°C	
I_{DD} (Run)	Supply current in Run mode	f_{HCLK}=f_{HSE} up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12= 1.05V	f_{HCLK}= 26 MHz	Reduced code	1.57	1.61	mA	60	62	µA/MHz
					Coremark	1.63	1.49		63	57	
					Dhrystone2.1	1.73	1.57		67	60	
					Fibonacci	1.49	1.41		57	54	
					While(1)	1.24	1.24		48	48	
			VDD12= 1.10V	f_{HCLK}= 26 MHz	Reduced code	1.73	1.77	mA	66	68	µA/MHz
					Coremark	1.79	1.64		69	63	
					Dhrystone2.1	1.90	1.73		73	66	
					Fibonacci	1.64	1.55		63	60	
					While(1)	1.36	1.36		52	52	
				f_{HCLK}= 80 MHz	Reduced code	4.67	4.67	mA	58	58	µA/MHz
					Coremark	4.67	4.31		58	54	
					Dhrystone2.1	5.03	4.49		63	56	
					Fibonacci	4.13	3.95		52	49	
					While(1)	3.77	3.77		47	47	
I_{DD} (Run)	Supply current in Run mode	f_{HCLK}=f_{HSE} up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12= 1.20V	f_{HCLK}= 120 MHz	Reduced code	7.4	6.8	mA	62	57	µA/MHz
					Coremark	7.2	6.4		60	53	
					Dhrystone 2.1	7.6	6.6		64	55	
					Fibonacci	6.4	6.0		53	50	
					While(1)	6.6	6.6		55	55	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, VDD12 = 1.10 V.

Table 42. Current consumption in Sleep and Low-power sleep mode, Flash ON

Symbol	Parameter	Conditions		f_{HCLK}	TYP					MAX(1)					Unit
		-	Voltage scaling		25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
I_{DD} (Sleep)	Supply current in Sleep mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	1.10	1.45	2.55	4.15	7.00	1.40	2.2	4.2	7.5	14.0	mA
				16 MHz	0.78	1.15	2.25	3.80	6.65	1.00	1.8	3.8	7.1	14.0	
				8 MHz	0.52	0.87	1.95	3.55	6.35	0.72	1.5	3.5	6.8	13.0	
				4 MHz	0.38	0.74	1.85	3.40	6.25	0.57	1.4	3.4	6.7	13.0	
				2 MHz	0.32	0.63	1.75	3.35	6.15	0.50	1.3	3.3	6.6	13.0	
				1 MHz	0.29	0.61	1.75	3.30	6.10	0.46	1.3	3.3	6.5	13.0	
				100 KHz	0.26	0.58	1.70	3.25	6.10	0.43	1.2	3.2	6.5	13.0	
			Range 1 Boost Mode	120 MHz	4.20	4.70	6.25	8.40	12.00	4.80	6.0	8.7	13.0	21.0	
			Range 1 Normal Mode	80 MHz	2.80	3.25	4.65	6.60	10.00	3.30	4.3	6.8	11.0	18.0	
				72 MHz	2.55	3.00	4.40	6.40	9.85	3.00	4.0	6.5	11.0	18.0	
				64 MHz	2.30	2.75	4.20	6.15	9.60	2.70	3.8	6.3	11.0	18.0	
				48 MHz	2.15	2.60	4.00	6.00	9.45	2.60	3.5	6.0	10.0	18.0	
				32 MHz	1.55	2.00	3.40	5.35	8.80	1.90	2.9	5.4	9.3	17.0	
				24 MHz	1.25	1.70	3.10	5.05	8.50	1.60	2.5	5.0	9.0	16.0	
				16 MHz	0.93	1.40	2.80	4.70	8.20	1.20	2.2	4.7	8.6	16.0	
I_{DD} (LPSleep)	Supply current in Low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	235	625	1950	3750	6900	410	1400	3800	7500	14000	µA
				1 MHz	220	605	1900	3700	6850	390	1400	3700	7500	14000	
				400 KHz	215	595	1900	3700	6850	390	1300	3700	7500	14000	
				100 KHz	210	595	1900	3700	6800	380	1300	3700	7500	14000	

1. Guaranteed by characterization results, unless otherwise specified.

Table 51. Current consumption in VBAT mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{BAT}	25°C	55°C	85°C	105°C	125°C	25°C	55°C	85°C	105°C	125°C	
IDD(VBAT)	Backup domain supply current	RTC disabled	1.8 V	3.00	27.0	165	495	1350	8.0	67.0	390	1200	3000	nA
			2.4 V	4.00	31.0	190	560	1550	10.0	76.0	440	1300	3300	
			3 V	6.00	43.0	255	750	2000	13.0	91.0	510	1500	3800	
			3.6 V	14.0	83.0	485	1450	4050	34.0	200	1100	3100	8300	
		RTC enabled and clocked by LSE bypassed at 32768 Hz	1.8 V	215	240	390	730	-	-	-	-	-	-	
			2.4 V	305	340	510	900	-	-	-	-	-	-	
			3 V	415	455	680	1200	-	-	-	-	-	-	
			3.6 V	540	595	925	1900	-	-	-	-	-	-	
		RTC enabled and clocked by LSE quartz(2)	1.8 V	305	345	510	865	1600	-	-	-	-	-	
			2.4 V	395	440	625	1050	1800	-	-	-	-	-	
			3 V	510	565	805	1350	2300	-	-	-	-	-	
			3.6 V	650	740	1200	2200	4450	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

Table 52. Peripheral current consumption (continued)

Peripheral		Range 1 Boost Mode	Range 1 Normal Mode	Range 2	Low-power run and sleep	Unit
APB1 (Cont.)	I2C1 APB clock domain	1.4	1.4	1.25	2	µA/MHz
	I2C2 independent clock domain	3.5	3.4	2.5	3.5	
	I2C2 APB clock domain	1.4	1.25	1.25	1	
	I2C3 independent clock domain	3.25	3.15	2.9	3	
	I2C3 APB clock domain	1.15	1	0.835	1	
	I2C4 independent clock domain	3.5	3.25	2.75	3	
	I2C4 APB clock domain	1.35	1.25	1	1.5	
	LPUART1 independent clock domain	3.15	3	2.45	3	
	LPUART1 APB clock domain	1.65	1.5	1.3	1.5	
	LPTIM1 independent clock domain	3.6	3.5	2.9	3	
	LPTIM1 APB clock domain	1	0.875	0.835	1	
	LPTIM2 independent clock domain	3.4	3.25	2.55	3.5	
	LPTIM2 APB clock domain	1.1	1	0.79	1	
	OPAMP	0.415	0.375	0.415	0.5	
	PWR	0.5	0.375	0.415	0.5	
	RTCAPB	1.25	1.15	1.25	1	
	SPI2	2.6	2.4	2.1	2.5	
	SPI3	3	2.75	2.5	3	
	TIM2	6.15	5.75	4.65	4.5	
	TIM3	5.25	4.9	4.15	5	
	TIM4	5.15	4.75	4.15	5	
	TIM5	6.5	6	5	6	
	TIM6	1.35	1.15	1.25	1	
	TIM7	1.25	1.15	0.835	1	

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 74. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A(1)

1. Negative injection is limited to -30 mA for PF0, PF1, PG6, PG7, PG8, PG12, PG13, PG14.

6.3.16 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

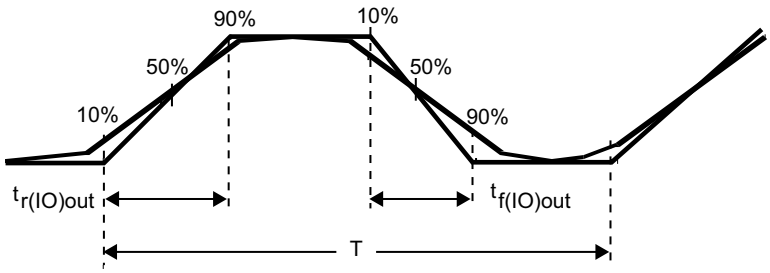
The characterization results are given in *Table 75*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 76. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH} (1)	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	0.7xV_{DDIOx} (2)	-	-	V
	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	0.49xV_{DDIOX}+0.26 (3)	-	-	
	I/O input high level voltage except BOOT0	1.08 V<V_{DDIOx}<1.62 V	0.61xV_{DDIOX}+0.05 (3)	-	-	
	BOOT0 I/O input high level voltage	1.62 V<V_{DDIOx}<3.6 V	0.77xV_{DDIOX} (3)	-	-	
V_{hys} (3)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	200	-	mV
	FT_sx	1.08 V<V_{DDIOx}<1.62 V	-	150	-	
	BOOT0 I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	200	-	
I_{lkg}	FT_xx input leakage current(3)	V_{IN} ≤ Max(V_{DDXXX})(4)	-	-	±100	nA
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX})+1 V(4)(5)	-	-	650(3)(6)	
		Max(V_{DDXXX})+1 V < VIN ≤ 5.5 V(3)(5)	-	-	200(6)	
	FT_lu, FT_u, PB2 and PC3 IO	V_{IN} ≤ Max(V_{DDXXX}) (4)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX})+1 V(4)	-	-	2500(3)(7)	
		Max(V_{DDXXX})+1 V < VIN ≤ 5.5 V(4)(5)(7)	-	-	250(7)	
	TT_xx input leakage current	V_{IN} ≤ Max(V_{DDXXX})(6)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} < 3.6 V(6)	-	-	2000(3)	
	OPAMPx_VINM (x=1,2) dedicated input leakage current	-	-	-	(8)	
R_{PU}	Weak pull-up equivalent resistor (9)	V_{IN} = V_{SS}	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(9)	V_{IN} = V_{DDIOx}	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

Figure 39. I/O AC characteristics definition(1)



Maximum frequency is achieved if (t_r + t_f (≤ 2/3)T and if the duty cycle is (45-55%) when loaded by the specified capacitance.

MS32132V2

1. Refer to *Table 78: I/O AC characteristics*.

6.3.18 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 79. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3_x V_{DDIOx}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7_x V_{DDIOx}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	350	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Table 87. ADC accuracy - limited test conditions 4(1)(2)(3)

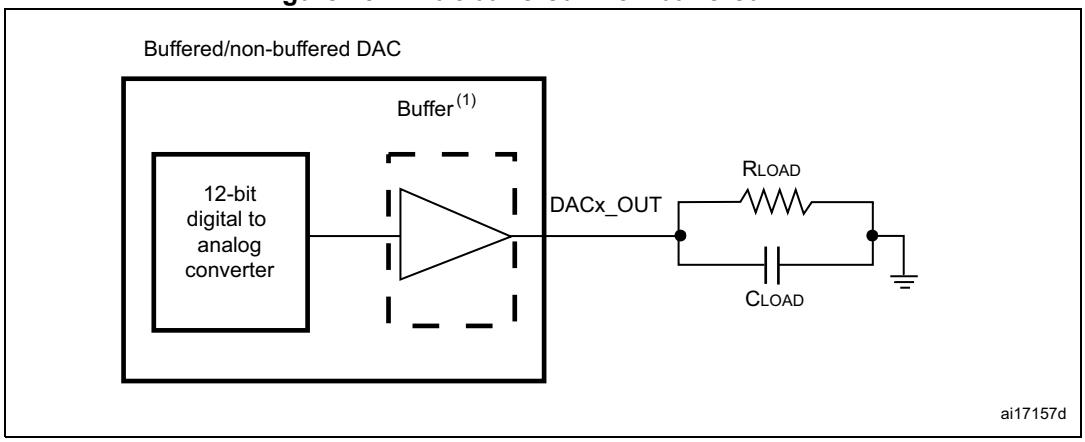
Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 26 MHz, 1.65 V ≤ V_{DDA} = VREF+ ≤ 3.6 V, Voltage scaling Range 2	Single ended	Fast channel (max speed)	-	5	5.4	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	4	5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	4	
				Slow channel (max speed)	-	2	4	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2	3.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	4	4.5	
				Slow channel (max speed)	-	4	4.5	
			Differential	Fast channel (max speed)	-	3	4	
				Slow channel (max speed)	-	3	4	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	2.5	3	
				Slow channel (max speed)	-	2.5	3	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.2	10.5	-	bits
				Slow channel (max speed)	10.2	10.5	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	63	65	-	dB
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	64	65	-	
				Slow channel (max speed)	64	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

Table 88. DAC characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDV}(DAC)	DAC consumption from V_{REF+}	DAC output buffer ON	No load, middle code (0x800)	-	185	240	µA
			No load, worst code (0xF1C)	-	340	400	
		DAC output buffer OFF	No load, middle code (0x800)	-	155	205	
		Sample and hold mode, buffer ON, C_{SH} = 100 nF, worst case		-	185 x Ton/(Ton +Toff) (4)	400 x Ton/(Ton +Toff) (4)	
		Sample and hold mode, buffer OFF, C_{SH} = 100 nF, worst case		-	155 x Ton/(Ton +Toff) (4)	205 x Ton/(Ton +Toff) (4)	

1. Guaranteed by design.
2. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).
3. Refer to *Table 76: I/O static characteristics*.
4. Ton is the Refresh phase duration. Toff is the Hold phase duration. Refer to RM0351 reference manual for more details.

Figure 43. 12-bit buffered / non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.30 Communication interfaces characteristics

I²C interface characteristics

The I2C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to RM0351 reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.17: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to *Table 100* below for the analog filter characteristics:

Table 100. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

Figure 49. USB OTG timings – definition of data signal rise and fall time

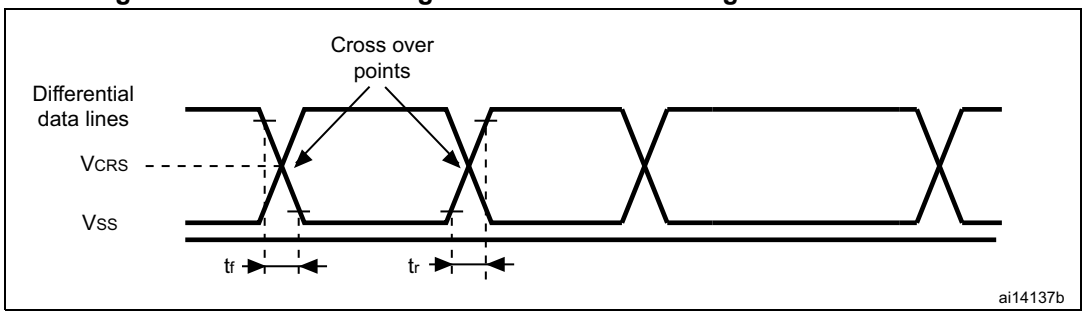


Table 104. USB OTG electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{rLS}	Rise time in LS(2)	C_L = 200 to 600 pF	75	300	ns
t_{fLS}	Fall time in LS(2)				
t_{rfmLS}	Rise/ fall time matching in LS	t_r / t_f	80	125	%
t_{rFS}	Rise time in FS(2)	C_L = 50 pF	4	20	ns
t_{fFS}	Fall time in FS(2)	C_L = 50 pF			
t_{rfmFS}	Rise/ fall time matching in FS	t_r / t_f	90	111	%
V_{CRS}	Output signal crossover voltage (LS/FS)	-	1.3	2.0	V
Z_{DRV}	Output driver impedance(3)	Driving high or low	28	44	Ω

1. Guaranteed by design
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

Table 105. USB BCD DC electrical characteristics(1)

Driver characteristics						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
$I_{DD(USBBCD)}$	Primary detection mode consumption	-	-	-	300	µA
	Secondary detection mode consumption	-	-	-		
RDAT_LKG	Data line leakage resistance	-	300	-	-	kΩ
VDAT_LKG	Data line leakage voltage	-	0.0	-	3.6	V
RDCP_DAT	Dedicated charging port resistance across D+/D-	-	-	-	200	Ω
VLGC_HI	Logic high	-	2.0	-	3.6	V
VLGC_LOW	Logic low	-	-	-	0.8	V

Figure 53. Asynchronous multiplexed PSRAM/NOR write waveforms

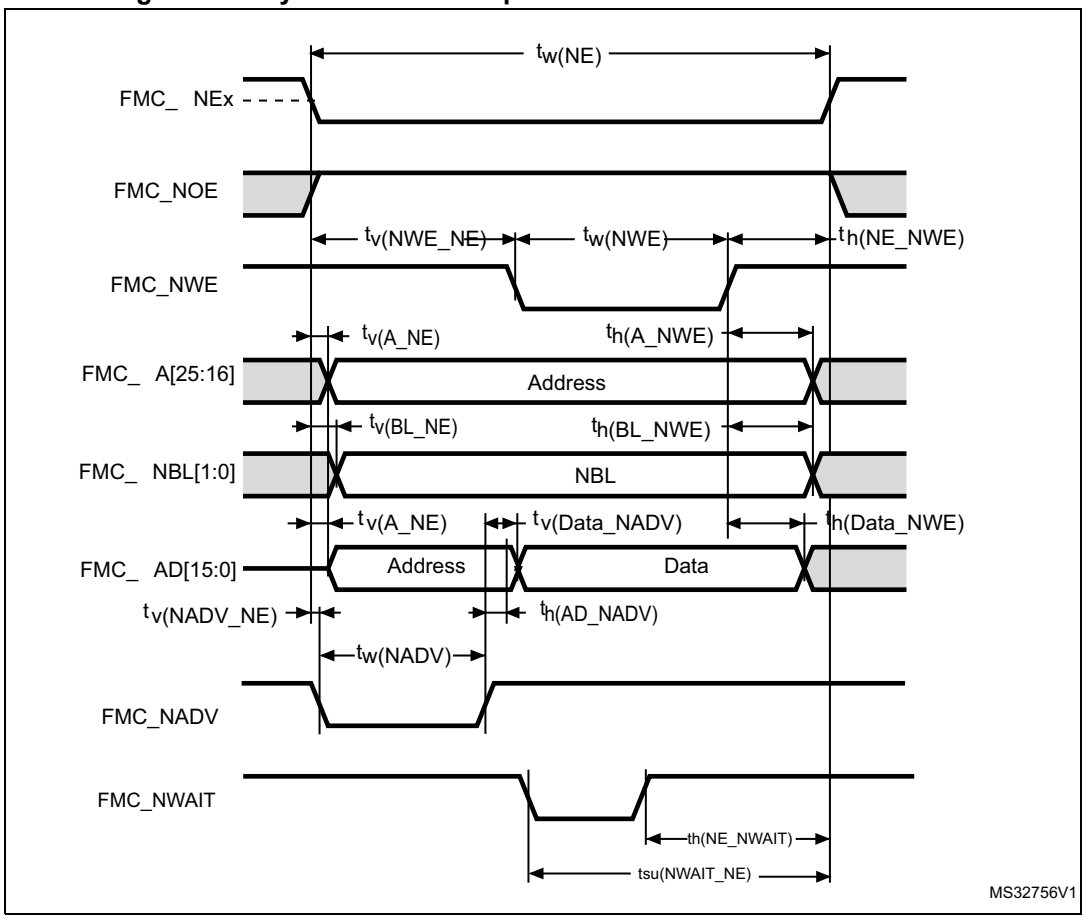


Table 112. Asynchronous multiplexed PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$5T_{HCLK}$-0.5	$5T_{HCLK}$+1	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	T_{HCLK}-0.5	T_{HCLK}+1	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{HCLK}$-0.5	$2T_{HCLK}$+0.5	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$2T_{HCLK}$-0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	3	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	1	
$t_{w(NADV)}$	FMC_NADV low time	T_{HCLK}+0.5	T_{HCLK}+1.5	
$t_{h(AD\_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high	T_{HCLK}-3	-	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	0	-	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$2T_{HCLK}$-0.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	T_{HCLK}	
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	T_{HCLK}+2	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$2T_{HCLK}$+0.5	-	

Table 121. OctoSPI(1) characteristics in DTR mode (no DQS)(2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	OctoSPI clock frequency	1.71 V < V_{DD} < 3.6 V Voltage Range 1 C_{LOAD} = 20 pF		-	-	58	MHz
		2.7 V < V_{DD} < 3.6 V Voltage Range 1 C_{LOAD} = 20 pF		-	-	60	
		1.71 V < V_{DD} < 3.6 V Voltage Range 1 C_{LOAD} = 15 pF		-	-	60	
		1.71 V < V_{DD} < 3.6 V Voltage Range 2 C_{LOAD} = 20 pF		-	-	26	
$t_{w(CKH)}$	OctoSPI clock high and low time	-		$t_{(CK)}$/2-1	-	$t_{(CK)}$/2+0.5	ns
$t_{w(CKL)}$				$t_{(CK)}$/2-1	-	$t_{(CK)}$/2+0.5	
$t_{sf(IN)}$ $t_{sr(IN)}$	Data input setup time	Voltage Range 1		0.5	-	-	
		Voltage Range 2		1	-	-	
$t_{hf(IN)}$ $t_{hr(IN)}$	Data input hold time	Voltage Range 1		7.75	-	-	
		Voltage Range 2		10.75	-	-	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time	Voltage Range 1	DHQC = 0	-	4.5	6	
			DHQC = 1 Pres=1,2 ...		tpclk/4+1	tpclk/4+3	
		Voltage Range 2	DHQC = 0		8.5	12	
$t_{hr(OUT)}$ $t_{hf(OUT)}$	Data output hold time	Voltage Range 1	DHQC = 0	1	-	-	
			DHQC = 1 Pres=1,2 ...	tpclk/4-2	-	-	
		Voltage Range 2	DHQC = 0	3.5	-	-	

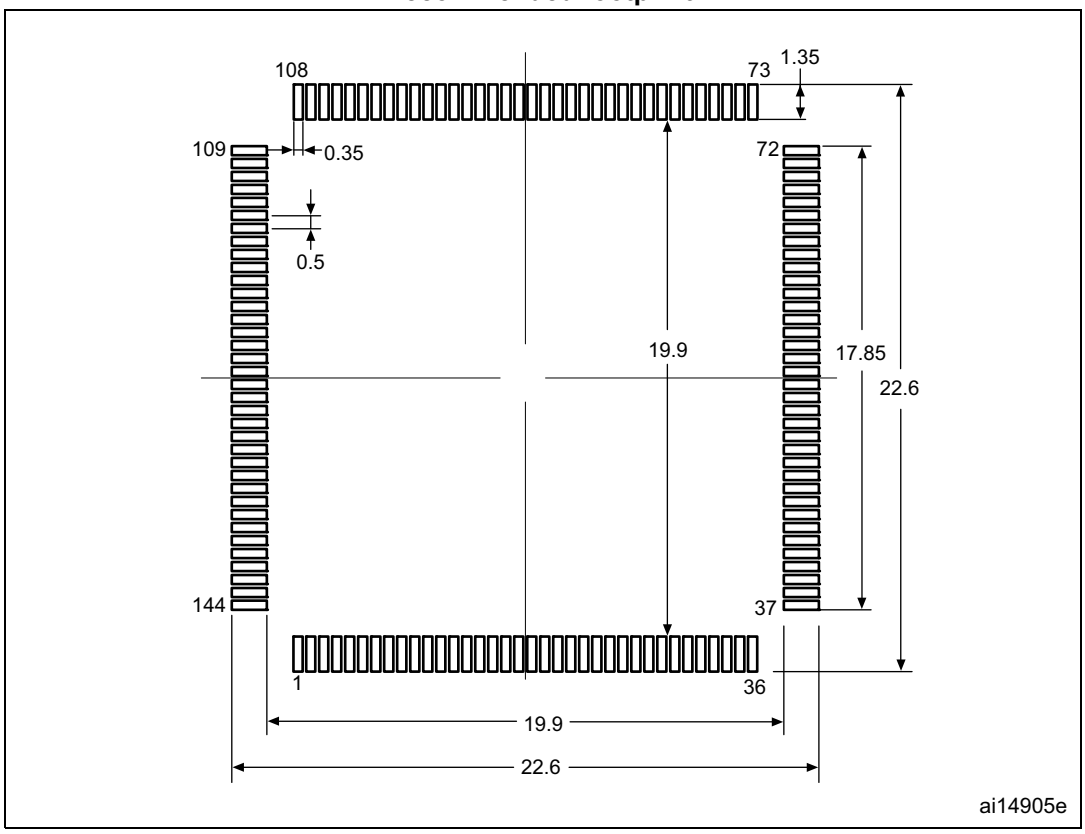
1. Values in the table applies to Octal and Quad SPI mode.
2. Guaranteed by characterization results.

Table 122. OctoSPI characteristics in DTR mode (with DQS)(1)/Octal and Hyperbus (continued)

Symbol	Parameter	Conditions		Min	Typ	Max(2)	Unit
$t_{w(CKH)}$	OctoSPI clock high and low time	-		$t_{(CK)}/2-1$	-	$t_{(CK)}/2+0.5$	ns
$t_{w(CKL)}$				$t_{(CK)}/2-0.5$	-	$t_{(CK)}/2+0.5$	
$t_{v(CK)}$	Clock valid time	-		-	-	$t_{(CK)}+1$	
$t_{h(CK)}$	Clock hold time	-		$t_{(CK)}/2-0.5$	-	-	
$t_{w(CS)}$	Chip select high time	-		3 x $t_{(CK)}$	-	-	
$t_{v(DQ)}$	Data input vallid time	-		0	-	-	
$t_{v(DS)}$	Data storbe input valid time	-		0	-	-	
$t_{h(DS)}$	Data storbe input hold time	-		0	-	-	
$t_{v(RWDS)}$	Data storbe output valid time	-		-	-	3 x $t_{(CK)}$	
$t_{sr(IN)}$ $t_{sf(IN)}$	Data input setup time	Voltage Range 1		-3.5	-	$t_{(CK)}/2-5.75$(3)	
		Voltage Range 2		-5.5	-	$t_{(CK)}/2-9$(3)	
$t_{hr(IN)}$ $t_{hf(IN)}$	Data input hold time	Voltage Range 1		5.75	-	-	
		Voltage Range 2		9	-	-	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time	Voltage Range 1	DHQC = 0	-	4.5	6	ns
			DHQC = 1 Pres=1,2 ...		tpclk/4+1.5	tpclk/4+2.25	
		Voltage Range 2	DHQC = 0		8	11	
$t_{hr(OUT)}$ $t_{hf(OUT)}$	Data output hold time	Voltage Range 1	DHQC = 0	0.5	-	-	
			DHQC = 1 Pres=1,2 ...	tpclk/4-1.75	-	-	
		Voltage Range 2	DHQC = 0	0.75	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency values are given for a RWDS to DQ skew of maximum +/-1.0 ns.
3. Data input setup time maximum does not take into account Data level switching duration.

Figure 79. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint



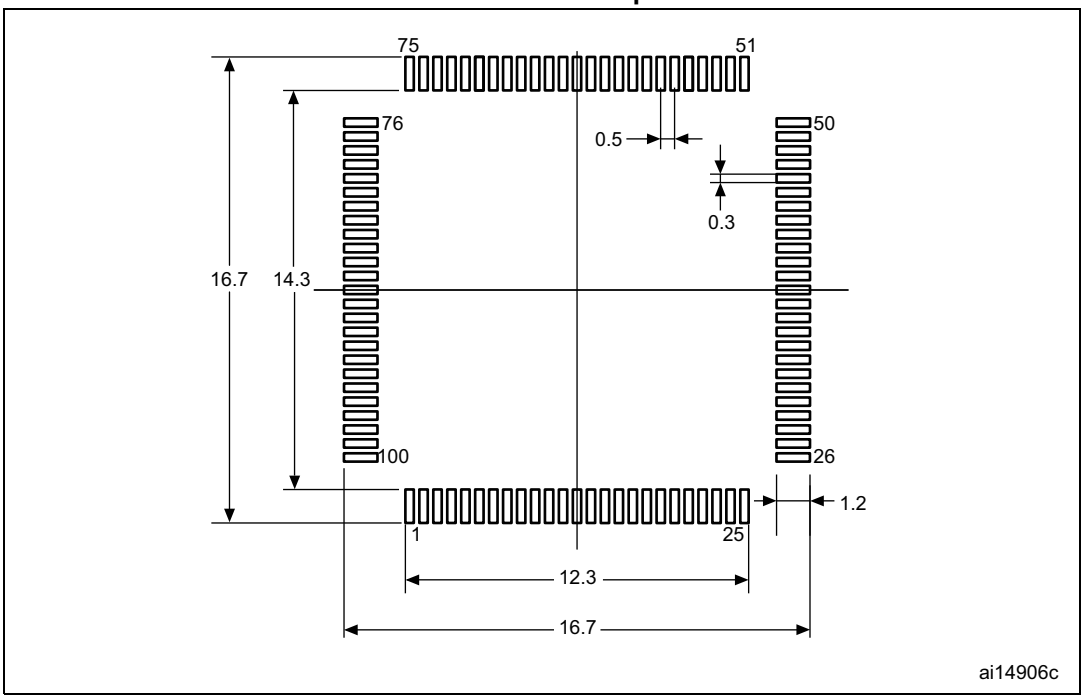
1. Dimensions are expressed in millimeters.

Table 136. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 89. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

LQFP100 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.