Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, SAI, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	112
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-UFBGA, WLCSP
Supplier Device Package	144-WLCSP (5.24x5.24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l4r9ziy6tr

Contents

The main features of the firewall are the following:

- Three segments can be protected and defined thanks to the firewall registers:
  - Code segment (located in Flash or SRAM1 if defined as executable protected area)
  - Non-volatile data segment (located in Flash)
  - Volatile data segment (located in SRAM1)
- The start address and the length of each segment are configurable:
  - Code segment: up to 2048 Kbytes with granularity of 256 bytes
  - Non-volatile data segment: up to 2048 Kbytes with granularity of 256 bytes
  - Volatile data segment: up to 192 Kbytes of SRAM1 with a granularity of 64 bytes
- Specific mechanism implemented to open the firewall to get access to the protected areas (call gate entry sequence)
- Volatile data segment can be shared or not with the non-protected code
- Volatile data segment can be executed or not depending on the firewall configuration

The Flash readout protection must be set to level 2 in order to reach the expected level of protection.

3.8 Boot modes

At startup, a BOOT0 pin and an nBOOT1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The BOOT0 value may come from the PH3-BOOT0 pin or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

A Flash empty-check mechanism is implemented to force the boot from system Flash if the first Flash memory location is not programmed and if the boot selection is configured to boot from main Flash.

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI, CAN or USB OTG FS in device mode through the DFU (device firmware upgrade).

3.9 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator with polynomial value and size.

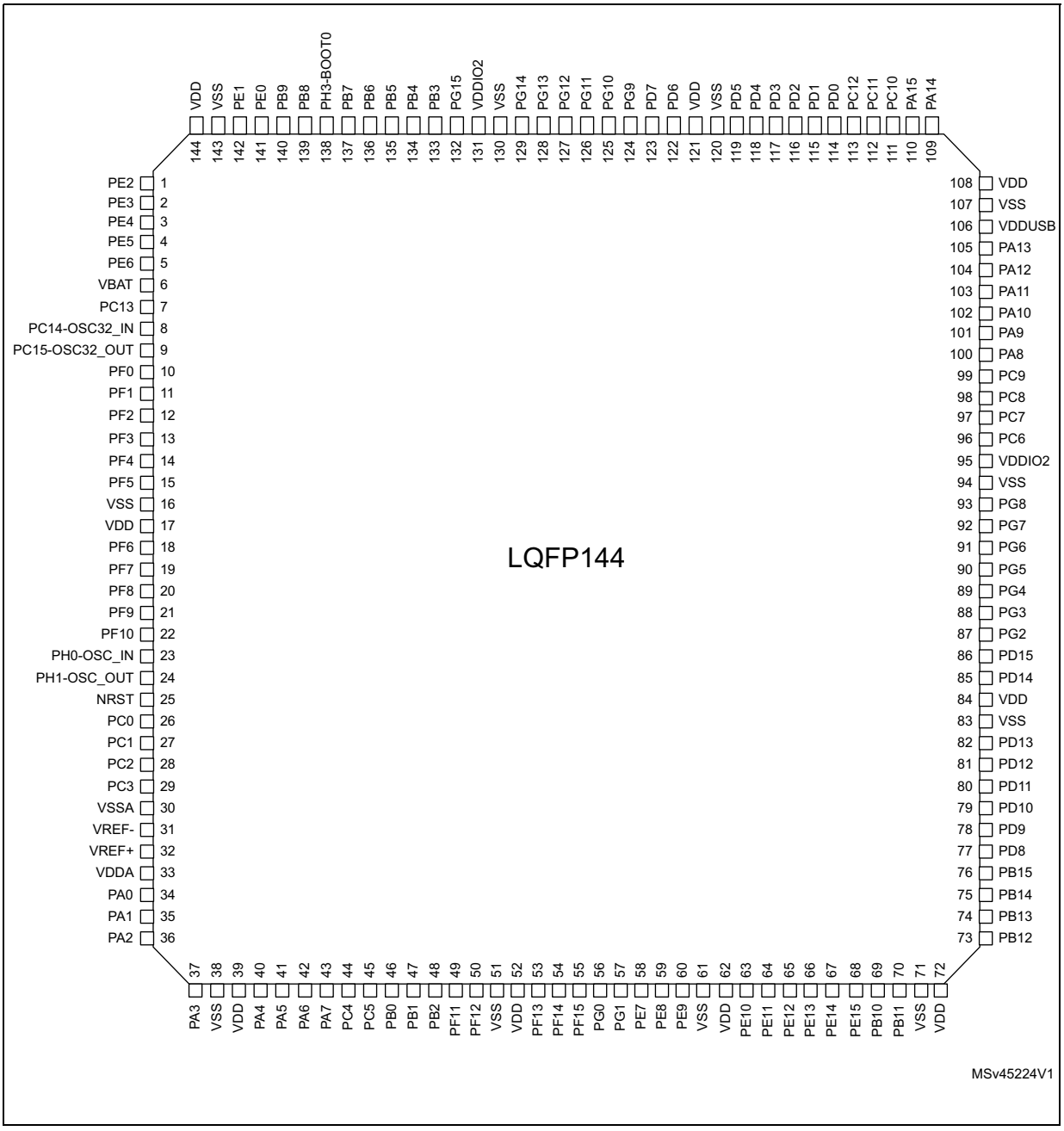
Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a mean to verify the Flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime, which can be ulteriorly compared with a reference signature generated at link-time and which can be stored at a given memory location.

Table 5. Functionalities depending on the working mode(1)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CPU	Y	-	Y	-	-	-	-	-	-	-	-	-	-
Flash memory (2 Mbytes)	O(2)	O(2)	O(2)	O(2)	-	-	-	-	-	-	-	-	-
SRAM1 (192 Kbytes)	Y	Y(3)	Y	Y(3)	Y	-	Y	-	-	-	-	-	-
SRAM2 (64 Kbytes)	Y	Y(3)	Y	Y(3)	Y	-	Y	-	O(4)	-	-	-	-
SRAM3 (384 Kbytes)	Y	Y(3)	Y	Y(3)	Y	-	Y(3)	-	-	-	-	-	-
FSMC	O	O	O	O	-	-	-	-	-	-	-	-	-
OctoSPIs	O	O	O	O	-	-	-	-	-	-	-	-	-
Backup Registers	Y	Y	Y	Y	Y	-	Y	-	Y	-	Y	-	Y
Brownout reset (BOR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	-
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	O	O	-	-	-	-	-
Peripheral Voltage Monitor (PVMx; x=1,2,3,4)	O	O	O	O	O	O	O	O	-	-	-	-	-
DMA	O	O	O	O	-	-	-	-	-	-	-	-	-
DMA2D	O	O	O	O	-	-	-	-	-	-	-	-	-
High speed internal (HSI16)	O	O	O	O	(5)	-	(5)	-	-	-	-	-	-
Oscillator HSI48	O	O	-	-	-	-	-	-	-	-	-	-	-
High speed external (HSE)	O	O	O	O	-	-	-	-	-	-	-	-	-
Low speed internal (LSI)	O	O	O	O	O	-	O	-	O	-	-	-	-
Low speed external (LSE)	O	O	O	O	O	-	O	-	O	-	O	-	O
Multi speed internal (MSI)	O	O	O	O	-	-	-	-	-	-	-	-	-
Clock security system (CSS)	O	O	O	O	-	-	-	-	-	-	-	-	-

Figure 12. STM32L4R5xx and STM32L4R7xx LQFP144 pinout(1)



1. The above figure shows the package top view.

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
-	-	-	-	-	-	-	-	58	79	J12	K2	K2	K12	DSI_CKN	I/O	-	(3)	-	-
-	-	-	-	-	-	-	-	59	80	-	-	-	-	VDD12DSI	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	H11	J2	J2	J11	DSI_D1P	I/O	-	(3)	-	-
-	-	-	-	-	-	-	-	-	-	H12	J1	J1	J12	DSI_D1N	I/O	-	(3)	-	-
-	-	-	-	-	-	-	-	-	-	J10	K3	K3	K13	VSSDSI	S	-	-	-	-
-	-	-	-	-	K3	-	-	-	-	-	-	-	-	VSS	S	-	-	-	-
-	-	-	-	-	L3	-	-	-	-	-	-	-	-	NC	-	-	-	-	-
-	-	-	-	-	L1	-	-	-	-	-	-	-	-	NC	-	-	-	-	-
-	-	-	-	-	L2	-	-	-	-	-	-	-	-	NC	-	-	-	-	-
-	-	-	-	-	K1	-	-	-	-	-	-	-	-	NC	-	-	-	-	-
-	-	-	-	-	K2	-	-	-	-	-	-	-	-	NC	-	-	-	-	-
-	-	-	-	-	J2	-	-	-	-	-	-	-	-	NC	-	-	-	-	-
-	-	-	-	-	J1	-	-	-	-	-	-	-	-	NC	-	-	-	-	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
68	D10	D10	101	101	D4	F10	F10	70	103	D10	D4	D4	E12	PA9	I/O	FT_flu	-	TIM1_CH2, SPI2_SCK, DCMI_D0, USART1_TX, SAI1_FS_A, TIM15_BKIN, EVENTOUT	OTG_FS_VBUS
69	C12	C12	102	102	D5	F9	F9	71	104	C10	D5	D5	D11	PA10	I/O	FT_flu	-	TIM1_CH3, SAI1_D1, DCMI_D1, USART1_RX, OTG_FS_ID, SAI1_SD_A, TIM17_BKIN, EVENTOUT	-
70	B12	B12	103	103	C1	E13	E13	72	105	B12	C1	C1	E13	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, USART1_CTS_NSS, CAN1_RX, OTG_FS_DM, EVENTOUT	-

Table 15. STM32L4Rxxx pin definitions (continued)

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
STM32L4R5xxx, STM32L4R7xxx								STM32L4R9xxx											
LQFP100	BGA132_SMPS	BGA132	LQFP144_SMPS	LQFP144	WLCSP144	UFBGA169_SMPS	UFBGA169	LQFP100	LQFP144	UFBGA144	WLCSP144_SMPS	WLCSP144	UFBGA169						
71	A12	A12	104	104	C2	D13	D13	73	106	B11	C2	C2	D13	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, USART1_RTS_DE, CAN1_TX, OTG_FS_DP, EVENTOUT	-
72	A11	A11	105	105	B3	A11	A11	74	107	B10	B3	B3	A11	PA13 (JTMS/ SWDIO)	I/O	FT	- (4)	JTMS/SWDIO, IR_OUT, OTG_FS_NOE, SAI1_SD_B, EVENTOUT	-
73	C11	C11	106	106	B2	E12	E12	75	108	C11	B2	B2	D12	VDDUSB	S	-	-	-	-
74	F11	F11	107	107	A1	C12	C12	76	109	A12	A1	A1	C12	VSS	S	-	-	-	-
75	G11	G11	108	108	B1	C13	C13	77	110	A11	B1	B1	C13	VDD	S	-	-	-	-
-	-	-	-	-	-	E11	E11	-	-	-	-	-	-	PH6	I/O	FT	-	I2C2_SMBA, OCTOSPIM_P2_CLK, DCMI_D8, EVENTOUT	-
-	-	-	-	-	-	D12	D12	-	-	-	-	-	-	PH7	I/O	FT_f	-	I2C3_SCL, DCMI_D9, EVENTOUT	-

Table 17. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port F	PF0	-	-	-	-	FMC_A0	-	-	EVENTOUT
	PF1	-	-	-	-	FMC_A1	-	-	EVENTOUT
	PF2	-	-	-	-	FMC_A2	-	-	EVENTOUT
	PF3	-	-	-	-	FMC_A3	-	-	EVENTOUT
	PF4	-	-	-	-	FMC_A4	-	-	EVENTOUT
	PF5	-	-	-	-	FMC_A5	-	-	EVENTOUT
	PF6	-	-	OCTOSPIM_P1_IO3	-	-	SAI1_SD_B	-	EVENTOUT
	PF7	-	-	OCTOSPIM_P1_IO2	-	-	SAI1_MCLK_B	-	EVENTOUT
	PF8	-	-	OCTOSPIM_P1_IO0	-	-	SAI1_SCK_B	-	EVENTOUT
	PF9	-	-	OCTOSPIM_P1_IO1	-	-	SAI1_FS_B	TIM15_CH1	EVENTOUT
	PF10	-	-	DCMI_D11	-	-	SAI1_D3	TIM15_CH2	EVENTOUT
	PF11	-	LCD_DE	DCMI_D12	DSI_TE	-	-	-	EVENTOUT
	PF12	-	-	-	LCD_B0	FMC_A6	-	-	EVENTOUT
	PF13	-	-	-	LCD_B1	FMC_A7	-	-	EVENTOUT
	PF14	-	TSC_G8_IO1	-	LCD_G0	FMC_A8	-	-	EVENTOUT
	PF15	-	TSC_G8_IO2	-	LCD_G1	FMC_A9	-	-	EVENTOUT

Table 17. Alternate function AF8 to AF15(1) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	OTG_FS/DCMI/ OCTOSPI_P1/P2	LCD	SDMMC/ COMP1/2/ FMC	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port G	PG0	-	TSC_G8_IO3	-	-	FMC_A10	-	-	EVENTOUT
	PG1	-	TSC_G8_IO4	-	-	FMC_A11	-	-	EVENTOUT
	PG2	-	-	-	-	FMC_A12	SAI2_SCK_B	-	EVENTOUT
	PG3	-	-	-	-	FMC_A13	SAI2_FS_B	-	EVENTOUT
	PG4	-	-	-	-	FMC_A14	SAI2_MCLK_B	-	EVENTOUT
	PG5	LPUART1_CTS	-	-	-	FMC_A15	SAI2_SD_B	-	EVENTOUT
	PG6	LPUART1_RTS_DE	LCD_R1	-	DSI_TE	-	-	-	EVENTOUT
	PG7	LPUART1_TX	-	-	-	FMC_INT	SAI1_MCLK_A	-	EVENTOUT
	PG8	LPUART1_RX	-	-	-	-	-	-	EVENTOUT
	PG9	-	-	-	-	FMC_NCE/FMC_NE2	SAI2_SCK_A	TIM15_CH1N	EVENTOUT
	PG10	-	-	-	-	FMC_NE3	SAI2_FS_A	TIM15_CH1	EVENTOUT
	PG11	-	-	-	-	-	SAI2_MCLK_A	TIM15_CH2	EVENTOUT
	PG12	-	-	-	-	FMC_NE4	SAI2_SD_A	-	EVENTOUT
	PG13	-	-	-	LCD_R0	FMC_A24	-	-	EVENTOUT
	PG14	-	-	-	LCD_R1	FMC_A25	-	-	EVENTOUT
	PG15	-	-	DCMI_D13	-	-	-	-	EVENTOUT

Table 22. General operating conditions (continued)

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDUSB}	USB supply voltage	USB used		3.0	3.6	V
		USB not used		0	3.6	
V_{IN}	I/O input voltage	TT_xx I/O		-0.3	V_{DDIOx}+0.3	
		BOOT0		0	9	
		All I/O except BOOT0 and TT_xx		-0.3	MIN(MIN(V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD})+3.6 V, 5.5 V)(3)(4)	
P_D	Power dissipation at T_A = 85 °C for suffix 6(5)	LQFP144	-	-	625	mW
		LQFP100	-	-	476	
		UFBGA169	-	-	385	
		UFBGA132	-	-	364	
		WLCSP144	-	-	664	
P_D	Power dissipation at T_A = 125 °C for suffix 3(5)	LQFP144	-	-	156	mW
		LQFP100	-	-	119	
		UFBGA169	-	-	96	
		UFBGA132	-	-	91	
		WLCSP144	-	-	831	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation		–40	85	°C
		Low-power dissipation(6)		–40	105	
	Ambient temperature for the suffix 3 version	Maximum power dissipation		–40	125	
		Low-power dissipation(6)		–40	130	
T_J	Junction temperature range	Suffix 6 version		–40	105	°C
		Suffix 3 version		–40	130	

1. When RESET is released functionality is guaranteed down to V_{BOR0} Min.
2. For Flash erase and program operation, V_{DD12} min must be 1.08 V.
3. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between MIN(V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB})+3.6 V and 5.5V.
4. For operation with voltage higher than Min (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
5. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.7: Thermal characteristics*).
6. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.7: Thermal characteristics*).

Table 36. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART enable (Cache ON Prefetch OFF) (continued)

Symbol	Parameter	Conditions		Code	TYP Single Bank Mode	TYP Dual Bank Mode	Unit	TYP Single Bank Mode	TYP Dual Bank Mode	Unit
		-	Voltage scaling		25°C	25°C		25°C	25°C	
I_{DD}(LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2MHz all pripherals disable		Reduced code(1)	490	460	µA	245	230	µA/MHz
				Coremark	520	515		260	258	
				Dhrystone2.1	530	530		265	265	
				Fibonacci	470	495		235	248	
				While(1)	455	515		228	258	

1. Reduced code used for characterization results provided in *Table 26*, *Table 30*, *Table 34*.

Table 41. Typical consumption in Run and Low-power run modes, with different codes running from SRAM1 and power supplied by external SMPS

Symbol	Parameter	Conditions(1)				TYP	Unit	TYP	Unit
		-	VDD12	fHCLK	Code	25°C		25°C	
IDD (Run)	Supply current in Run mode	fHCLK=fHSE up to 48 MHZ included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12=1.05 V	fHCLK= 26 MHz	Reduced code	1.32	mA	51	µA/MHz
					Coremark	1.22		47	
					Dhrystone2.1	1.43		55	
					Fibonacci	1.26		48	
					While(1)	1.12		43	
			VDD12=1.10V	fHCLK= 26 MHz	Reduced code	1.45	mA	56	µA/MHz
					Coremark	1.34		51	
					Dhrystone2.1	1.57		61	
					Fibonacci	1.38		53	
					While(1)	1.23		47	
				fHCLK= 80 MHz	Reduced code	3.95	mA	59	µA/MHz
					Coremark	3.77		57	
					Dhrystone2.1	4.49		67	
					Fibonacci	3.77		57	
					While(1)	3.38		51	
			VDD12=1.20V	fHCLK= 120 MHz	Reduced code	7.2	mA	60	µA/MHz
					Coremark	6.6		55	
					Dhrystone2.1	7.8		65	
					Fibonacci	7.0		58	
					While(1)	6.0		50	

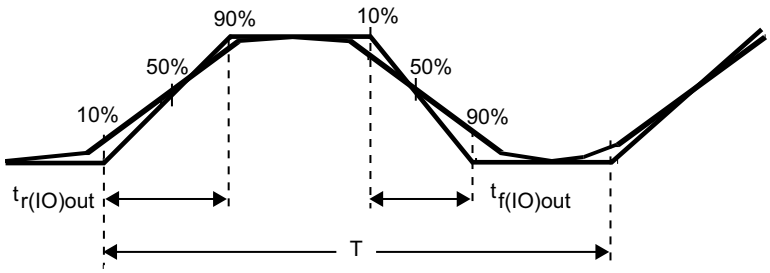
1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%.

Table 43. Current consumption in Sleep and Low-power sleep modes, Flash ON and power supplied by external SMPS

Symbol	Parameter	Conditions(1)			TYP					Unit
		-	VDD12	f_{HCLK}	25°C	55°C	85°C	105°C	125°C	
I_{DD}(Sleep)	Supply current in Sleep mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	VDD12=1.20V	120 MHz	1.68	1.89	2.51	3.37	4.81	mA
			VDD12=1.10V	80 MHz	1.01	1.17	1.67	2.37	3.59	
				72 MHz	0.92	1.08	1.58	2.30	3.54	
				64 MHz	0.83	0.99	1.51	2.21	3.45	
				48 MHz	0.77	0.93	1.44	2.16	3.40	
				32 MHz	0.56	0.72	1.22	1.92	3.16	
				26 MHz	0.47	0.63	1.10	1.79	3.02	
				16 MHz	0.33	0.50	0.97	1.64	2.87	
				8 MHz	0.22	0.38	0.84	1.53	2.74	
				4 MHz	0.16	0.32	0.80	1.47	2.70	
				2 MHz	0.14	0.27	0.75	1.45	2.65	
				1 MHz	0.12	0.26	0.75	1.42	2.63	
				100 KHz	0.11	0.25	0.73	1.40	2.63	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%.

Figure 39. I/O AC characteristics definition(1)



Maximum frequency is achieved if (t_r + t_f (≤ 2/3)T and if the duty cycle is (45-55%) when loaded by the specified capacitance.

MS32132V2

1. Refer to *Table 78: I/O AC characteristics*.

6.3.18 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

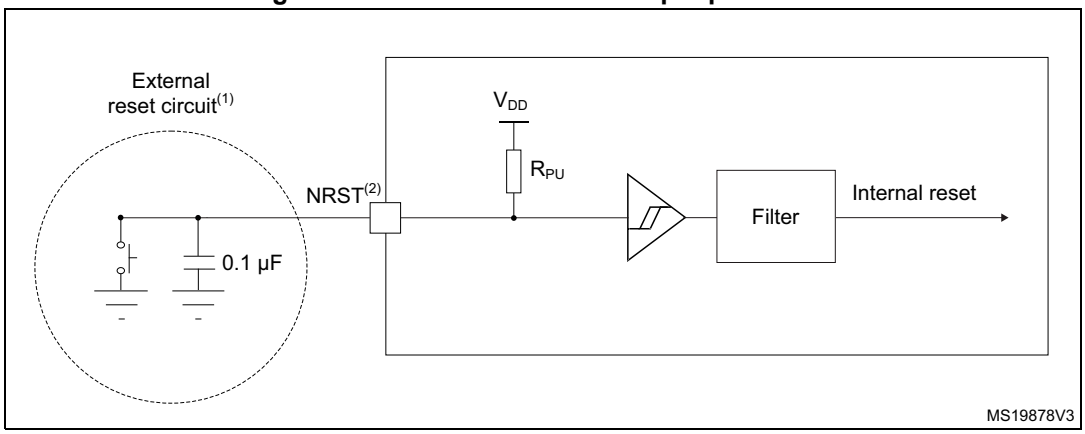
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 79. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3_x V_{DDIOx}$	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.7_x V_{DDIOx}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	70	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	350	-	-	ns

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Figure 40. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 79: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

6.3.19 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length in order to guarantee that it is detected by the event controller.

Table 80. EXTI input characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	20	-	-	ns

1. Guaranteed by design.

6.3.20 Analog switches booster

Table 81. Analog switches booster characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs
$I_{DD(BOOST)}$	Booster consumption for 1.62 V ≤ V_{DD} ≤ 2.0 V	-	-	250	µA
	Booster consumption for 2.0 V ≤ V_{DD} ≤ 2.7 V	-	-	500	
	Booster consumption for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	900	

1. Guaranteed by design.

Figure 51. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms

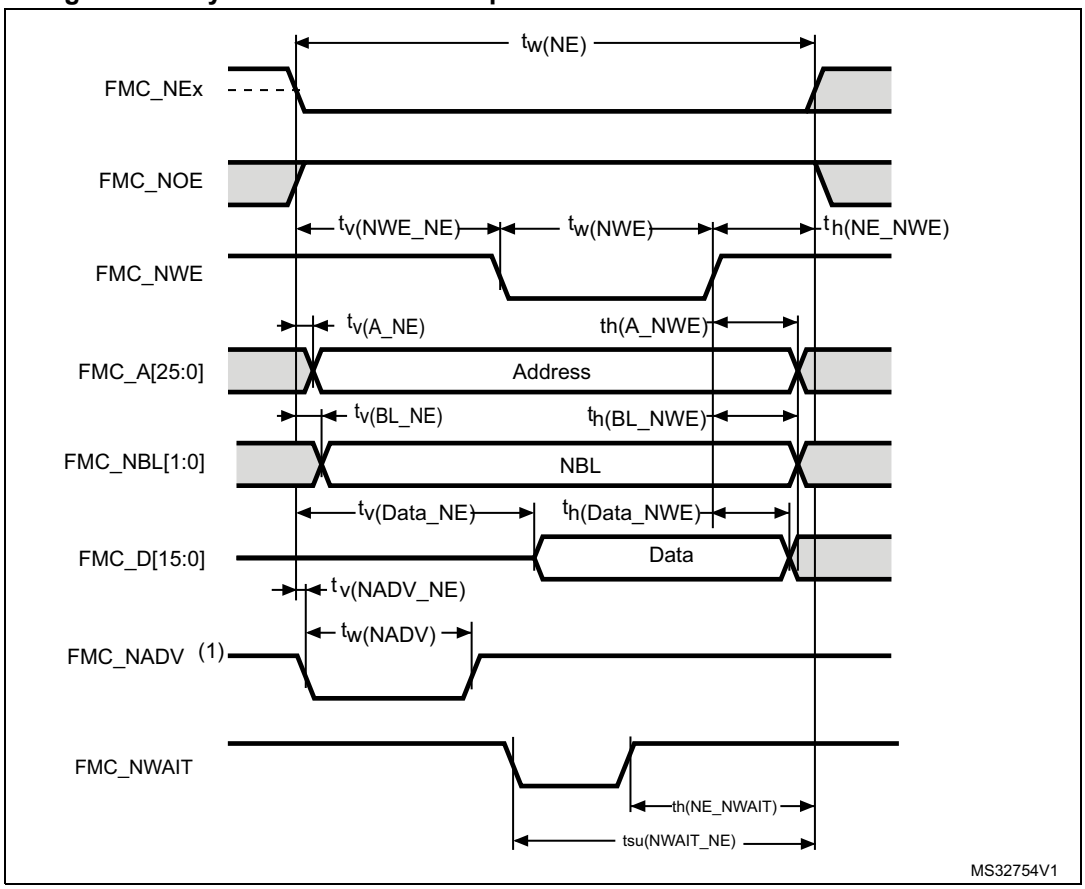


Table 108. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{HCLK}$-0.5	$4T_{HCLK}$+1	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	T_{HCLK}-0.5	T_{HCLK}+1	
$t_{w(NWE)}$	FMC_NWE low time	T_{HCLK}-0.5	T_{HCLK}+1	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$2T_{HCLK}$-0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	0	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	$2T_{HCLK}$-1	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	T_{HCLK}	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$2T_{HCLK}$-0.5	-	
$t_{v(Data\_NE)}$	Data to FMC_NEx low to Data valid	-	T_{HCLK}+3	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$2T_{HCLK}$+1	-	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	-	1	
$t_{w(NADV)}$	FMC_NADV low time	-	T_{HCLK}+1.5	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 117. Synchronous non-multiplexed PSRAM write timings(1)(2)(3)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	RxT_{HCLK}-0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	5.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	RxT_{HCLK}/2 +0.5	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	2	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	RxT_{HCLK}/2 +1	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	1	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	RxT_{HCLK}/2 +1.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	1.5	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.
3. Clock ratio R = (HCLK period /FMC_CLK period).

NAND controller waveforms and timings

Figure 58 through *Figure 61* represent synchronous waveforms, and *Table 118* and *Table 119* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 65. OctoSPI Hyperbus read

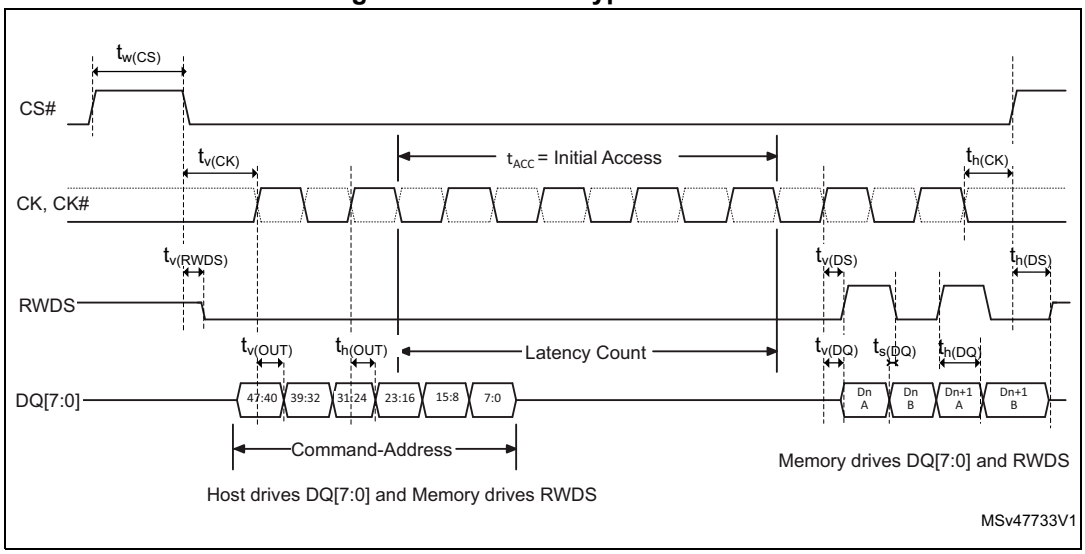


Figure 66. OctoSPI Hyperbus read with double latency

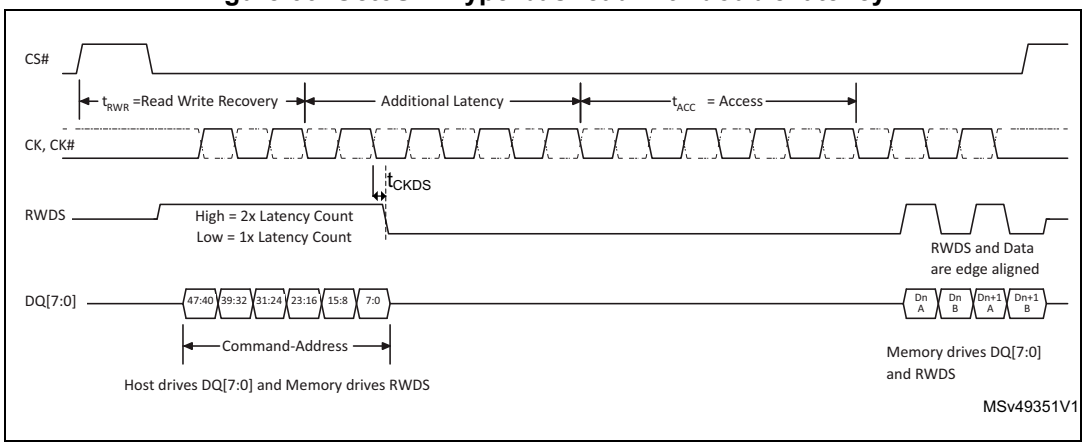


Figure 67. OctoSPI Hyperbus write

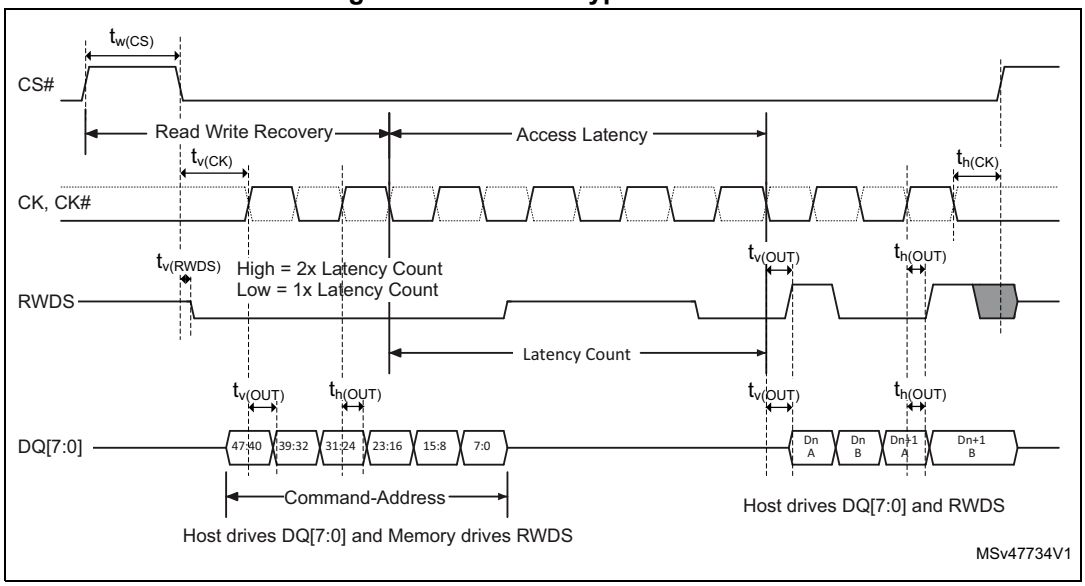


Table 129. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.080	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 76. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package recommended footprint

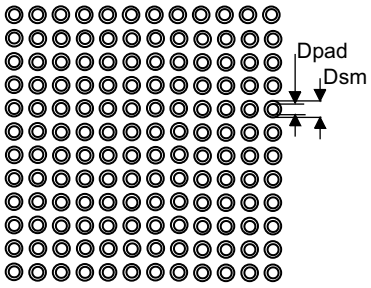


Table 130. UFBGA144 recommended PCB design rules (0.80 mm pitch BGA)

Dimension	Recommended values
Pitch	0.80 mm
Dpad	0.400 mm
Dsm	0.550 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm