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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	DMA, I ² S, LCD, LVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 20x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl33z128vlh4r

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1.4 Voltage and current operating ratings

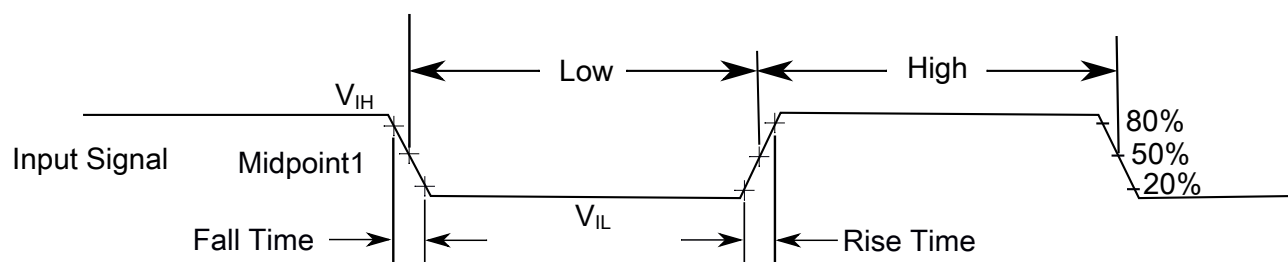
Table 4. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	IO pin input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 1. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- $C_L=30$ pF loads
- Slew rate disabled
- Normal drive strength

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 5. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V_{DD} -to- V_{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V_{SS} -to- V_{SSA} differential voltage	-0.1	0.1	V	
V_{IH}	Input high voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	$0.7 \times V_{DD}$	—	V	
		$0.75 \times V_{DD}$	—	V	
V_{IL}	Input low voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	—	$0.35 \times V_{DD}$	V	
		—	$0.3 \times V_{DD}$	V	
V_{HYS}	Input hysteresis	$0.06 \times V_{DD}$	—	V	
I_{ICIO}	IO pin negative DC injection current — single pin $V_{IN} < V_{SS}-0.3\text{V}$	-3	—	mA	1
I_{ICont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins Negative current injection	-25	—	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	2
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	

1. All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} greater than V_{IO_MIN} ($= V_{SS}-0.3\text{ V}$) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|$.
2. Open drain outputs must be pulled to V_{DD} .

2.2.2 LVD and POR operating requirements

Table 6. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	—
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	—
	Low-voltage warning thresholds — high range					1

Table continues on the next page...

Table 8. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• VLPS → RUN	—	7.5	8	μs	
	• STOP → RUN	—	7.5	8	μs	

1. Normal boot (FTFA_FOPT[LPBOOT]=11)

2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

NOTE

The while (1) test is executed with flash cache enabled.

Table 9. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_RUNCO}	Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V _{DD} = 3.0 V - at 25 °C - at 105 °C	— —	5.76 6.04	6.40 6.68	mA	2
I _{DD_RUNCO}	Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V _{DD} = 3.0 V - at 25 °C - at 105 °C	— —	3.21 3.49	3.85 4.13	mA	
I _{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, V _{DD} = 3.0 V - at 25 °C - at 105 °C	— —	6.45 6.75	7.09 7.39	mA	2
I _{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, V _{DD} = 3.0 V - at 25 °C - at 105 °C	— —	3.95 4.23	4.59 4.87	mA	2

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 12 MHz core/6 MHz flash, $V_{DD} = 3.0\text{ V}$ - at 25 °C - at 105 °C	— —	2.68 2.96	3.32 3.60	mA	2
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock enable 48 MHz core/24 MHz flash, $V_{DD} = 3.0\text{ V}$ - at 25 °C - at 105 °C	— —	8.08 8.39	8.72 9.03	mA	2
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in flash all peripheral clock disable, 48 MHz core/24 MHz flash, $V_{DD} = 3.0\text{ V}$ - at 25 °C - at 105 °C	— —	3.90 4.21	4.54 4.85	mA	
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in Flash all peripheral clock disable, 24 MHz core/12 MHz flash, $V_{DD} = 3.0\text{ V}$ - at 25 °C - at 105 °C	— —	2.66 2.94	3.30 3.58	mA	
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock disable, 12 MHz core/6 MHz flash, $V_{DD} = 3.0\text{ V}$ - at 25 °C - at 105 °C	— —	2.03 2.31	2.67 2.95	mA	
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock enable, 48 MHz core/24 MHz flash, $V_{DD} = 3.0\text{ V}$ - at 25 °C - at 105 °C	— —	5.52 5.83	6.16 6.47	mA	
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock disable, 48 MHz core/24 MHz flash, $V_{DD} = 3.0\text{ V}$ - at 25 °C - at 105 °C	— —	5.29 5.56	5.93 6.20	mA	
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock enable, 48 MHz core/24 MHz flash, $V_{DD} = 3.0\text{ V}$ - at 25 °C - at 105 °C	— —	6.91 7.19	7.55 7.91	mA	

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 1.8 V - at 25 °C and below - at 50 °C - at 70 °C - at 85 °C - at 105 °C	—	1.96	2.36	μA	3
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V - at 25 °C and below - at 50 °C - at 70 °C - at 85 °C - at 105 °C	—	0.66	0.80	μA	
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 3.0 V - at 25 °C and below - at 50 °C - at 70 °C - at 85 °C - at 105 °C	—	1.26	1.40	μA	3
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 1.8 V - at 25 °C and below - at 50 °C - at 70 °C - at 85 °C - at 105 °C	—	1.16	1.30	μA	3
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 0) at 3.0 V - at 25 °C and below - at 50 °C - at 70 °C - at 85 °C - at 105 °C	—	0.35	0.47	μA	
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 1) at 3 V					

Table 10. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
								nA
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	μA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. • IRC8M (8 MHz internal reference clock) • IRC2M (2 MHz internal reference clock)	114	114	114	114	114	114	μA
		34	34	34	34	34	34	
I_{TPM}	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents. • IRC8M (8 MHz internal reference clock) • IRC2M (2 MHz internal reference clock)	147	147	147	147	147	147	μA
		42	42	42	42	42	42	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx or VLLSx mode.	45	45	45	45	45	45	μA
I_{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	330	330	330	330	330	330	μA
I_{LCD}	LCD peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the OSC0_CR[EREFSTEN, EREFSTEN] bits. VIREG disabled, resistor bias network enabled, 1/8 duty cycle, 8 x 36 configuration for driving 288 Segments, 32 Hz frame rate, no LCD glass connected. Includes ERCLK32K (32 kHz external crystal) power consumption.	4.5	4.5	4.5	4.5	4.5	4.5	μA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG-Lite in HIRC for run mode, and LIRC for VLPR mode
- No GPIOs toggled
- Code execution from flash
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

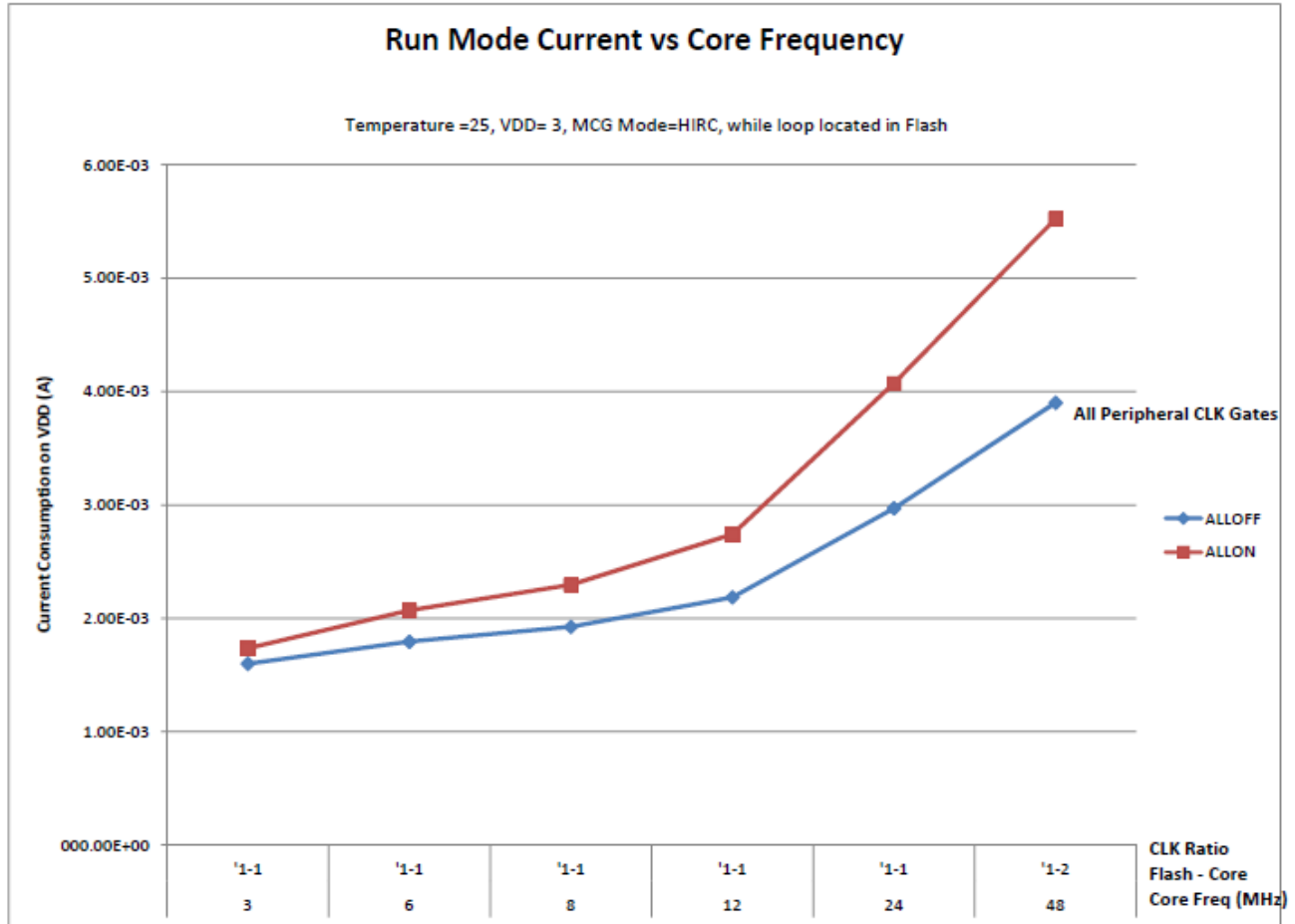


Figure 2. Run mode supply current vs. core frequency

Cell and Wideband TEM Cell Method. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, $f_{OSC} = \text{IRC48M}$, $f_{SYS} = 48\text{ MHz}$, $f_{BUS} = 24\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 12. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN}	Input capacitance	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 13. Device clock specifications

Symbol	Description	Min.	Max.	Unit
Normal run mode				
f_{SYS}	System and core clock ¹	—	48	MHz
f_{BUS}	Bus clock ¹	—	24	MHz
f_{FLASH}	Flash clock ¹	—	24	MHz
f_{LPTMR}	LPTMR clock	—	24	MHz
VLPR and VLPS modes ²				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	1	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{LPTMR}	LPTMR clock ³	—	24	MHz
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz

Table continues on the next page...

3.1.1 SWD electricals

Table 17. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

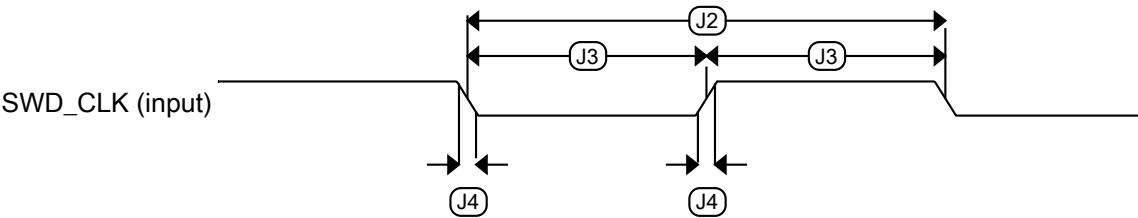


Figure 4. Serial wire clock input timing

Table 20. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	24 MHz 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1) 32 kHz 4 MHz 8 MHz (RANGE=01) 16 MHz 24 MHz 32 MHz	—	25	—	μ A	1
		—	400	—	μ A	
		—	500	—	μ A	
		—	2.5	—	mA	
		—	3	—	mA	
		—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	M Ω	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	M Ω	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	M Ω	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	M Ω	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	k Ω	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	k Ω	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	k Ω	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	k Ω	
V_{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD} =3.3 V, Temperature =25 °C

2. See crystal or resonator manufacturer's recommendation

3.6.1.1 16-bit ADC operating conditions

Table 26. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	—
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	3
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	3
V_{ADIN}	Input voltage	16-bit differential mode - All other modes	V_{REFL} V_{REFL}	— —	$31/32 \times V_{REFH}$ V_{REFH}	V	—
C_{ADIN}	Input capacitance	16-bit mode 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	—
R_{ADIN}	Input series resistance		—	2	5	k Ω	—
R_{AS}	Analog source resistance (external)	13-bit / 12-bit modes $f_{ADCK} < 4$ MHz	—	—	5	k Ω	4
f_{ADCK}	ADC conversion clock frequency	$\leq$ 13-bit mode	1.0	—	24	MHz	5
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	5
C_{rate}	ADC conversion rate	$\leq$ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	1200	ksps	6
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	ksps	6

1. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 1.0$ MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. V_{REFH} can act as V_{REF_OUT} when V_{REFV1} module is enabled.
4. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had $< 8 \Omega$ analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
5. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
6. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

Table 27. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
					−0.7 to +0.5		
E_{FS}	Full-scale error	12-bit modes <12-bit modes	—	−4	−5.4	LSB ⁴	$V_{ADIN} = V_{DDA}$ ⁵
E_Q	Quantization error	16-bit modes ≤13-bit modes	—	−1 to 0	—	LSB ⁴	
					±0.5		
ENOB	Effective number of bits	16-bit differential mode - Avg = 32 - Avg = 4 16-bit single-ended mode - Avg = 32 - Avg = 4	12.8 11.9	14.5 13.8	— — — —	bits bits bits bits	⁶
SINAD	Signal-to-noise plus distortion	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	
THD	Total harmonic distortion	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	—	−94	—	dB dB	⁷
SFDR	Spurious free dynamic range	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	82 78	95 90	— —	dB dB	⁷
E_{IL}	Input leakage error		$I_{in} \times R_{AS}$			mV	I_{in} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	⁸
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	⁸

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$

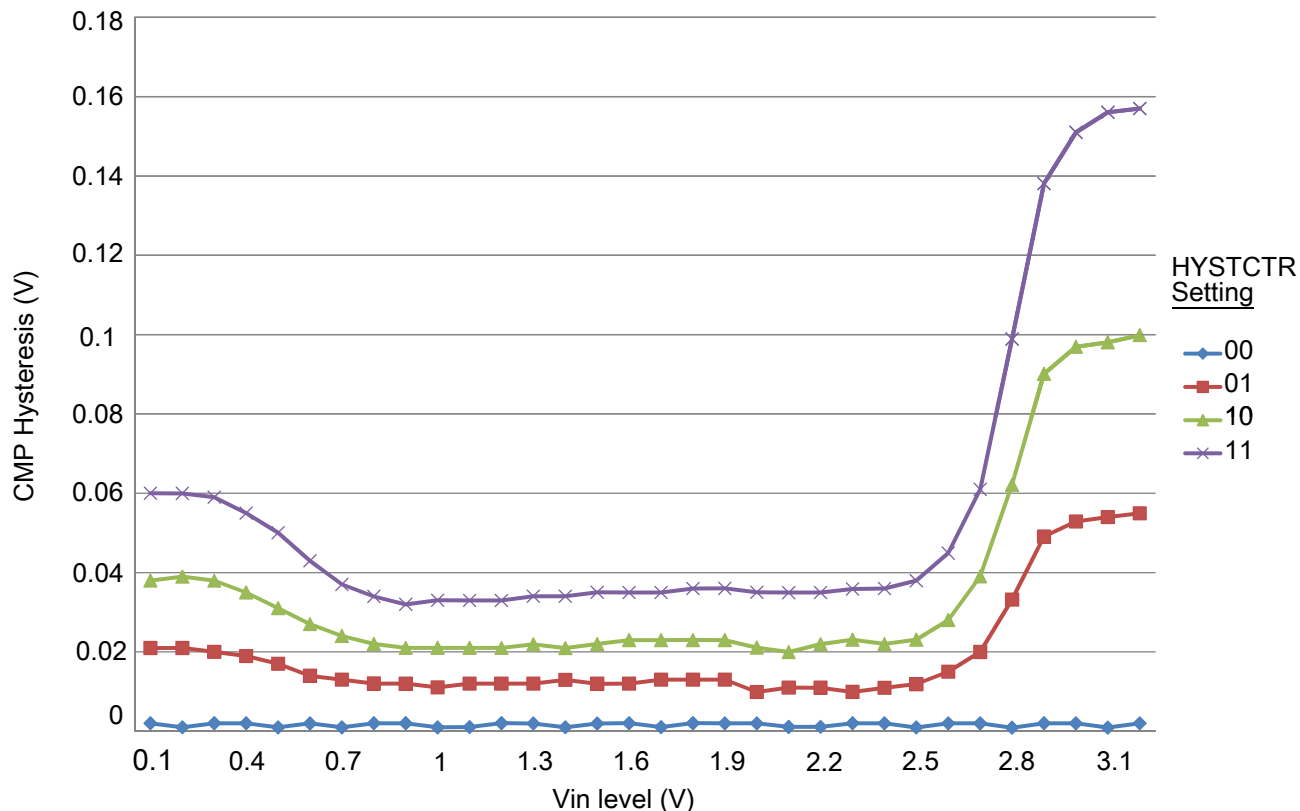


Figure 11. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.6.4 12-bit DAC electrical characteristics

3.6.4.1 12-bit DAC operating requirements

Table 33. 12-bit DAC operating requirements

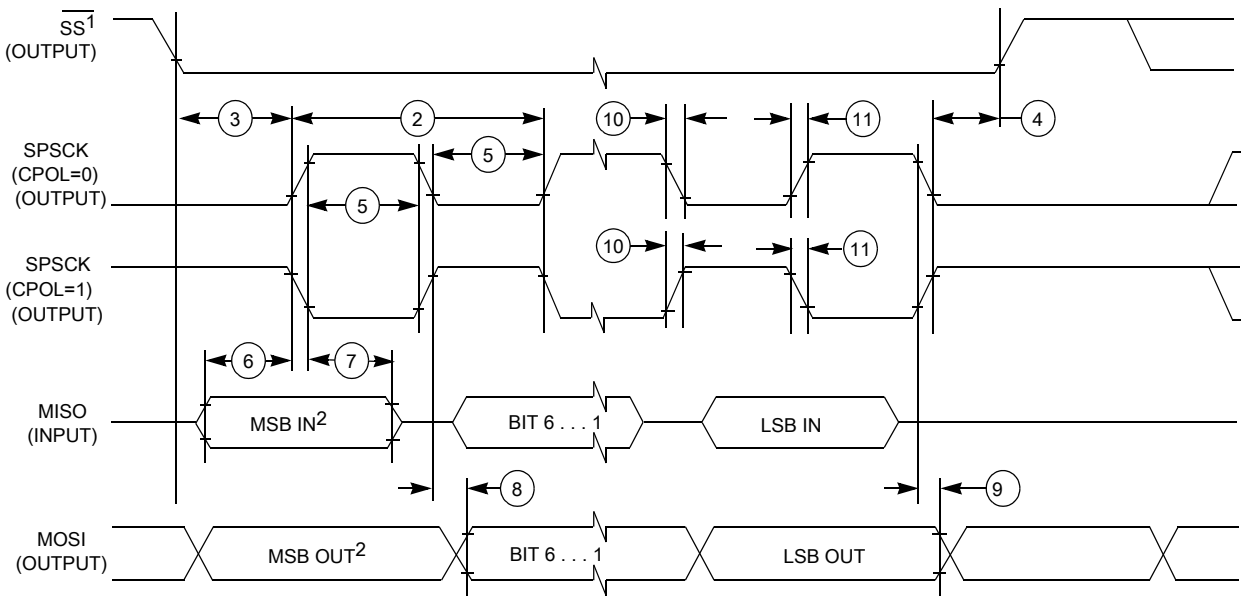
Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage		3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH} .
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

Table 36. SPI master mode timing on slew rate enabled pads (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Note
8	t_v	Data valid (after SPSCCK edge)	—	52	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	$t_{periph} - 25$	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 14. SPI master mode timing (CPHA = 0)

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can be achieved only when using the high drive pins across the full voltage range and when using the normal drive pins and $V_{DD} \geq 2.7$ V.
2. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum t_{HD; DAT} must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement t_{SU; DAT} ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t_{rmax} + t_{SU; DAT} = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification) before the SCL line is released.
7. C_b = total capacitance of the one bus line in pF.

To achieve 1MHz I2C clock rates, consider the following recommendations:

- To counter the effects of clock stretching, the I2C baud Rate select bits can be configured for faster than desired baud rate.
- Use high drive pad and DSE bit should be set in PORTx_PCRn register.
- Minimize loading on the I2C SDA and SCL pins to ensure fastest rise times for the SCL line to avoid clock stretching.
- Use smaller pull up resistors on SDA and SCL to reduce the RC time constant.

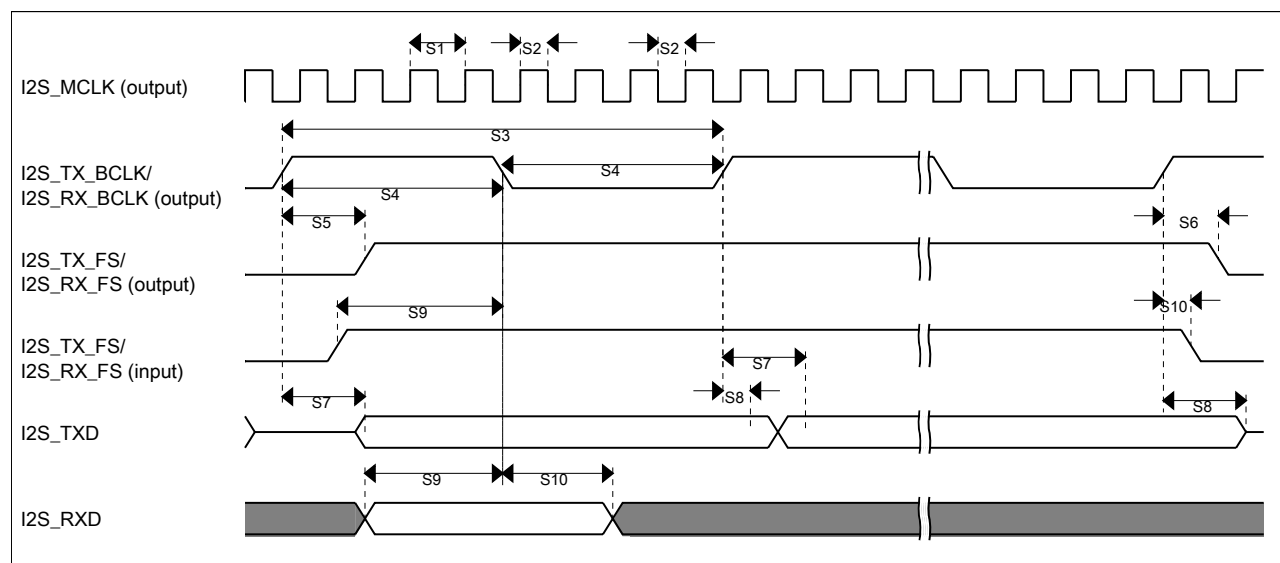
Table 40. I²C 1Mbit/s timing

Characteristic	Symbol	Minimum	Maximum	Unit
SCL Clock Frequency	f _{SCL}	0	1 ¹	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t _{HD; STA}	0.26	—	μs
LOW period of the SCL clock	t _{LOW}	0.5	—	μs
HIGH period of the SCL clock	t _{HIGH}	0.26	—	μs
Set-up time for a repeated START condition	t _{SU; STA}	0.26	—	μs
Data hold time for I ² C bus devices	t _{HD; DAT}	0	—	μs
Data set-up time	t _{SU; DAT}	50	—	ns
Rise time of SDA and SCL signals	t _r	20 + 0.1C _b	120	ns
Fall time of SDA and SCL signals	t _f	20 + 0.1C _b ²	120	ns
Set-up time for STOP condition	t _{SU; STO}	0.26	—	μs
Bus free time between STOP and START condition	t _{BUF}	0.5	—	μs
Pulse width of spikes that must be suppressed by the input filter	t _{SP}	0	50	ns

1. The maximum SCL clock frequency of 1 Mbit/s can support maximum bus loading when using the high drive pins across the full voltage range.
2. C_b = total capacitance of the one bus line in pF.

Table 41. I2S/SAI master mode timing (continued)

Num.	Characteristic	Min.	Max.	Unit
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	19	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	26	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns


Figure 19. I2S/SAI timing — master modes
Table 42. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	33	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns

Table continues on the next page...

Table 42. I2S/SAI slave mode timing (continued)

Num.	Characteristic	Min.	Max.	Unit
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	28	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

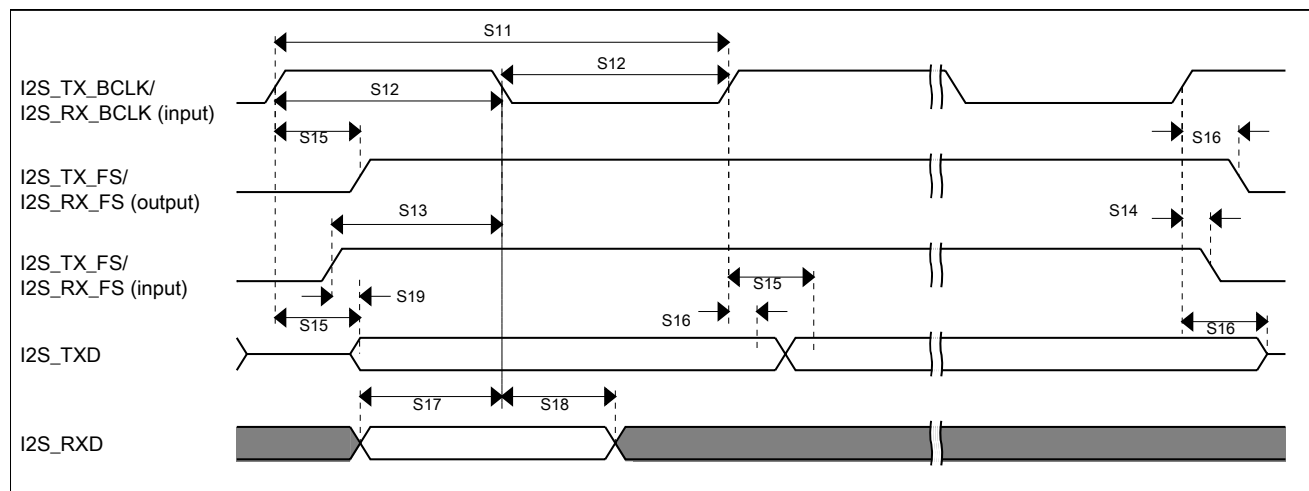


Figure 20. I2S/SAI timing — slave modes

3.8.4.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 43. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns

Table continues on the next page...

Table 43. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK		—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

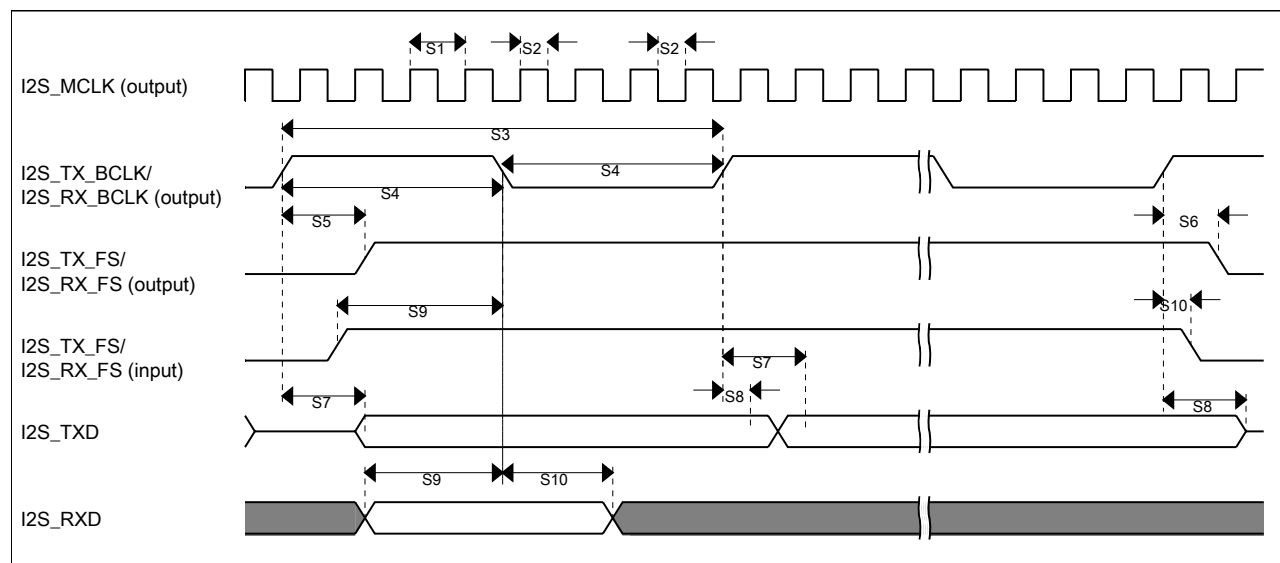


Figure 21. I2S/SAI timing — master modes

Table 44. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	87	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	72	ns

64 LQFP	64 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
58	A4	PTD1	LCD_P41/ ADC0_SE5b	LCD_P41/ ADC0_SE5b	PTD1	SPI0_SCK		TPM0_CH1		FXIO0_D1	LCD_P41
59	C2	PTD2	LCD_P42	LCD_P42	PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO	FXIO0_D2	LCD_P42
60	B3	PTD3	LCD_P43	LCD_P43	PTD3	SPI0_MISO	UART2_TX	TPM0_CH3	SPI0_MOSI	FXIO0_D3	LCD_P43
61	A3	PTD4/ LLWU_P14	LCD_P44	LCD_P44	PTD4/ LLWU_P14	SPI1_SS	UART2_RX	TPM0_CH4		FXIO0_D4	LCD_P44
62	C1	PTD5	LCD_P45/ ADC0_SE6b	LCD_P45/ ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5		FXIO0_D5	LCD_P45
63	B2	PTD6/ LLWU_P15	LCD_P46/ ADC0_SE7b	LCD_P46/ ADC0_SE7b	PTD6/ LLWU_P15	SPI1_MOSI	LPUART0_RX		SPI1_MISO	FXIO0_D6	LCD_P46
64	A2	PTD7	LCD_P47	LCD_P47	PTD7	SPI1_MISO	LPUART0_TX		SPI1_MOSI	FXIO0_D7	LCD_P47

5.2 KL33 Family Pinouts

Figure below shows the 64 LQFP pinouts: