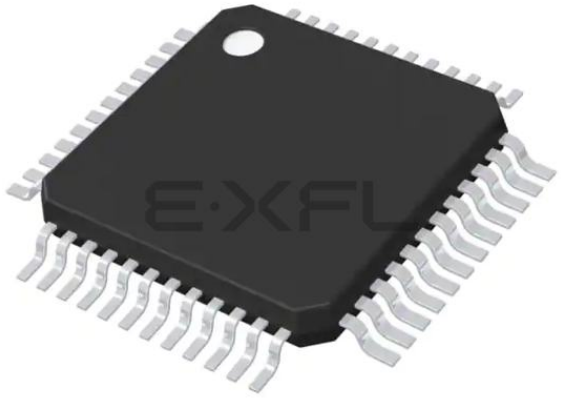
# Infineon Technologies - XC886CLM8FFAACAXUMA1 Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | XC800 |
| Core Size | 8-Bit |
| Speed | 24MHz |
| Connectivity | CANbus, LINbus, SSI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 34 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1.75K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.3V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 140°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | PG-TQFP-48 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xc886clm8ffaacaxuma1 |

## 2.2 Logic Symbol

The logic symbols of the SAA-XC886 are shown in **Figure 3**.

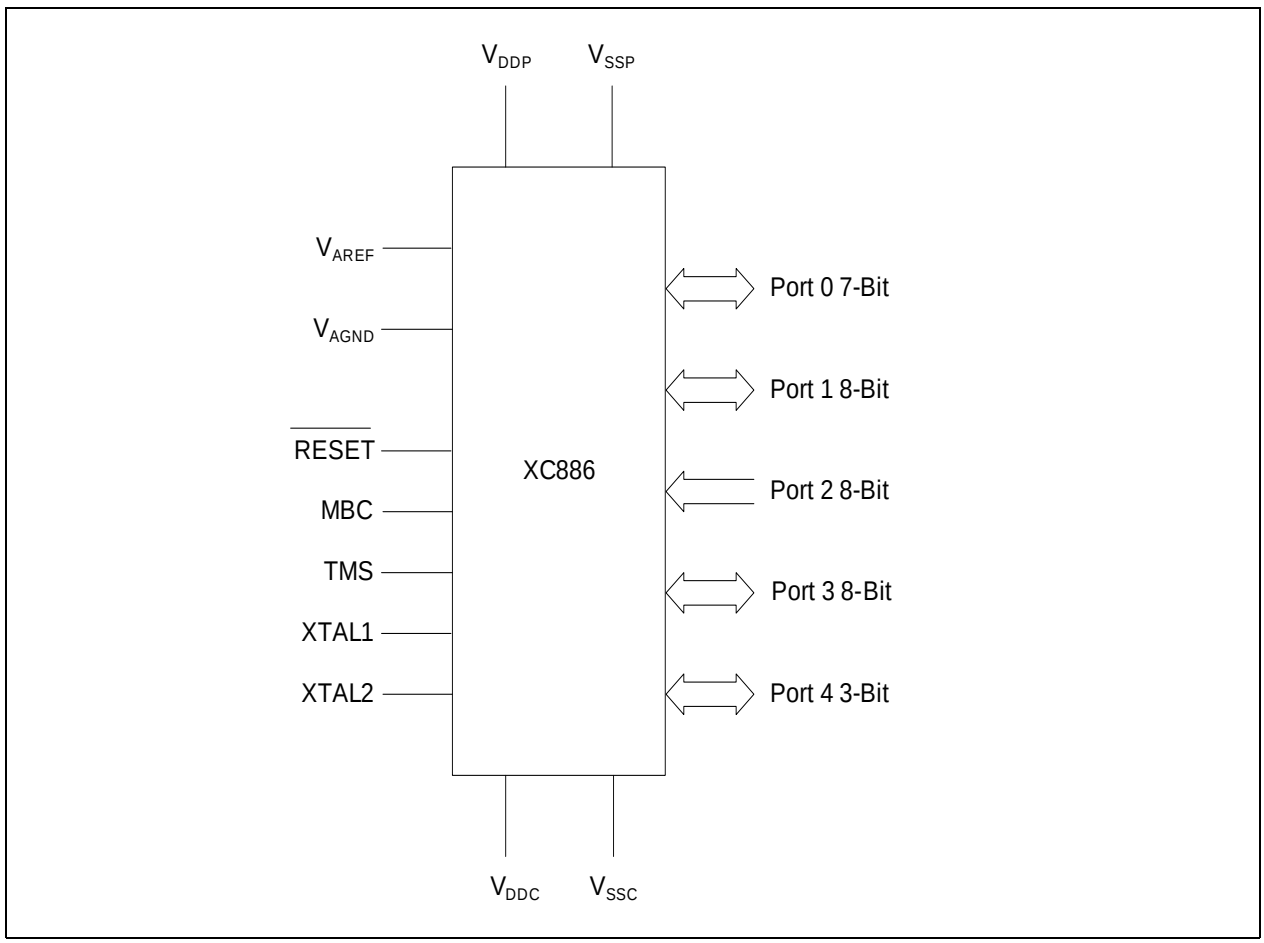



**Figure 3 SAA-XC886 Logic Symbol**

**Table 2 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Number | Type | Reset State | Function |
|---|---|---|---|---|
| **P2** | | I | | **Port 2**<br>Port 2 is an 8-bit general purpose input-only port. It can be used as alternate functions for the digital inputs of the JTAG and CCU6. It is also used as the analog inputs for the ADC. |
| P2.0 | 14 | | Hi-Z | CCPOS0_0 CCU6 Hall Input 0<br>EXINT1_0 External Interrupt Input 1<br>T12HR_2 CCU6 Timer 12 Hardware Run Input<br>TCK_1 JTAG Clock Input<br>CC61_3 Input of Capture/Compare channel 1<br>AN0 Analog Input 0 |
| P2.1 | 15 | | Hi-Z | CCPOS1_0 CCU6 Hall Input 1<br>EXINT2_0 External Interrupt Input 2<br>T13HR_2 CCU6 Timer 13 Hardware Run Input<br>TDI_1 JTAG Serial Data Input<br>CC62_3 Input of Capture/Compare channel 2<br>AN1 Analog Input 1 |
| P2.2 | 16 | | Hi-Z | CCPOS2_0 CCU6 Hall Input 2<br>CTRAP_1 CCU6 Trap Input<br>CC60_3 Input of Capture/Compare channel 0<br>AN2 Analog Input 2 |
| P2.3 | 19 | | Hi-Z | AN3 Analog Input 3 |
| P2.4 | 20 | | Hi-Z | AN4 Analog Input 4 |
| P2.5 | 21 | | Hi-Z | AN5 Analog Input 5 |
| P2.6 | 22 | | Hi-Z | AN6 Analog Input 6 |
| P2.7 | 25 | | Hi-Z | AN7 Analog Input 7 |

**Table 2 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Number | Type | Reset State | Function | |
|---|---|---|---|---|---|
| **P4** | | I/O | | **Port 4**<br>Port 4 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, Timer 0, Timer 1, Timer 21 and MultiCAN. | |
| P4.0 | 45 | | Hi-Z | RXDC0_3<br>CC60_1 | MultiCAN Node 0 Receiver Input<br>Output of Capture/Compare channel 0 |
| P4.1 | 46 | | Hi-Z | TXDC0_3<br>COUT60_1 | MultiCAN Node 0 Transmitter Output<br>Output of Capture/Compare channel 0 |
| P4.3 | 32 | | Hi-Z | EXF21_1<br>COUT63_2 | Timer 21 External Flag Output<br>Output of Capture/Compare channel 3 |

**SYSCON0**
**System Control Register 0** **Reset Value: $04_H$**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | **0** | | **IMODE** | **0** | **1** | **0** | **RMAP** |
| | r | | rw | r | r | r | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| **RMAP** | 0 | rw | **Interrupt Node XINTR0 Enable**<br>0 The access to the standard SFR area is enabled<br>1 The access to the mapped SFR area is enabled |
| **1** | 2 | r | **Reserved**<br>Returns 1 if read; should be written with 1. |
| **0** | [7:5], 3,1 | r | **Reserved**<br>Returns 0 if read; should be written with 0. |

*Note: The RMAP bit should be cleared/set by ANL or ORL instructions.*

### 3.2.2.2 Address Extension by Paging

Address extension is further performed at the module level by paging. With the address extension by mapping, the SAA-XC886 has a 256-SFR address range. However, this is still less than the total number of SFRs needed by the on-chip peripherals. To meet this requirement, some peripherals have a built-in local address extension mechanism for increasing the number of addressable SFRs. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit field PAGE in the module page register MOD_PAGE. Hence, the bit field PAGE must be programmed before accessing the SFR of the target module. Each module may contain a different number of pages and a different number of SFRs per page, depending on the specific requirement. Besides setting the correct RMAP bit value to select the SFR area, the user must also ensure that a valid PAGE is selected to target the desired SFR. A page inside the extended address range can be selected as shown in **Figure 8**.

**Table 7 SCU Register Overview** (cont'd)

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $BE_H$ | **COCON** **Reset: $00_H$** Clock Output Control Register | Bit Field | 0 | | TLEN | COUTS | COREL | | | |
| | | Type | r | | rw | rw | rw | | | |
| $E9_H$ | **MISC_CON** **Reset: $00_H$** Miscellaneous Control Register | Bit Field | 0 | | | | | | | DFLASHEN |
| | | Type | r | | | | | | | rwh |
| RMAP = 0, PAGE 3 | | | | | | | | | | |
| $B3_H$ | **XADDRH** **Reset: $F0_H$** On-chip XRAM Address Higher Order | Bit Field | ADDRH | | | | | | | |
| | | Type | rw | | | | | | | |
| $B4_H$ | **IRCON3** **Reset: $00_H$** Interrupt Request Register 3 | Bit Field | 0 | | CANSRC5 | CCU6SR1 | 0 | | CANSRC4 | CCU6SR0 |
| | | Type | r | | rwh | rwh | r | | rwh | rwh |
| $B5_H$ | **IRCON4** **Reset: $00_H$** Interrupt Request Register 4 | Bit Field | 0 | | CANSRC7 | CCU6SR3 | 0 | | CANSRC6 | CCU6SR2 |
| | | Type | r | | rwh | rwh | r | | rwh | rwh |
| $B7_H$ | **MODPISEL1** **Reset: $00_H$** Peripheral Input Select Register 1 | Bit Field | EXINT6IS | 0 | | UR1RIS | | T21EXIS | JTAGTDIS1 | JTAGTCKS1 |
| | | Type | rw | r | | rw | | rw | rw | rw |
| $BA_H$ | **MODPISEL2** **Reset: $00_H$** Peripheral Input Select Register 2 | Bit Field | 0 | | | | T21IS | T2IS | T1IS | T0IS |
| | | Type | r | | | | rw | rw | rw | rw |
| $BB_H$ | **PMCON2** **Reset: $00_H$** Power Mode Control Register 2 | Bit Field | 0 | | | | | | UART1_DIS | T21_DIS |
| | | Type | r | | | | | | rw | rw |
| $BD_H$ | **MODSUSP** **Reset: $01_H$** Module Suspend Control Register | Bit Field | 0 | | | T21SUSP | T2SUSP | T13SUSP | T12SUSP | WDTSUSP |
| | | Type | r | | | rw | rw | rw | rw | rw |

### 3.2.4.5 WDT Registers

The WDT SFRs can be accessed in the mapped memory area (RMAP = 1).

**Table 8 WDT Register Overview**

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| RMAP = 1 | | | | | | | | | | |
| $BB_H$ | **WDTCON** **Reset: $00_H$** Watchdog Timer Control Register | Bit Field | 0 | | WINBEN | WDTPR | 0 | WDTEN | WDTRS | WDTIN |
| | | Type | r | | rw | rh | r | rw | rwh | rw |
| $BC_H$ | **WDTREL** **Reset: $00_H$** Watchdog Timer Reload Register | Bit Field | WDTREL | | | | | | | |
| | | Type | rw | | | | | | | |
| $BD_H$ | **WDTWINB** **Reset: $00_H$** Watchdog Window-Boundary Count Register | Bit Field | WDTWINB | | | | | | | |
| | | Type | rw | | | | | | | |

## 3.4 Interrupt System

The XC800 Core supports one non-maskable interrupt (NMI) and 14 maskable interrupt requests. In addition to the standard interrupt functions supported by the core, e.g., configurable interrupt priority and interrupt masking, the SAA-XC886 interrupt system provides extended interrupt support capabilities such as the mapping of each interrupt vector to several interrupt sources to increase the number of interrupt sources supported, and additional status registers for detecting and determining the interrupt source.

### 3.4.1 Interrupt Source

**Figure 12** to **Figure 16** give a general overview of the interrupt sources and nodes, and their corresponding control and status flags.

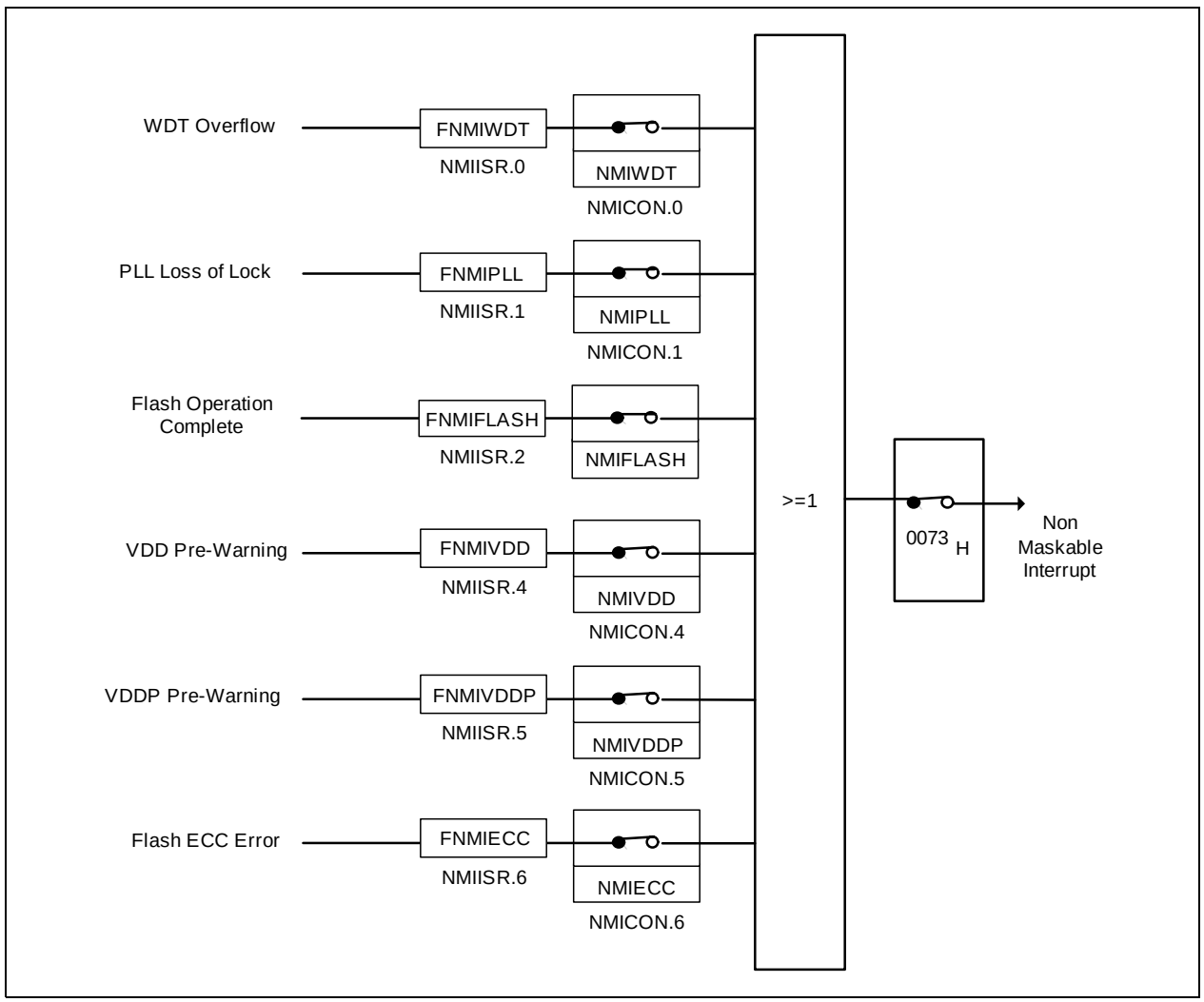



**Figure 12 Non-Maskable Interrupt Request Sources**

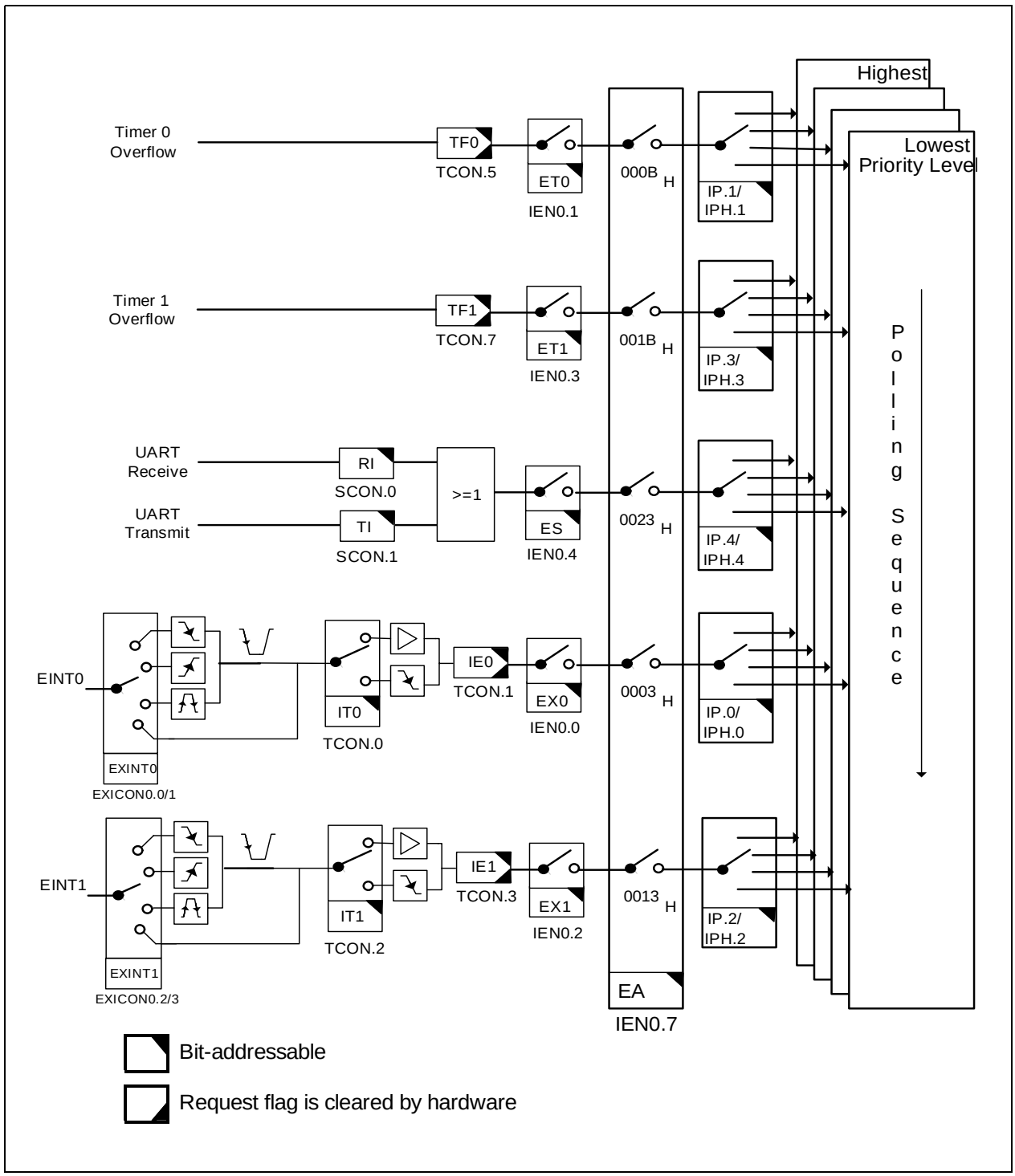



**Figure 13 Interrupt Request Sources (Part 1)**

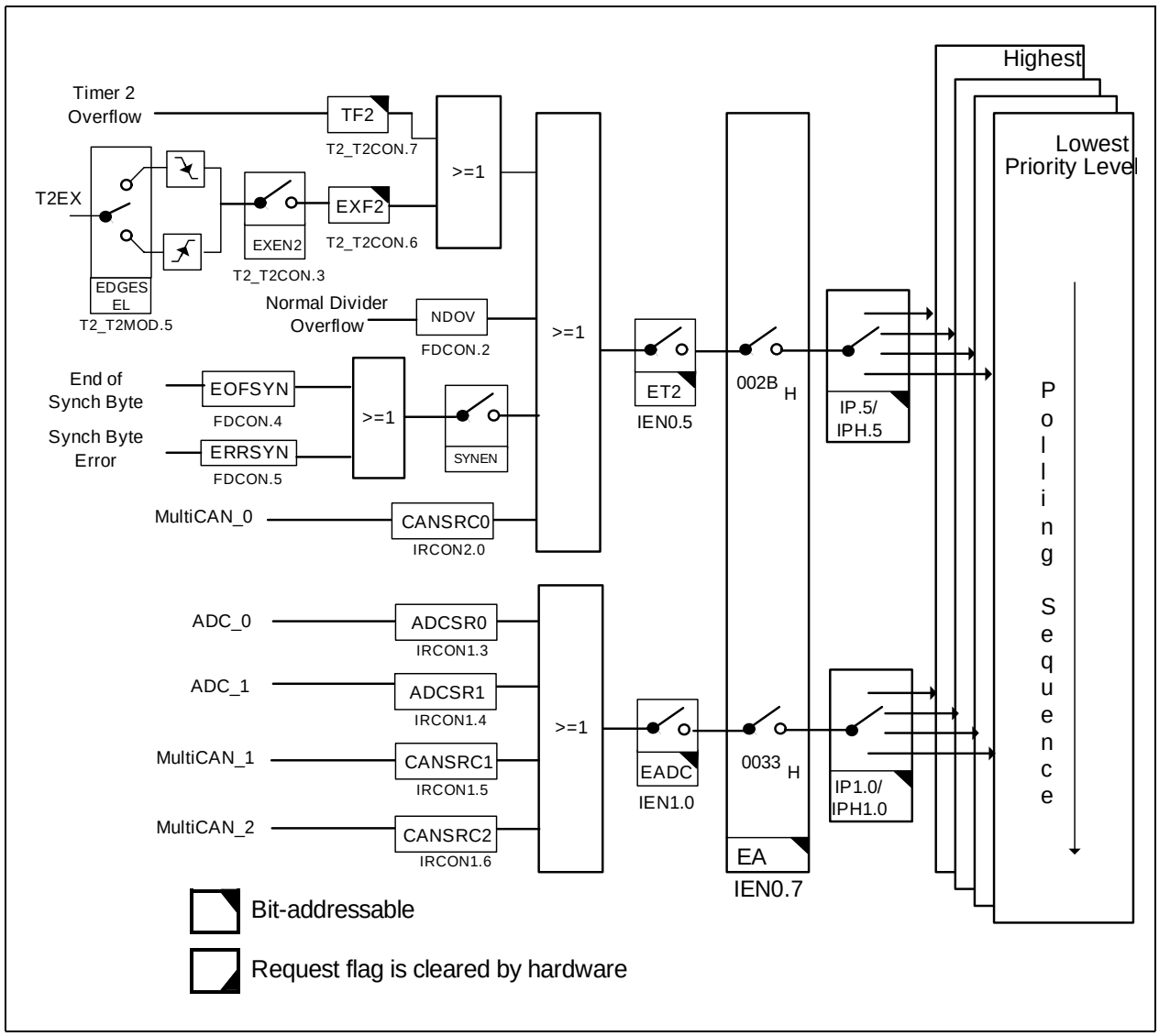



**Figure 14 Interrupt Request Sources (Part 2)**

### 3.4.2 Interrupt Source and Vector

Each interrupt event source has an associated interrupt vector address for the interrupt node it belongs to. This vector is accessed to service the corresponding interrupt node request. The interrupt service of each interrupt source can be individually enabled or disabled via an enable bit. The assignment of the SAA-XC886 interrupt sources to the interrupt vector address and the corresponding interrupt node enable bits are summarized in **Table 19**.

**Table 19 Interrupt Vector Addresses**

| Interrupt Source | Vector Address | Assignment for SAA-XC886 | Enable Bit | SFR |
|---|---|---|---|---|
| NMI | $0073_H$ | Watchdog Timer NMI | NMIWDT | NMICON |
| | | PLL NMI | NMIPLL | |
| | | Flash NMI | NMIFLASH | |
| | | VDDC Prewarning NMI | NMIVDD | |
| | | VDDP Prewarning NMI | NMIVDDP | |
| | | Flash ECC NMI | NMIECC | |
| XINTR0 | $0003_H$ | External Interrupt 0 | EX0 | IEN0 |
| XINTR1 | $000B_H$ | Timer 0 | ET0 | |
| XINTR2 | $0013_H$ | External Interrupt 1 | EX1 | |
| XINTR3 | $001B_H$ | Timer 1 | ET1 | |
| XINTR4 | $0023_H$ | UART | ES | |
| XINTR5 | $002B_H$ | T2 | ET2 | |
| | | UART Fractional Divider (Normal Divider Overflow) | | |
| | | MultiCAN Node 0 | | |
| | | LIN | | |

**Figure 18** shows the structure of a bidirectional port pin.

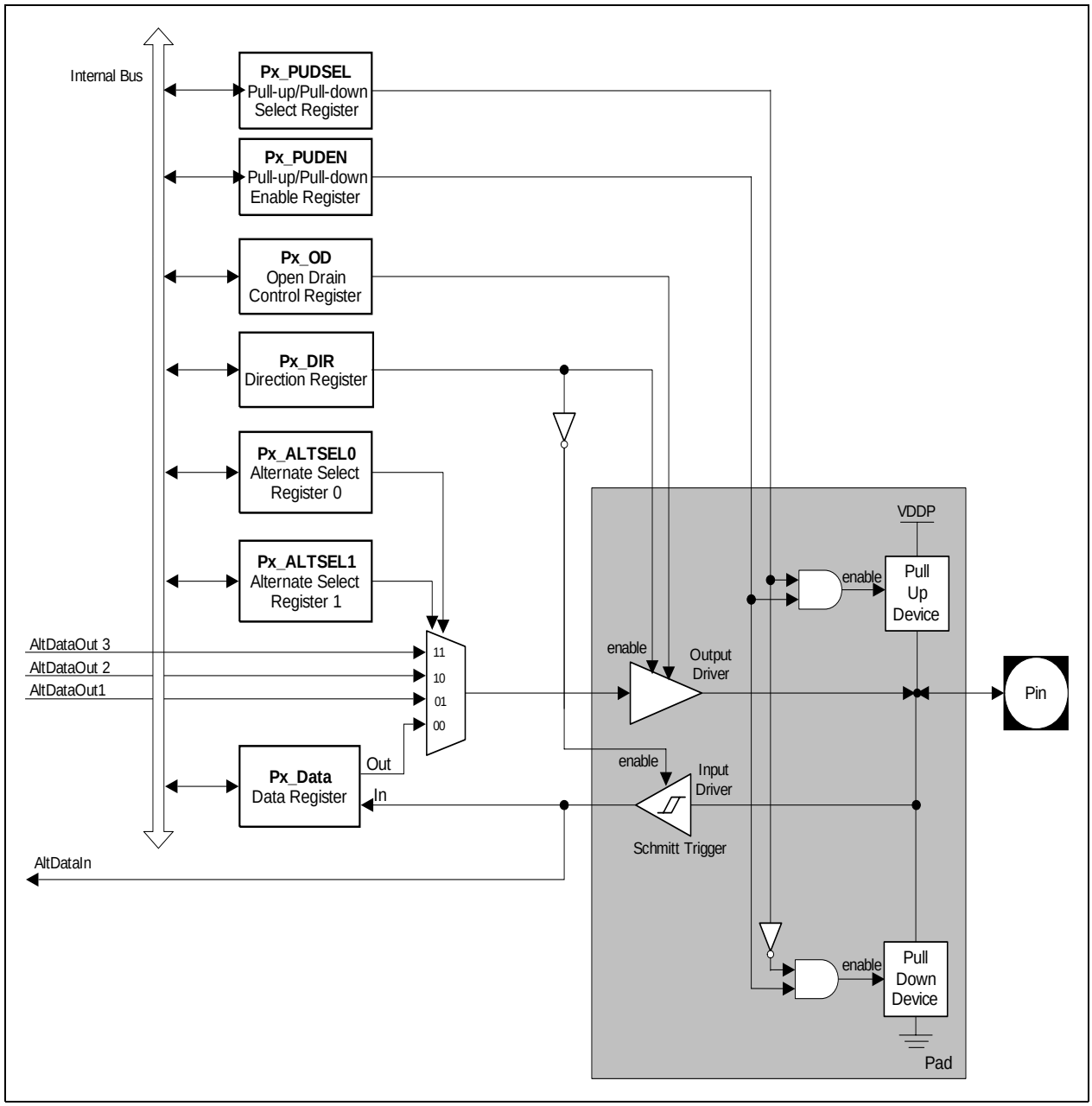



**Figure 18 General Structure of Bidirectional Port**

**Figure 19** shows the structure of an input-only port pin.

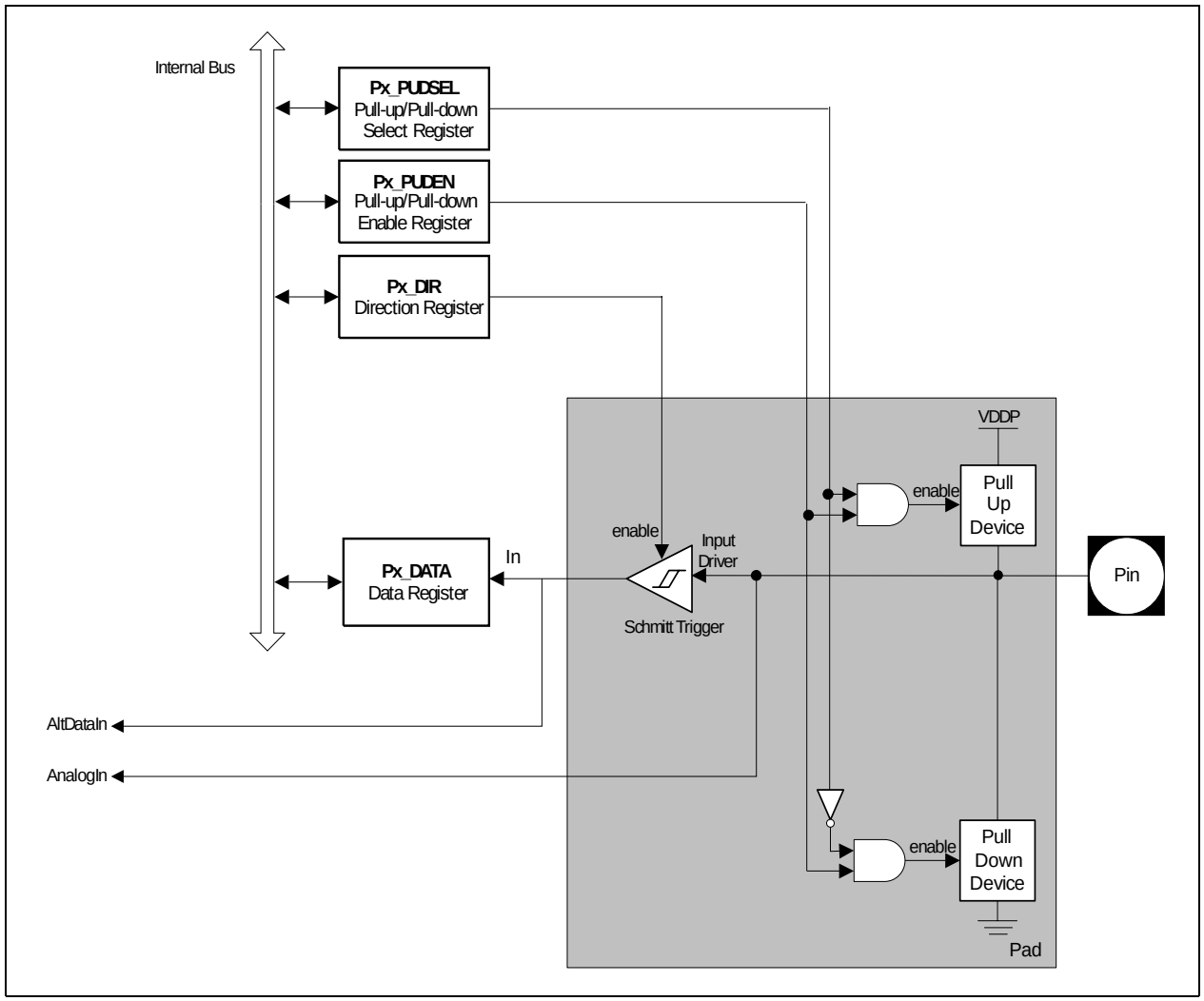



**Figure 19 General Structure of Input Port**

### PLL Mode

The system clock is derived from the oscillator clock, multiplied by the N factor, and divided by the P and K factors. Both VCO bypass and PLL bypass must be inactive for this PLL mode. The PLL mode is used during normal system operation.

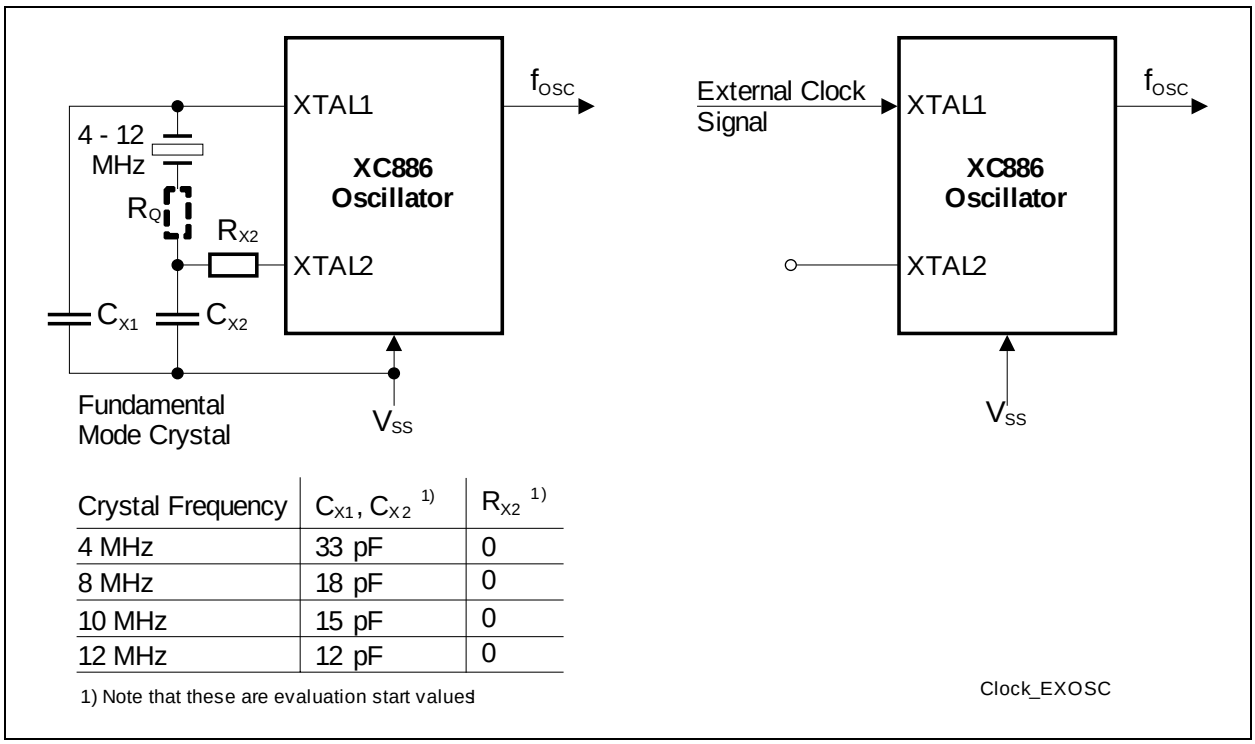
$$f_{SYS} = f_{OSC} \times \frac{N}{P \times K} \quad (3.3)$$

### System Frequency Selection

For the SAA-XC886, the value of P is fixed to 1. In order to obtain the required fsys, the value of N and K can be selected by bits NDIV and KDIV respectively for different oscillator inputs. The output frequency must always be configured for 96 MHz. **Table 23** provides examples on how $f_{sys}$ = 96 MHz can be obtained for the different oscillator sources.

**Table 23 System frequency ($f_{sys}$ = 96 MHz)**

| Oscillator | Fosc | N | P | K | Fsys |
|---|---|---|---|---|---|
| On-chip | 9.6 MHz | 20 | 1 | 2 | 96 MHz |
| External | 8 MHz | 24 | 1 | 2 | 96 MHz |
| | 6 MHz | 32 | 1 | 2 | 96 MHz |
| | 4 MHz | 48 | 1 | 2 | 96 MHz |




| Crystal Frequency | $C_{X1}$, $C_{X2}$ 1) | $R_{X2}$ 1) |
|---|---|---|
| 4 MHz | 33 pF | 0 |
| 8 MHz | 18 pF | 0 |
| 10 MHz | 15 pF | 0 |
| 12 MHz | 12 pF | 0 |

1) Note that these are evaluation start values

**Figure 24 External Oscillator Circuitry**

*Note: For crystal operation, it is strongly recommended to measure the negative resistance in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the minimum and maximum values of the negative resistance specified by the crystal supplier.*

For power saving purposes, the clocks may be disabled or slowed down according to **Table 25**.

**Table 25 System frequency ($f_{sys}$ = 96 MHz)**

| Power Saving Mode | Action |
|---|---|
| Idle | Clock to the CPU is disabled. |
| Slow-down | Clocks to the CPU and all the peripherals are divided by a common programmable factor defined by bit field CMCON.CLKREL. |
| Power-down | Oscillator and PLL are switched off. |

## 3.21 Analog-to-Digital Converter

The SAA-XC886 includes a high-performance 10-bit Analog-to-Digital Converter (ADC) with eight multiplexed analog input channels. The ADC uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC are available at Port 2.

**Features**

- Successive approximation
- 8-bit or 10-bit resolution
  (TUE of ± 1 LSB and ± 2 LSB, respectively)
- Eight analog channels
- Four independent result registers
- Result data protection for slow CPU access
  (wait-for-read mode)
- Single conversion mode
- Autoscan functionality
- Limit checking for conversion results
- Data reduction filter
  (accumulation of up to 2 conversion results)
- Two independent conversion request sources with programmable priority
- Selectable conversion request trigger
- Flexible interrupt generation with configurable service nodes
- Programmable sample time
- Programmable clock divider
- Cancel/restart feature for running conversions
- Integrated sample and hold circuitry
- Compensation of offset errors
- Low power modes

### 3.21.1 ADC Clocking Scheme

A common module clock $f_{ADC}$ generates the various clock signals used by the analog and digital parts of the ADC module:

- $f_{ADCA}$ is input clock for the analog part.
- $f_{ADCI}$ is internal clock for the analog part (defines the time base for conversion length and the sample time). This clock is generated internally in the analog part, based on the input clock $f_{ADCA}$ to generate a correct duty cycle for the analog components.
- $f_{ADCD}$ is input clock for the digital part.

The internal clock for the analog part $f_{ADCI}$ is limited to a maximum frequency of 10 MHz. Therefore, the ADC clock prescaler must be programmed to a value that ensures $f_{ADCI}$ does not exceed 10 MHz. The prescaler ratio is selected by bit field CTC in register

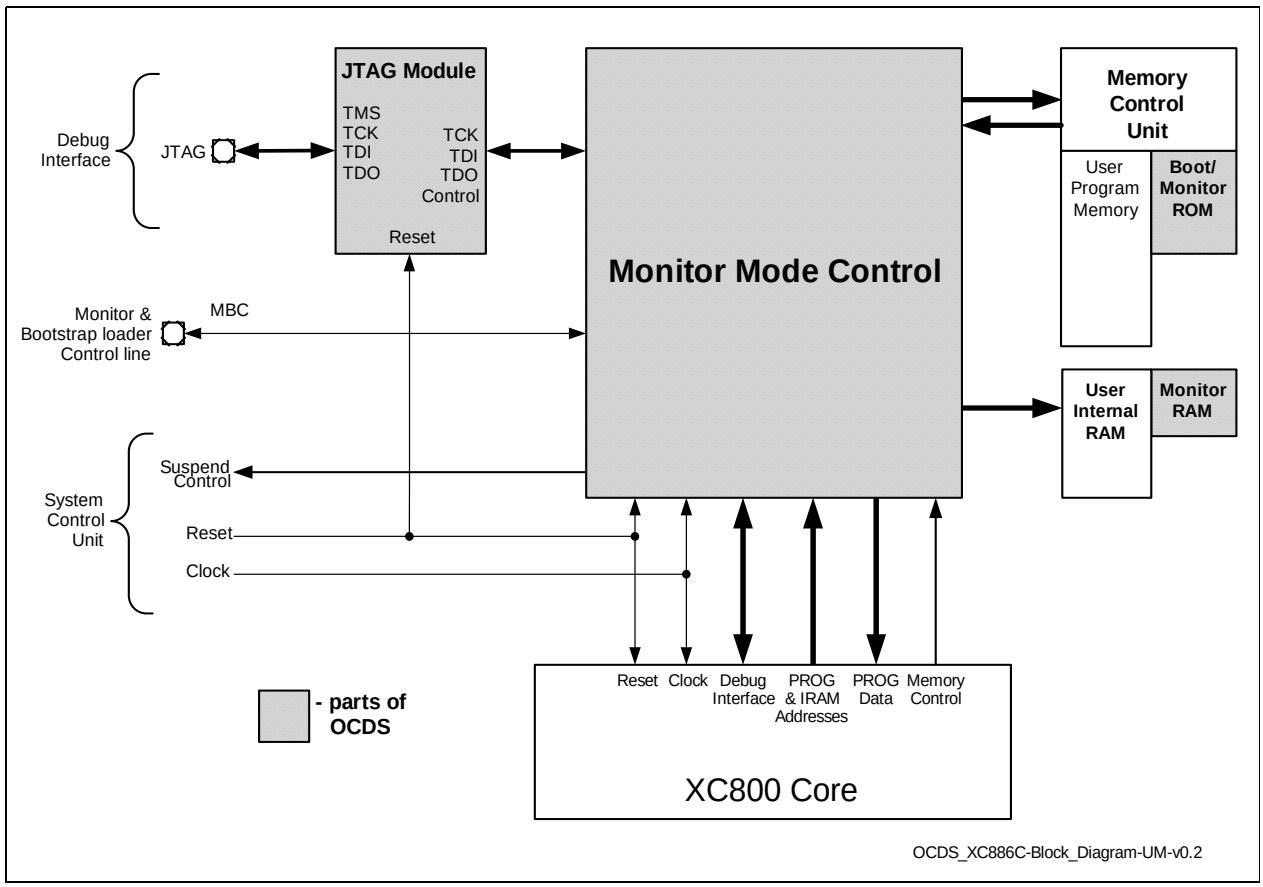



**Figure 36 OCDS Block Diagram**

### 3.22.1 JTAG ID Register

This is a read-only register located inside the JTAG module, and is used to recognize the device(s) connected to the JTAG interface. Its content is shifted out when INSTRUCTION register contains the IDCODE command (opcode $04_H$), and the same is also true immediately after reset.

The JTAG ID register contents for the SAA-XC886 Flash devices are given in **Table 34**.

**Table 34 JTAG ID Summary**

| Device Type | Device Name | JTAG ID |
|---|---|---|
| Flash | SAA-XC886*-8FF | $1012\ 0083_H$ |
| | SAA-XC886*-6FF | $1012\ 5083_H$ |

*Note: The asterisk (*) above denotes all possible device configurations.*

### 4.2.4 Power Supply Current

**Table 41** and **Table 42** provide the characteristics of the power supply current in the SAA-XC886.

**Table 41 Power Supply Current Parameters (Operating Conditions apply; $V_{DDP}$ = 5V range)**

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|---|---|---|---|---|
| | | typ.[1] | max.[2] | | |
| **$V_{DDP}$ = 5V Range** | | | | | |
| Active Mode | $I_{DDP}$ | 26.9 | 31.9 | mA | [3] |
| Idle Mode | $I_{DDP}$ | 20.3 | 24.4 | mA | [4] |
| Active Mode with slow-down enabled | $I_{DDP}$ | 13.7 | 17.0 | mA | [5] |
| Idle Mode with slow-down enabled | $I_{DDP}$ | 11.4 | 14.2 | mA | [6] |

1) The typical $I_{DDP}$ values are periodically measured at $T_A$ = + 25 °C and $V_{DDP}$ = 5.0 V.

**2)** The maximum $I_{DDP}$ values are measured under worst case conditions ($T_A$ = + 140 °C and $V_{DDP}$ = 5.5 V).

3) $I_{DDP}$ (active mode) is measured with: CPU clock and input clock to all peripherals running at 24 MHz(set by on-chip oscillator of 9.6 MHz and NDIV in PLL_CON to $1001_B$), $\overline{\text{RESET}}$ = $V_{DDP}$, no load on ports.

4) $I_{DDP}$ (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 24 MHz, $\overline{\text{RESET}}$ = $V_{DDP}$, no load on ports.

5) $I_{DDP}$ (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 8 MHz by setting CLKREL in CMCON to $0110_B$, $\overline{\text{RESET}}$ = $V_{DDP}$, no load on ports.

6) $I_{DDP}$ (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 8 MHz by setting CLKREL in CMCON to $0110_B$, $\overline{\text{RESET}}$ = $V_{DDP}$, no load on ports.

### 4.3.2 Output Rise/Fall Times

**Table 43** provides the characteristics of the output rise/fall times in the SAA-XC886.

**Table 43 Output Rise/Fall Times Parameters (Operating Conditions apply)**

| Parameter | Symbol | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|
| | | min. | max. | | |
| **$V_{DDP}$ = 5V Range** | | | | | |
| Rise/fall times | $t_R$, $t_F$ | – | 10 | ns | 20 pF.[1)2)3)] |

1) Rise/Fall time measurements are taken with 10% - 90% of pad supply.

2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

3) Additional rise/fall time valid for $C_L$ = 20pF - 100pF @ 0.125 ns/pF.

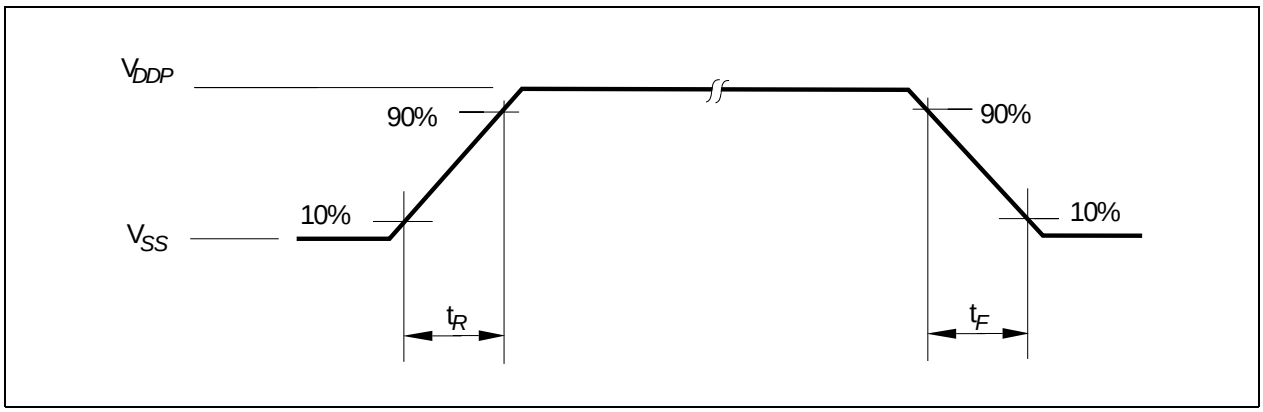



**Figure 42 Rise/Fall Times Parameters**

### 4.3.3 Power-on Reset and PLL Timing

**Table 47** provides the characteristics of the power-on reset and PLL timing in the SAA-XC886.

**Table 44 Power-On Reset and PLL Timing (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| Pad operating voltage | $V_{PAD}$ | CC | 2.3 | – | – | V | 1) |
| On-Chip Oscillator start-up time | $t_{OSCST}$ | CC | – | – | 500 | ns | 1) |
| Flash initialization time | $t_{FINIT}$ | CC | – | 160 | – | µs | 1) |
| $\overline{\text{RESET}}$ hold time | $t_{RST}$ | SR | – | 500 | – | µs | $V_{DDP}$ rise time (10% – 90%) ≤ 500µs1)2) |
| PLL lock-in in time | $t_{LOCK}$ | CC | – | – | 200 | µs | 1) |
| PLL accumulated jitter | $D_P$ | | – | – | 0.7 | ns | 1)3) |

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

2) $\overline{\text{RESET}}$ signal has to be active (low) until $V_{DDC}$ has reached 90% of its maximum value (typ. 2.5 V).

3) PLL lock at 96 MHz using a 4 MHz external oscillator. The PLL Divider settings are K = 2, N = 48 and P = 1.

**Table 48 JTAG Timing (Operating Conditions apply; CL = 50 pF)** (cont'd)

| Parameter | Symbol | | Limits | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | min | max | | |
| TDO high impedance to valid output from TCK | $t_4$ | CC | - | 35 | ns | 1) |
| TDO valid output to high impedance from TCK | $t_5$ | CC | - | 27 | ns | 1) |

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

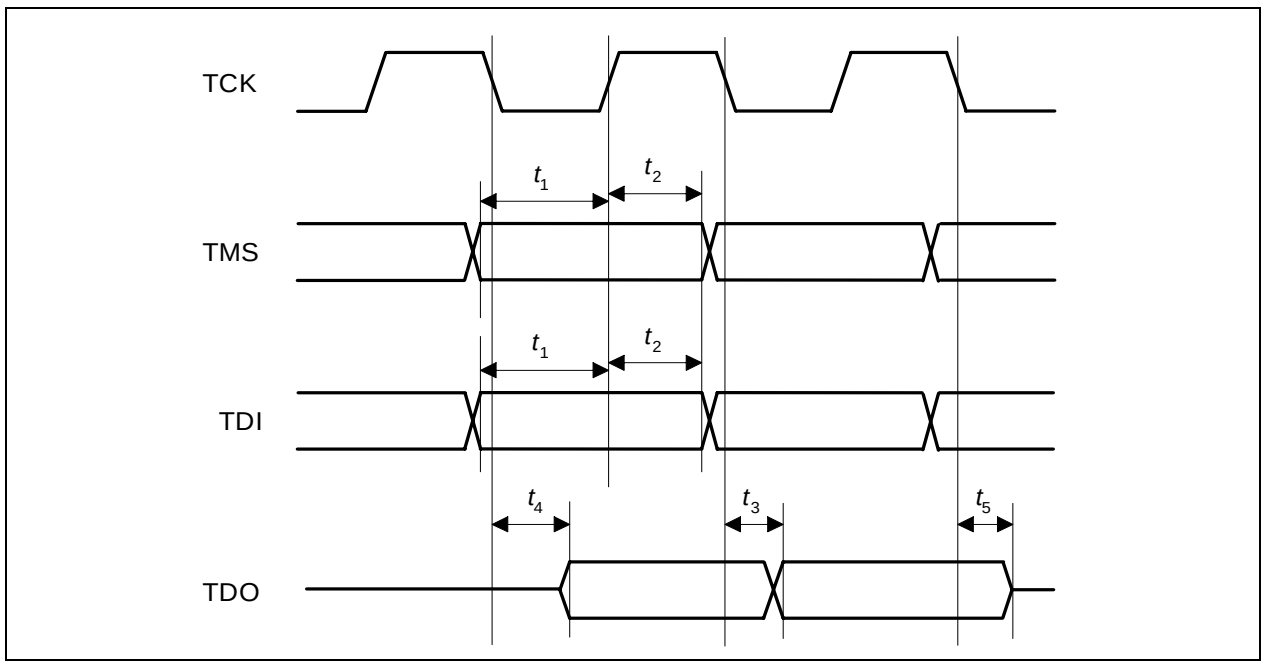



**Figure 46 JTAG Timing**