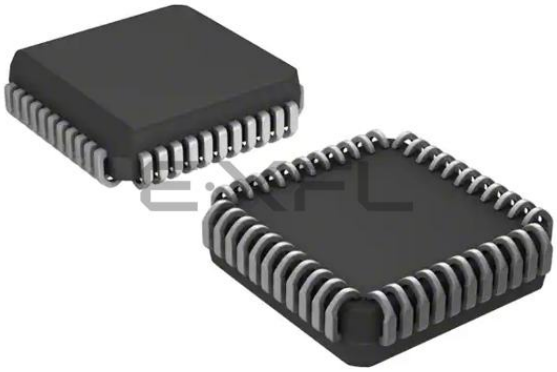

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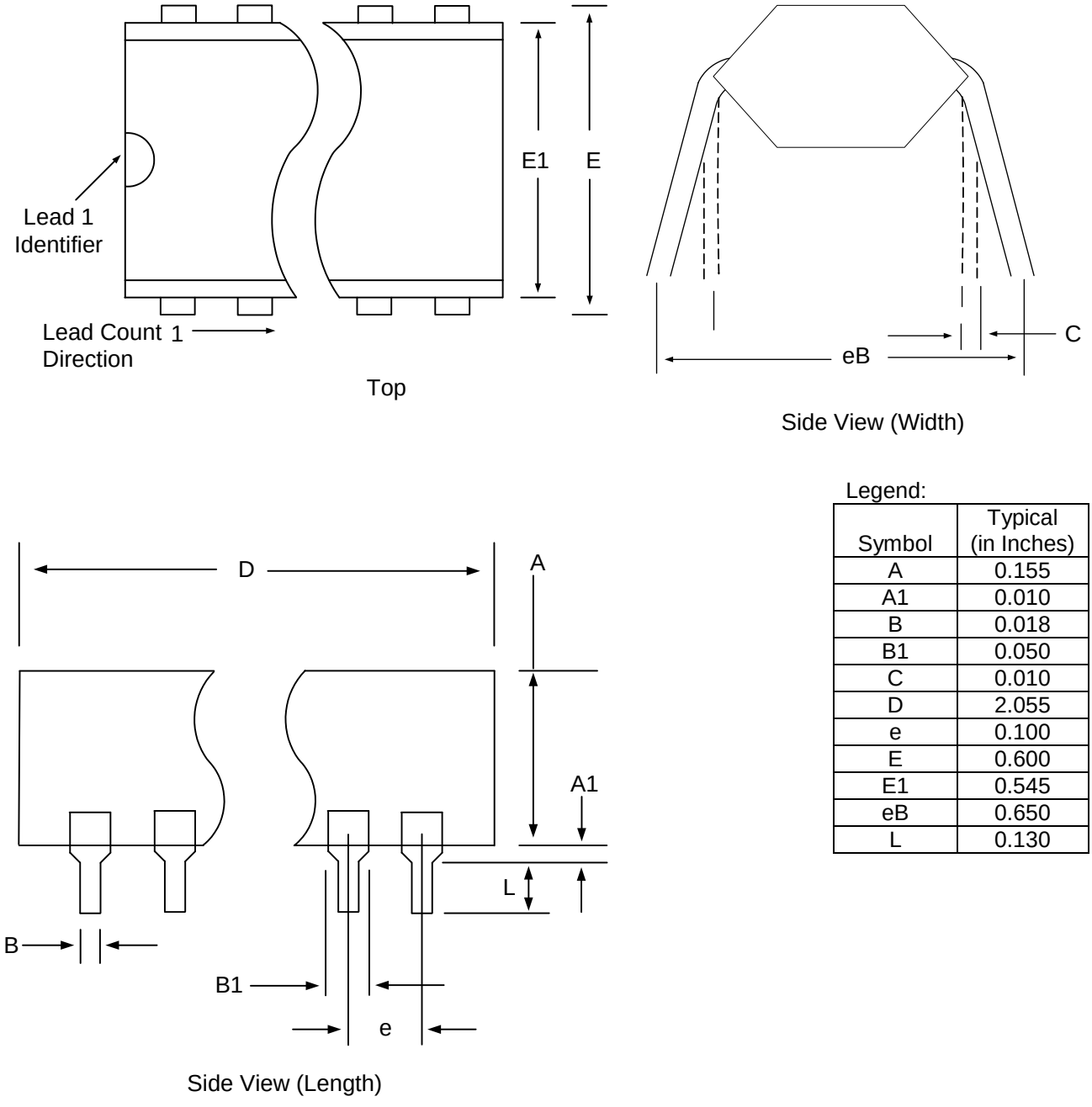
Applications	Communications Controller
Core Processor	8-Bit
Program Memory Type	External Program Memory
Controller Series	-
RAM Size	192 x 8
Interface	Serial Interface Unit - SDLC/HDLC
Number of I/O	32
Voltage - Supply	4.5V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ia8x44plc44ir3

TABLE OF CONTENTS

2.2 PDIP Physical Dimensions

The physical dimensions for the 40 PDIP are as shown in Figure 2.



Legend:

Symbol	Typical (in Inches)
A	0.155
A1	0.010
B	0.018
B1	0.050
C	0.010
D	2.055
e	0.100
E	0.600
E1	0.545
eB	0.650
L	0.130

Figure 2. PDIP Physical Package Dimensions

Table 2. IA8044 and IA8344 44-Pin PLCC Pin Listing

Pin	Name
1	N.C.
2	P1.0
3	P1.1
4	P1.2
5	P1.3
6	P1.4
7	P1.5
8	P1.6
9	P1.7
10	RST/VPD
11	P3.0

Pin	Name
12	N.C.
13	P3.1
14	P3.2
15	P3.3
16	P3.4
17	P3.5
18	P3.6
19	P3.7
20	XTAL2
21	XTAL1
22	VSS

Pin	Name
23	N.C.
24	P2.0
25	P2.1
26	P2.2
27	P2.3
28	P2.4
29	P2.5
30	P2.6
31	P2.7
32	PSEN
33	ALE

Pin	Name
34	N.C.
35	EA
36	P0.7
37	P0.6
38	P0.5
39	P0.4
40	P0.3
41	P0.2
42	P0.1
43	P0.0
44	VCC

3. Maximum Ratings and DC Characteristics

The IA8044/IA8344 absolute maximum ratings and DC characteristics are provided in Tables 3 and 4, respectively.

Table 3. IA8044 and IA8344 Absolute Maximum Ratings

Parameter	Rating
Ambient temperature under bias	−40°C to +85°C
Storage temperature	−40°C to +150°C
Power supply (V_{DD})	−0.3 to +6VDC
Voltage on any pin to VSS	−0.3 to (V_{DD} +0.3)[a]
Power dissipation	2W

[a]This device does not contain EPROM or its related programming circuitry. Therefore, this limit must be adhered to especially for input pin EA, which is used as the programming voltage pin in the Intel device. Exceeding the listed maximum voltage will cause damage to the device.

Table 4. IA8044 and IA8344 DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VIL	Input Low Voltage	–	–	0.8	V
VIH	Input High Voltage	2.0	–	–	V
VOL	Output Low Voltage (IOL= 4mA)	–	–	0.4	V
VOH	Output High Voltage (IOH= 4mA)	3.5	–	–	V
RPU	Pull-Up Resistance (Ports 1, 2, 3)	–	50	–	KW
RPD	Pull-Down Resistance (RST)	–	50	–	KW
IIL	Input Low Current (Ports 1, 2, 3)	−200	–	1	µA
IIL1	Input Low Current (PO, EA)	−1	–	1	µA
IIH	Input High Current (RST)	−1	–	200	µA
IIH1	Input High Current (PO, EA)	−1	–	1	µA
IOZ	Tri-state Leakage Current (Port 0)	−10	–	10	µA
ICC	Power Supply Current (@ 12 MHz)	–	–	50	mA
CIO	Pin Capacitance	–	4	–	pF

4. Functional Description

4.1 Functional Block Diagram

A functional block diagram of the IA8044 and IA8344 is shown in Figure 5. Descriptions of the functional modules are provided in the following subsections.

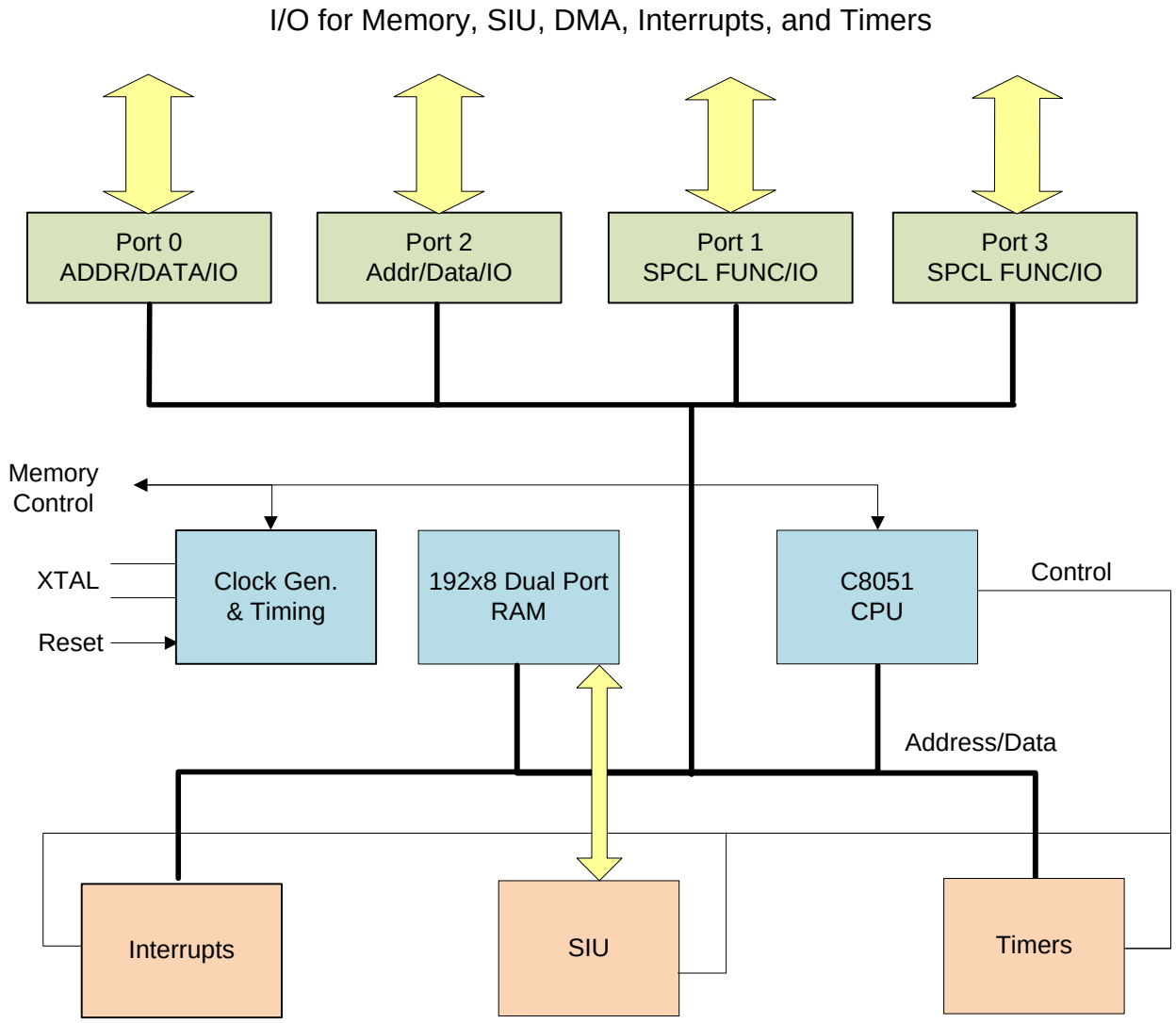


Figure 5. Functional Block Diagram

4.3.4 Bit Addressable Memory

Both the internal RAM and the SFRs have locations that are bit addressable in addition to the byte addressable locations (see Tables 7 and 8).

Table 7. SFR Bit Addressable Locations

Byte Address	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]	Register
F0h	F7h	F6h	F5h	F4h	F3h	F2h	F1h	F0h	B
E0h	E7h	E6h	E5h	E4h	E3h	E2h	E1h	E0h	ACC
D8h	DFh	DEh	DDh	DCh	DBh	DAh	D9h	D8h	NSNR
D0h	D7h	D6h	D5h	D4h	D3h	D2h	D1h	D0h	PSW
C8h	CFh	CEh	CDh	CCh	CBh	CAh	C9h	C8h	STS
B8h	–	–	–	BCh	BBh	BAh	B9h	B8h	IP
B0h	B7h	B6h	B5h	B4h	B3h	B2h	B1h	B0h	P3
A8h	AFh	–	–	ACh	ABh	AAh	A9h	A8h	IE
A0h	A7h	A6h	A5h	A4h	A3h	A2h	A1h	A0h	P2
90h	97h	96h	95h	94h	93h	92h	91h	90h	P1
88h	8Fh	8Eh	8Dh	8Ch	8Bh	8Ah	89h	88h	TCON
80h	87h	86h	85h	84h	83h	82h	81h	80h	P0

Table 8. Internal RAM Bit Addressable Locations

Byte Address	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
30h-BFh	Upper Internal RAM Locations							
2Fh	7Fh	7Eh	7Dh	7Ch	7Bh	7Ah	79h	78h
2Eh	77h	76h	75h	74h	73h	72h	71h	70h
2Dh	6Fh	6Eh	6Dh	6Ch	6Bh	6Ah	69h	68h
2Ch	67h	66h	65h	64h	63h	62h	61h	60h
2Bh	5Fh	5Eh	5Dh	5Ch	5Bh	5Ah	59h	58h
2Ah	57h	56h	55h	54h	53h	52h	51h	50h
29h	4Fh	4Eh	4Dh	4Ch	4Bh	4Ah	49h	48h
28h	47h	46h	45h	44h	43h	42h	41h	40h
27h	3Fh	3Eh	3Dh	3Ch	3Bh	3Ah	39h	38h
26h	37h	36h	35h	34h	33h	32h	31h	30h
25h	2Fh	2Eh	2Dh	2Ch	2Bh	2Ah	29h	28h
24h	27h	26h	25h	24h	23h	22h	21h	20h
23h	1Fh	1Eh	1Dh	1Ch	1Bh	1Ah	19h	18h
22h	17h	16h	15h	14h	13h	12h	11h	10h
21h	0Fh	0Eh	0Dh	0Ch	0Bh	0Ah	09h	08h
20h	07h	06h	05h	04h	03h	02h	01h	00h
18h-1Fh	Register Bank 3							
10h-17h	Register Bank 2							
08h-0Fh	Register Bank 1							
00h-07h	Register Bank 0							

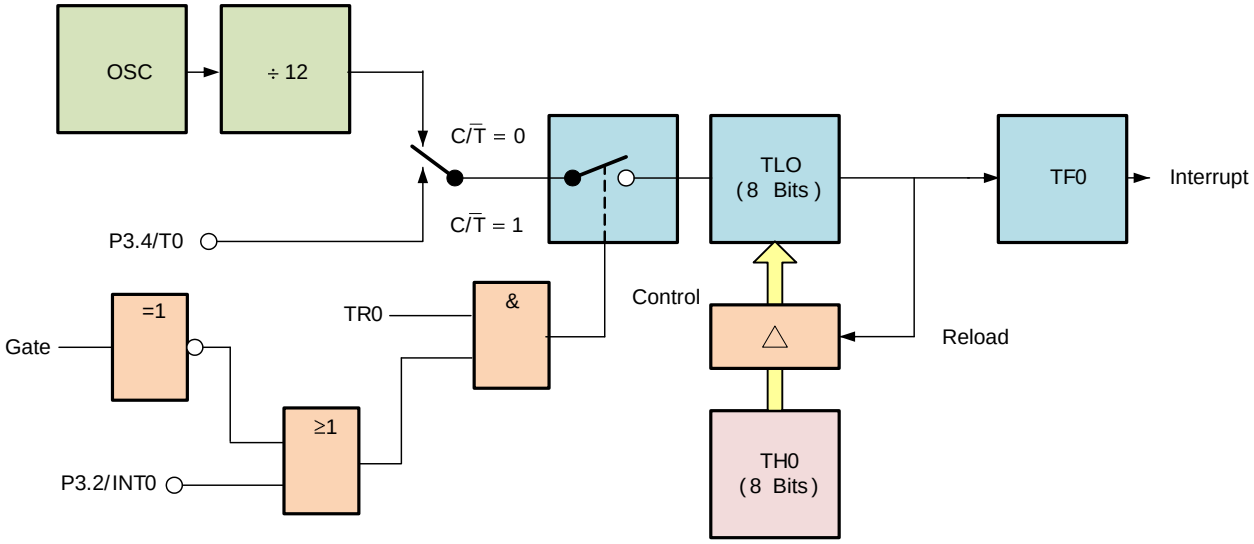


Figure 9. Timer 0 Mode 2

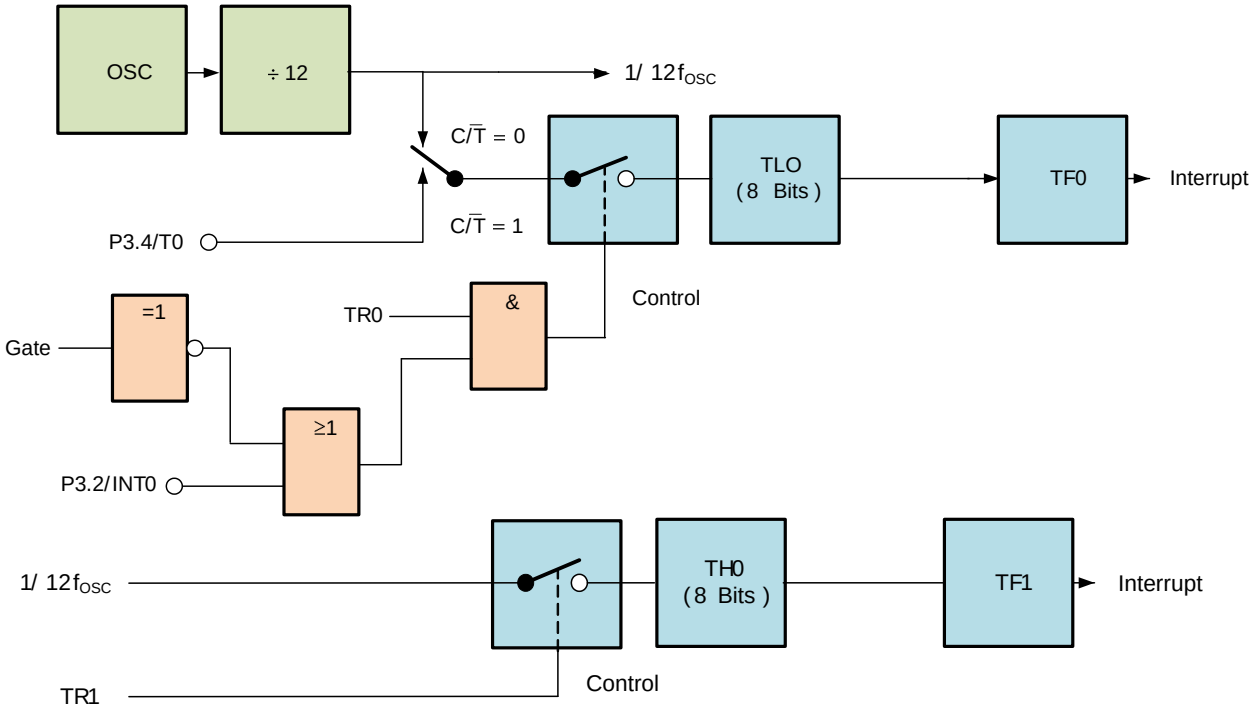


Figure 10. Timer 0 Mode 3

- Bit [3]—PT1 → (IP.3) Timer 1 interrupt priority bit
- Bit [2]—PX1 → (IP.2) External Interrupt 1 interrupt priority bit
- Bit [1]—PT0 → (IP.1) Timer 0 interrupt priority bit
- Bit [0]—PX0 → (IP.0) External Interrupt 0 interrupt priority bit

4.9.7 Interrupt Enable Register (IE)

Table 30 presents the interrupt enable register, which contains the global interrupt enable bit and individual interrupt enable bits. Setting a bit enables the corresponding interrupt.

Table 30. Interrupt Enable Register

7	6	5	4	3	2	1	0
EA	–	–	ES	ET1	EX1	ET0	EX0

- Bit [7]—EA → (PCON.7) Enable all interrupts bit
- Bit [6]—(PCON.6)
- Bit [5]—(PCON.5)
- Bit [4]—ES → (PCON.4) SIU interrupt enable bit
- Bit [3]—ET1 → (PCON.3) Timer 1 interrupt enable bit
- Bit [2]—EX1→ (PCON.2) External Interrupt 1 interrupt enable bit
- Bit [1]—ET0→ (PCON.1) Timer 0 interrupt enable bit
- Bit [0]—EX0→ (PCON.7) External Interrupt 0 interrupt enable bit

4.10 SIU—Serial Interface Unit

The SIU is a serial interface customized to support SDLC/HDLC protocol. As such, it supports Zero Bit insertion/deletion, flags automatic access recognition and a 16-bit CRC. The SIU has two modes of operation AUTO and FLEXIBLE. The AUTO mode uses a subset of the SDLC protocol implemented in hardware. This frees the CPU from having to respond to every frame but limits the frame types. In the FLEXIBLE mode every frame is under CPU control and therefore more options are available. The SIU is controlled by and communicates to the CPU by using several SFRs. Data transmitted by or received by the SIU is stored in the 192-byte internal RAM in blocks referred to as the transmit and receive buffers. The SIU can support operation in one of

three serial data link configurations, 1) half-duplex, point-to-point, 2) half-duplex, multipoint, or 3) loop mode.

4.10.1 SIU Special Function Registers

The CPU controls the SIU and receives status from the SIU via 11 SFRs. The Serial Interface Unit Control Registers are detailed in the sections that follow.

4.10.2 Serial Mode Register (SMD)

Table 31 presents the serial mode register, which sets the operational mode of the SIU. The CPU can read and write SMD. The SIU can read SMD. To prevent conflicts between CPU and SIU, accesses to SMD the CPU should write SMD only when RTS and RBE bits in the STS register are both zero. SMD is normally only accessed during initialization. This register is byte addressable. Table 32 presents the serial mode select clock mode bits.

Table 31. Serial Mode Register

7	6	5	4	3	2	1	0
SCM2	SCM1	SCM0	NRZI	LOOP	PFS	NB	NFCS

- Bit [7]—SCM2 → (SMD.7) Select clock mode—Bit [2].
- Bit [6]—SCM1 → (SMD.6) Select clock mode—Bit [1].
- Bit [5]—SCM0 → (SMD.5) Select clock mode—Bit [0].
- Bit [4]—NRZI → (SMD.4) When set selects NRZI encoding otherwise NRZ.
- Bit [3]—LOOP → (SMD.3) When set, selects loop configuration, else point-to-point mode.
- Bit [2]—PFS → (SMD.2) Pre-frame sync mode. When set, causes two bytes to be transmitted before the first flag of the frame for DPLL synchronization. If NRZI is set, 00H is transmitted, otherwise 55H. This ensures that 16 transitions are sent before the opening flag.
- Bit [1]—NB → (SMD.1) Non-buffered mode. No control field contained in SDLC frame.
- Bit [0]—NFCS → (SMD.0) When set, selects No FCS field contained in the SDLC frame.

4.10.5 Station Address Register (STAD)

Table 35 presents the Station Address Register, which contains the station address (node address) of the chip. The CPU can read or write STAD but should access STAD only when RTS = 0 and RBE = 0. Normally STAD is accessed only during initialization. STAD is byte addressable.

Table 35. Station Address Register

7	6	5	4	3	2	1	0
STAD.7	STAD.6	STAD.5	STAD.4	STAD.3	STAD.2	STAD.1	STAD.0

4.10.6 Transmit Buffer Start Address Register (TBS)

Table 36 presents the Transmit Buffer Start Address Register, which contains the address in internal RAM where the frame to be transmitted (starting with the I-field) is stored. The CPU should access TBS only when the SIU is not transmitting a frame, TBF = 0. TBS is byte addressable.

Table 36. Transmit Buffer Start Address Register

7	6	5	4	3	2	1	0
TBS.7	TBS.6	TBS.5	TBS.4	TBS.3	TBS.2	TBS.1	TBS.0

4.10.7 Transmit Buffer Length Register (TBL)

Table 37 presents the Transmit Buffer Length Register, which contains the length, in number of bytes, of the I-field to be transmitted. TBL = 0 is valid (no I-field). The CPU should access TBL only when the SIU is not transmitting a frame, TBF = 0. The transmit buffer will not wrap around after address 191 (BFH). A buffer end is automatically generated when address 191 is reached. TBL is byte addressable.

Table 37. Transmit Buffer Length Register

7	6	5	4	3	2	1	0
TBL.7	TBL.6	TBL.5	TBL.4	TBL.3	TBL.2	TBL.1	TBL.0

4.10.8 Transmit Control Byte Register (TCB)

Table 38 presents the Transmit Control Byte Register, which contains the byte to be placed in the control field of the transmitted frame during non-AUTO-mode transmission. The CPU should access TCB only when the SIU is not transmitting a frame, TBF = 0. TCB is byte addressable.

4.11 Data Clocking Options

The SIU may be clocked in one of two ways, with an external clock or in a self-clocked mode. In the external clocked mode, a serial clock must be provided on SCLK. This clock must be synchronized to the serial data. Incoming data is sampled at the rising edge of SCLK. Outgoing data is shifted out at the falling edge of SCLK.

In the self-clocked mode, the SIU uses a reference clock and the serial data to reproduce the serial data clock. The reference clock can be an external source applied to SCLK, the IA8044/IA8344's internal clock or the Timer 1 overflow. The reference clock must be 16× or 32× the data rate. A DPLL uses the reference clock and the serial data to adjust the sample time to the center of the serial bit. It does this by adjusting from a serial data transition in increments of 1/16 of a bit time.

The maximum data rate in the externally clocked mode is 2.4 Mbps in a point-to-point configuration and 1.0 Mbps in a loop configuration. With a 12-MHz CPU clock, the maximum data rate in the self-clocked mode with an external clock is 375 Kbps. The maximum data rate in the self-clocked mode with an internal clock will depend on the frequency of the IA8044/IA8344's input clock. An IA8044/IA8344 using a 12-MHz input clock can operate at a maximum data rate of 375 Kbps.

The Serial mode register Bits [5], [6], and [7] select the clocking option for the SIU (see SMD register description).

4.12 Operational Modes

The SIU operates in one of two modes, AUTO or FLEXIBLE. The mode selected determines how much intervention is required by the CPU when receiving and transmitting frames. In both modes, short frames, aborted frames, and frames with CRC errors will be ignored.

AUTO mode allows the SIU to recognize and respond to specific SDLC frames without the CPU's intervention. This provides for a faster turnaround time but restricts the operation of the SIU. When in AUTO mode, the SIU can only act as a normal response secondary station and responses will adhere to IBM's SDLC definitions.

When receiving in the AUTO mode, the SIU receives the frame and examines the control byte. It will then take the appropriate action for that frame. If the frame is an information frame, the SIU will load the receive buffer, interrupt the CPU and make the required response to the primary station. The SIU in AUTO mode can also respond to the following commands from the primary station:

- RR (Receive ready)
- RNR (Receive Not Ready)
- REJ (Reject)

The no-control field format is only supported by the FLEXIBLE mode. In this format, TCB and RCB are not used and the information field starts immediately after the address field. A control field may still be used in the frame but the SIU will treat it as a byte of the information field.

The no-control field and no-address field formats are supported only by the FLEXIBLE mode. In this format STAD, TCB, and RCB are not used and the information field starts immediately after the opening flag. This option can only be used with the no-control field option. A control field and address field may still be used in the frame but the SIU will treat each as a byte of the information field.

The no FCS field format prevents an FCS from being generated during transmission or being checked during reception. This option may be used in conjunction with the other frame format options. This option will work with both FLEXIBLE and AUTO modes. In AUTO mode, it could cause protocol violations. An FCS field may still be used in the frame but the SIU will treat it as a byte of the information field.

All the possible Frame Format combinations are presented in Table 47, along with the bit settings that select a given format.

Table 47. Frame Format Options

Frame Option	NFCS	NB	AM	Frame Format
Standard SDLC FLEXIBLE Mode	0	0	0	Fl | Ad | Co | Inf | FCS | Fl
Standard SDLC AUTO Mode	0	0	1	Fl | Ad | Co | Inf | FCS | Fl
No-Control Field FLEXIBLE Mode	0	1	1	Fl | Ad | Inf | FCS | Fl
No-Control Field No-Address Field FLEXIBLE Mode	0	1	0	Fl | Inf | FCS | Fl
No-FCS Field FLEXIBLE Mode	1	0	0	Fl | Ad | Co | Inf | Fl
No-FCS Field AUTO Mode	1	0	1	Fl | Ad | Co | Inf | Fl

4.15.2 BYP

The BYP contains registers and controllers used to perform the manipulations required for SDLC communications. The BYP registers may be accessed by the CPU (see Table 7, SFR Bit Addressable Locations). The BYP contains the SIU state machine that controls transmission and reception of frames.

4.16 Diagnostics

A diagnostic mode is included with the IA8044/IA8344 to allow testing of the SIU. Diagnostics use port pins P3.0 and P3.1. Writing a "0" to P3.1 enables the diagnostic mode. When P3.1 is cleared, writing data to P3.0 has the effect of writing a serial data stream to the SIU. P3.0 is the serial data and any write to Port 3 will clock SCLK. The transmit data may be monitored on P3.1 with any write to Port 3, again clocking SCLK. In the test mode P3.0 and P3.1 pins are placed in the high impedance state (see Figure 12).

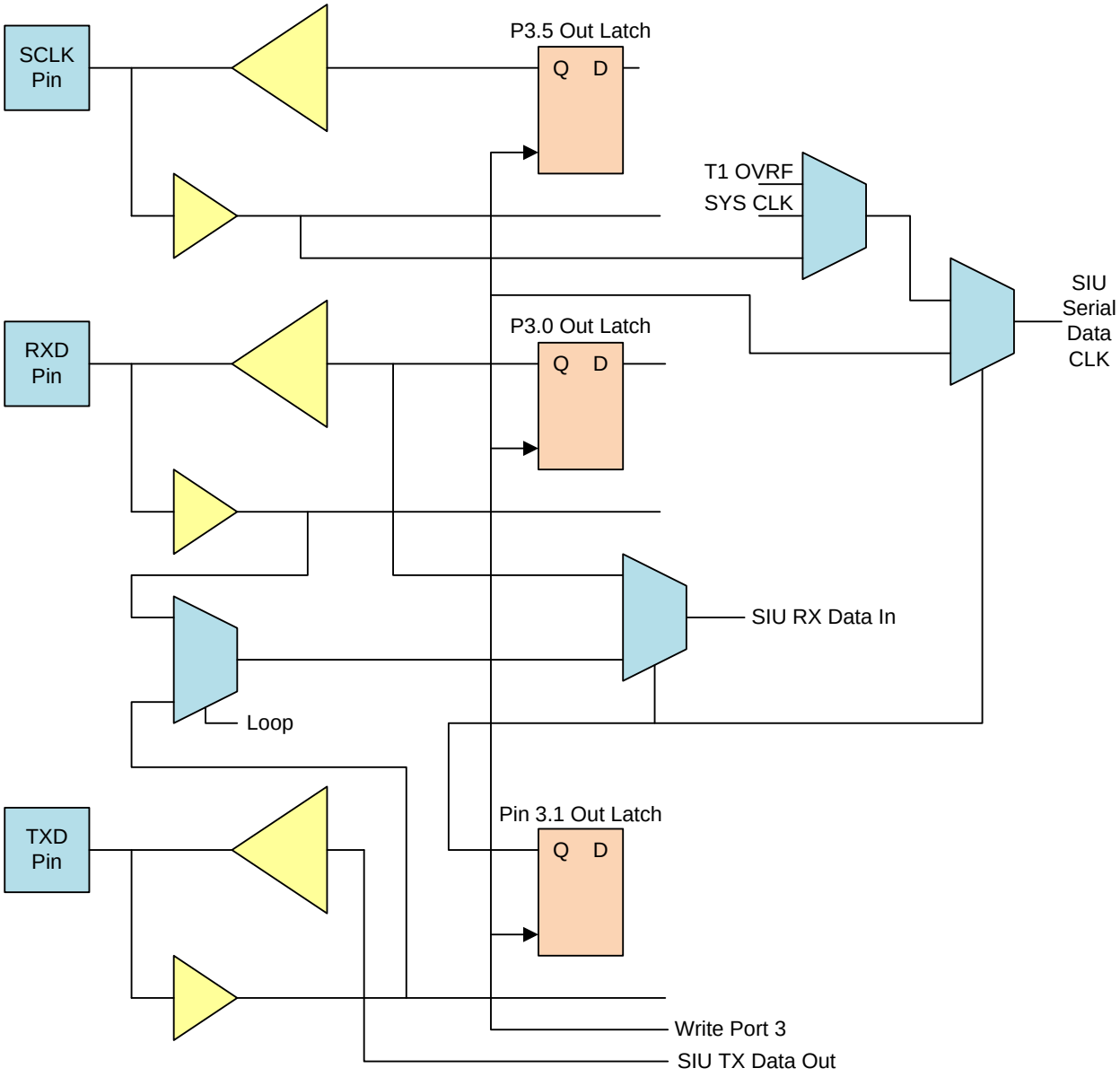


Figure 12. Diagnostic Signal Routing

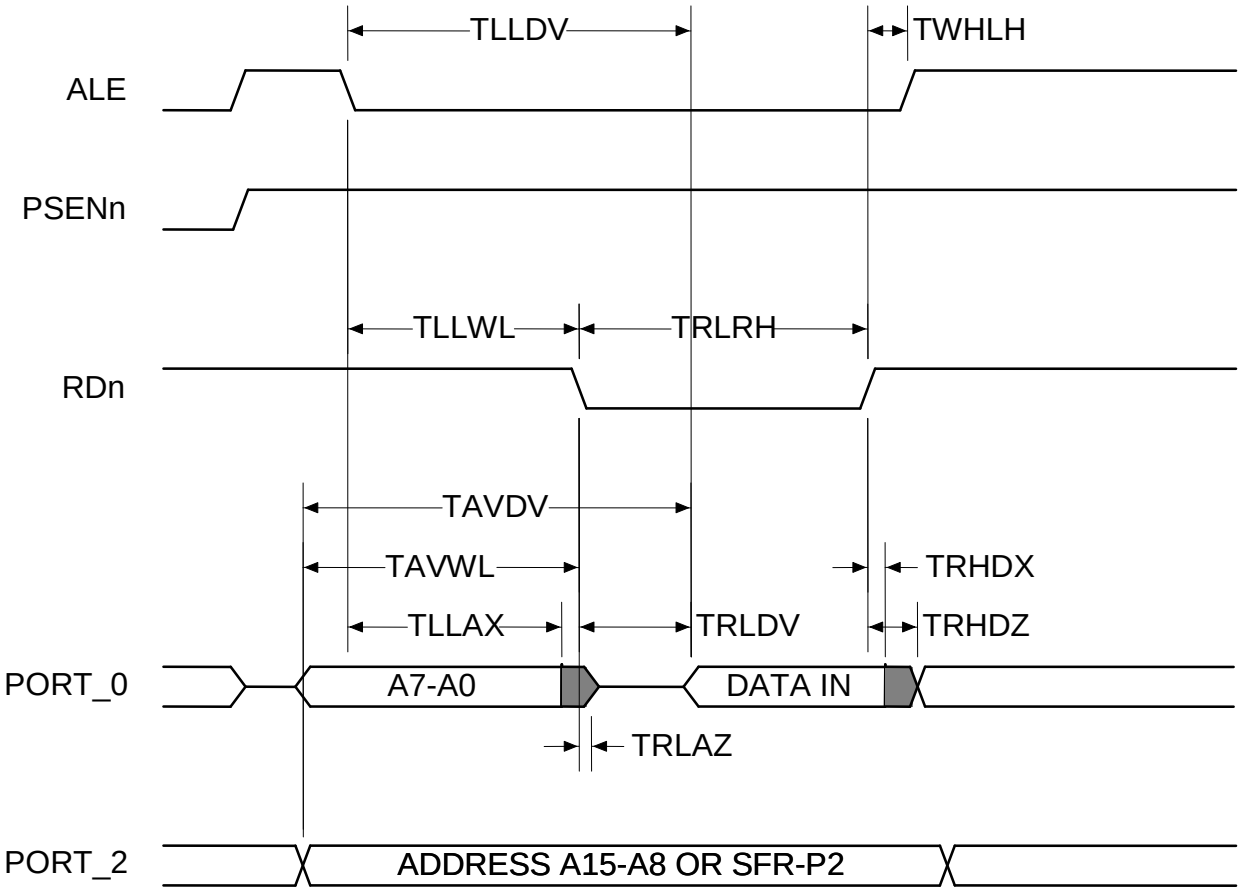


Figure 14. Data Memory Read Cycle

5.2 Serial I/O Waveforms

The IA8044/IA8344 synchronous data transmission and synchronous data reception are presented in Figures 16 and 17, respectively.

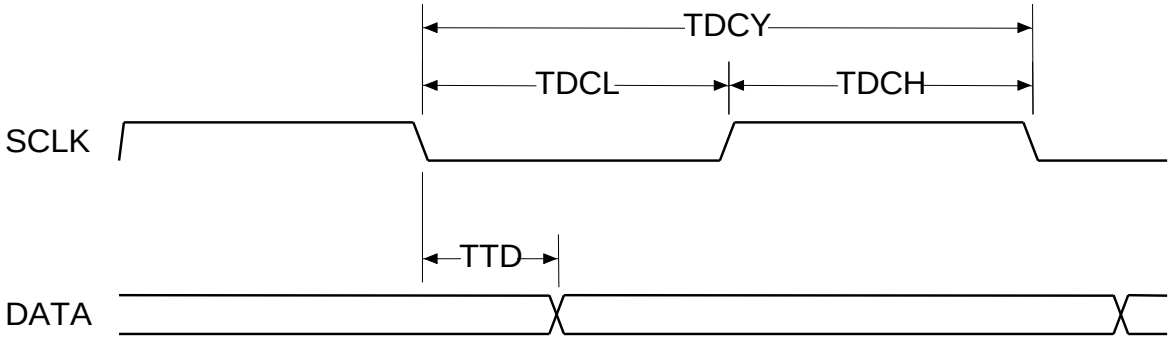


Figure 16. Synchronous Data Transmission

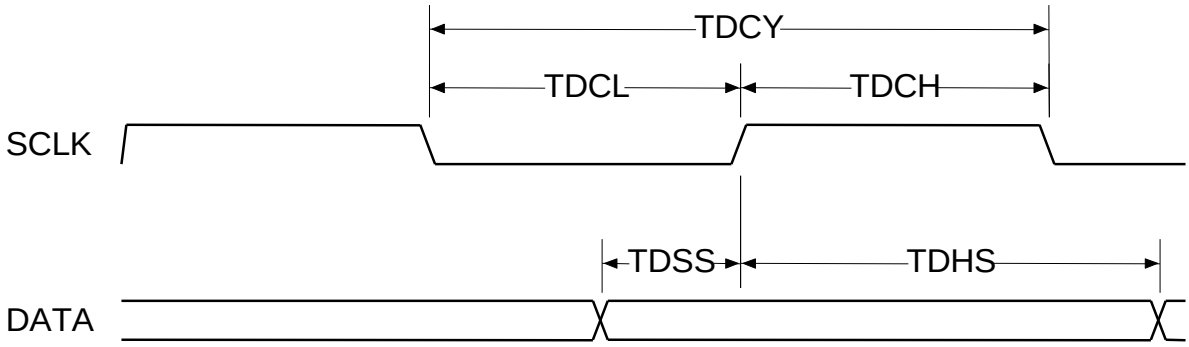


Figure 17. Synchronous Data Reception

6. Reset

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods) while the oscillator is running. The CPU responds by generating an internal reset, which is executed during the second cycle in which RST is high.

The internal reset sequence affects all SFRs as shown in Table 52. The internal reset sequence does not affect the contents of internal RAM.

Table 52. Reset Values Register

Register	Reset value
PC	0000H
ACC	00000000B
B	00000000B
PSW	00000000B
SP	00000111B
DPTR	0000H
P0–P3	11111111B
IP	XXX00000B
IE	0XX00000B
TMOD	00000000B
TCON	00000000B
TH0	00000000B
TL0	00000000B
TH1	00000000B
TL1	00000000B
SMD	00000000B
STS	00000000B
NSNR	00000000B
STAD	XXXXXXXXB
TBS	XXXXXXXXB
TBL	XXXXXXXXB
TCB	XXXXXXXXB
RBS	XXXXXXXXB
RBL	XXXXXXXXB
RFL	XXXXXXXXB
RCB	XXXXXXXXB
DMA CNT	00000000B
FIFO1	00000000B
FIFO2	00000000B
FIFO3	00000000B
SIUST	00000001B

7. Instruction Set

The IA8044 and IA8344 architecture and instruction set are identical to the Intel 8051's. Tables 53 through 57 present the instruction set of the IA8044/IA8344 microcontroller core.

Table 53. Arithmetic Operations

Mnemonic	Description	Byte	Cycle
ADD A,Rn	Add register to accumulator	1	1
ADD A, direct	Add direct byte to accumulator	2	1
ADD A,@Ri	Add indirect RAM to accumulator	1	1
ADD A,#data	Add immediate data to accumulator	2	1
ADDC A,Rn	Add register to accumulator with carry flag	1	1
ADDC A,direct	Add direct byte to A with carry flag	2	1
ADDC A,@Ri	Add indirect RAM to A with carry flag	1	1
ADDC A,#data	Add immediate data to A with carry flag	2	1
SUBB A,Rn	Subtract register from A with borrow	1	1
SUBB A,direct	Subtract direct byte from A with borrow	2	1
SUBB A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB A,#data	Subtract immediate data from A with borrow	2	1
INC A	Increment accumulator	1	1
INC Rn	Increment register	1	1
INC direct	Increment direct byte	2	1
INC @ Ri	Increment indirect RAM	1	1
DEC A	Decrement accumulator	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	1
DEC @Ri	Decrement indirect RAM	1	1
INC DPTR	Increment data pointer	1	2
MUL A,B	Multiply A and B	1	4
DIV A,B	Divide A by B	1	4
DA A	Decimal adjust accumulator	1	1

Errata No. 3

Problem: The device responds to an idle flag one bit time too early.

Description: This causes problems in a loop-mode network. It only occurs in loop mode when using an external SIU clock source and idle flags.

Workaround: None.

Errata No. 4

Problem: Under certain conditions the SIU will overwrite the RCB register when starting a transmission.

Description: The conditions are:

- The SIU is externally clocked.
- The SIU is in flexible mode.
- The CPU has not already read the RCB from a previous reception before the transmission takes place.

Workaround: Read the RCB before initiating a transmit.

11. For Additional Information

The Innovasic Semiconductor IA8044 and IA8344 are "plug-and-play" drop-in replacements and are form, fit, and function compatible parts to the Intel® 8044 and 8344. The IA8044 and IA8344 replace the obsolete Intel 8044 and 8344, allowing users to retain existing board designs, software compilers/assemblers, and emulation tools—thus avoiding expensive redesign efforts.

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Innovasic Support Team
3737 Princeton NE
Suite 130
Albuquerque, NM 87107

(505) 883-5263
Fax: (505) 883-5477
Toll Free: (888) 824-4184
E-mail: support@innovasic.com
Website: http://www.Innovasic.com