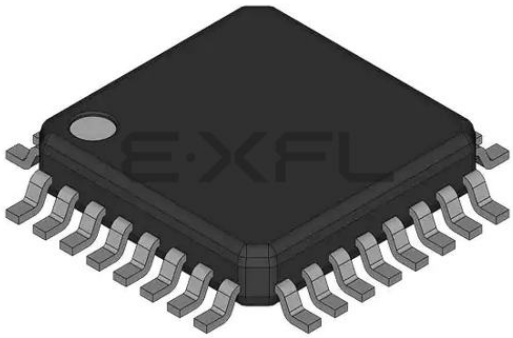

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	26
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f82313vlc

1.4 On-Chip Memory and Memory Protection

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Internal flash memory with security and protection to prevent unauthorized access
- Memory resource protection (MRP) unit to protect supervisor programs and resources from user programs
- Programming code can reside in flash memory during flash programming
- The dual-port RAM controller supports concurrent instruction fetches and data accesses, or dual data accesses by the core.
  - Concurrent accesses provide increased performance.
  - The data and instruction arrive at the core in the same cycle, reducing latency.
- On-chip memory
  - Up to 32 KB program/data flash memory
  - Up to 4 KB dual port data/program RAM

1.5 Interrupt Controller

- Five interrupt priority levels
  - Three user-programmable priority levels for each interrupt source: level 0, level 1, level 2
  - Unmaskable level 3 interrupts include illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction
  - Interrupt level 3 is highest priority and non-maskable. Its sources include:
    - Illegal instructions
    - Hardware stack overflow
    - SWI instruction
    - EOnce interrupts
    - Misaligned data accesses
  - Lowest-priority software interrupt: level LP
- Support for nested interrupts, so that a higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Masking of interrupt priority level is managed by the 56800EX core
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to System Integration Module (SIM) to restart clock when in wait and stop states
- Ability to relocate interrupt vector table

1.6.5 Comparator

- Full rail-to-rail comparison range
- Support for high and low speed modes
- Selectable input source includes external pins and internal DACs
- Programmable output polarity
- 6-bit programmable DAC as a voltage reference per comparator
- Three programmable hysteresis levels
- Selectable interrupt on rising-edge, falling-edge, or toggle of a comparator output

1.6.6 12-bit Digital-to-Analog Converter

- 12-bit resolution
- Powerdown mode
- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms, including square, triangle, and sawtooth waveforms (for applications like slope compensation)
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, ADC, or optionally to an off-chip destination

1.6.7 Quad Timer

- Four 16-bit up/down counters, with a programmable prescaler for each counter
- Operation modes: edge count, gated count, signed count, capture, compare, PWM, signal shot, single pulse, pulse string, cascaded, quadrature decode
- Programmable input filter
- Counting start can be synchronized across counters
- Up to 100 MHz operation clock

1.6.8 Queued Serial Communications Interface (QSCI) modules

- Operating clock can be up to two times the CPU operating frequency
- Four-word-deep FIFOs available on both transmit and receive buffers
- Standard mark/space non-return-to-zero (NRZ) format
- 16-bit integer and 3-bit fractional baud rate selection
- Full-duplex or single-wire operation
- Programmable 8-bit or 9-bit data format
- Error detection capability

- Two receiver wakeup methods:
  - Idle line
  - Address mark
- 1/16 bit-time noise detection
- Up to 6.25 Mbit/s baud rate at 100 MHz operation clock

1.6.9 Queued Serial Peripheral Interface (QSPI) modules

- Maximum 12.5 Mbit/s baud rate
- Selectable baud rate clock sources for low baud rate communication
- Baud rate as low as Baudrate_Freq_in / 8192
- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four-word-deep FIFOs available on transmit and receive buffers
- Programmable length transmissions (2 bits to 16 bits)
- Programmable transmit and receive shift order (MSB as first bit transmitted)

1.6.10 Inter-Integrated Circuit (I2C)/System Management Bus (SMBus) modules

- Compatible with I2C bus standard
- Support for System Management Bus (SMBus) specification, version 2
- Multi-master operation
- General call recognition
- 10-bit address extension
- Start/Repeat and Stop indication flags
- Support for dual slave addresses or configuration of a range of slave addresses
- Programmable glitch input filter with option to clock up to 100 MHz

1.6.11 Windowed Computer Operating Properly (COP) watchdog

- Programmable windowed timeout period
- Support for operation in all power modes: run mode, wait mode, stop mode
- Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
- Selectable reference clock source in support of EN60730 and IEC61508
- Selectable clock sources:
  - External crystal oscillator/external clock source
  - On-chip low-power 200 kHz oscillator

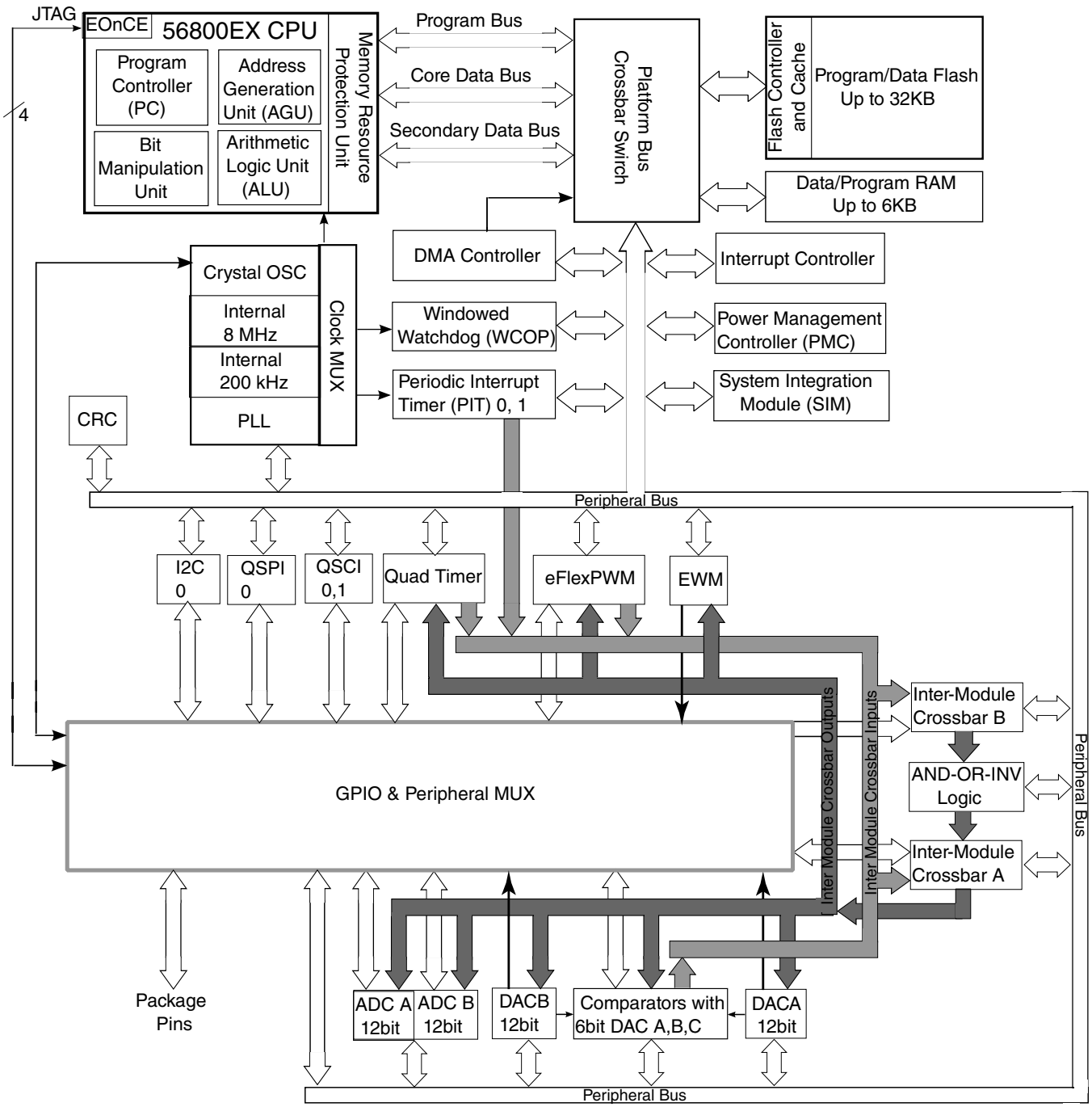


Figure 2. System diagram

Table 2. Signal descriptions (continued)

Signal Name	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
					The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
(RXD0)			Input		SCI0 receive data input
(XB_IN9)			Input		Crossbar module input 9
(XB_OUT6)			Output		Crossbar module output 6
GPIOC9	26	17	Input/ Output	Input, internal pullup enabled	GPIO Port C9: After reset, the default state is GPIOC9.
(SCLK0)			Input/ Output		SPI0 serial clock. In master mode, SCLK0 pin is an output, clocking slaved listeners. In slave mode, SCLK0 pin is the data clock input.
(XB_IN4)			Input		Crossbar module input 4
(TXD0)			Output		SCI0 transmit data output or transmit/receive in single wire operation
(XB_OUT8)			Output		Crossbar module output 8
GPIOC10	27	18	Input/ Output	Input, intemrnal pullup enabled	GPIO Port C10: After reset, the default state is GPIOC10.
(MOSI0)			Input/ Output		Master out/slave in for SPI0 — In master mode, MOSI0 pin is the data output. In slave mode, MOSI0 pin is the data input.
(XB_IN5)			Input		Crossbar module input 5
(MISO0)			Input/ Output		Master in/slave out for SPI0 — In master mode, MISO0 pin is the data input. In slave mode, MISO0 pin is the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
(XB_OUT9)			Output		Crossbar module output 9
GPIOC11	29	—	Input/ Output	Input, internal pullup enabled	GPIO Port C11: After reset, the default state is GPIOC11.
(SCL0)			Input/ Open-drain Output		I^2C0 serial clock
(TXD1)			Output		SCI1 transmit data output or transmit/receive in single wire operation
GPIOC12	30	—	Input/ Output	Input, internal pullup enabled	GPIO Port C12: After reset, the default state is GPIOC12.
(SDA0)			Input/ Open-drain Output		I^2C0 serial data line
(RXD1)			Input		SCI1 receive data input
GPIOC13	37	—	Input/ Output	Input, internal pullup enabled	GPIO Port C13: After reset, the default state is GPIOC13.
(TA3)			Input/ Output		Quad timer module A channel 3 input/output
(XB_IN6)			Input		Crossbar module input 6

Table continues on the next page...

Table 2. Signal descriptions (continued)

Signal Name	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
GPIOF0	28	—	Input/ Output	Input, internal pullup enabled	GPIO Port F0: After reset, the default state is GPIOF0.
(XB_IN6)			Input		Crossbar module input 6
(SCLK1)			Input/ Output		SPI1 serial clock — In master mode, SCLK1 pin is an output, clocking slaved listeners. In slave mode, SCLK1 pin is the data clock input 0.
GPIOF1	38	—	Input/ Output	Input, internal pullup enabled	GPIO Port F1: After reset, the default state is GPIOF1.
(CLKO1)			Output		Buffered clock output 1: the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
(XB_IN7)			Input		Crossbar module input 7
GPIOF2	—	19	Input/ Output	Input, internal pullup enabled	GPIO Port F2: After reset, the default state is GPIOF2.
(SCL0)			Input/ Open-drain Output		I^2C0 serial clock
(XB_OUT6)			Output		Crossbar module output 6
(MISO1)			Input/ Output		Master in/slave out for SPI1 —In master mode, MISO1 pin is the data input. In slave mode, MISO1 pin is the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
GPIOF3	—	20	Input/ Output	Input, internal pullup enabled	GPIO Port F3: After reset, the default state is GPIOF3.
(SDA0)			Input/ Open-drain Output		I^2C0 serial data line
(XB_OUT7)			Output		Crossbar module output 7
(MOSI1)			Input/ Output		Master out/slave in for SPI1— In master mode, MOSI1 pin is the data output. In slave mode, MOSI1 pin is the data input.

1. If CLKIN is selected as the device's external clock input, then both the GPS_C0 bit (in GPS1) and the EXT_SEL bit (in OCCS oscillator control register (OSCTL)) must be set. Also, the crystal oscillator should be powered down.

2.1 Signal groups

The input and output signals of the MC56F8F823xx are organized into functional groups, as detailed in Table 3.

Table 3. Functional Group Pin Allocations

Functional Group	Number of Pins	
	32LQFP	48LQFP
Power Inputs (V_{DD}, V_{DDA}), Power output(V_{CAP})	3	5
Ground (V_{SS}, V_{SSA})	3	4
Reset	1	1
Queued Serial Peripheral Interface (QSPI0 and QSPI1) ports	4	5
Queued Serial Communications Interface (QSCI0 and QSCI1) ports	4	7
Inter-Integrated Circuit Interface (I^2C0) ports	2	4
12-bit Analog-to-Digital Converter inputs	6	10
Analog Comparator inputs/outputs	5/2	9/3
12-bit Digital-to-Analog output	0	2
Quad Timer Module (TMRA and TMRB) ports	3	4
Inter-Module Crossbar inputs/outputs	8/4	12/6
Clock inputs/outputs	1/1	2/2
JTAG / Enhanced On-Chip Emulation (EOnCE)	4	4

3 Ordering parts

3.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **freescale.com** and perform a part number search for the following device numbers: MC56F82

4 Part identification

4.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

4.2 Format

Part numbers for this device have the following format: Q 56F8 2 C F P T PP N

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

5.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

5.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	μA

5.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

5.3.1 Example

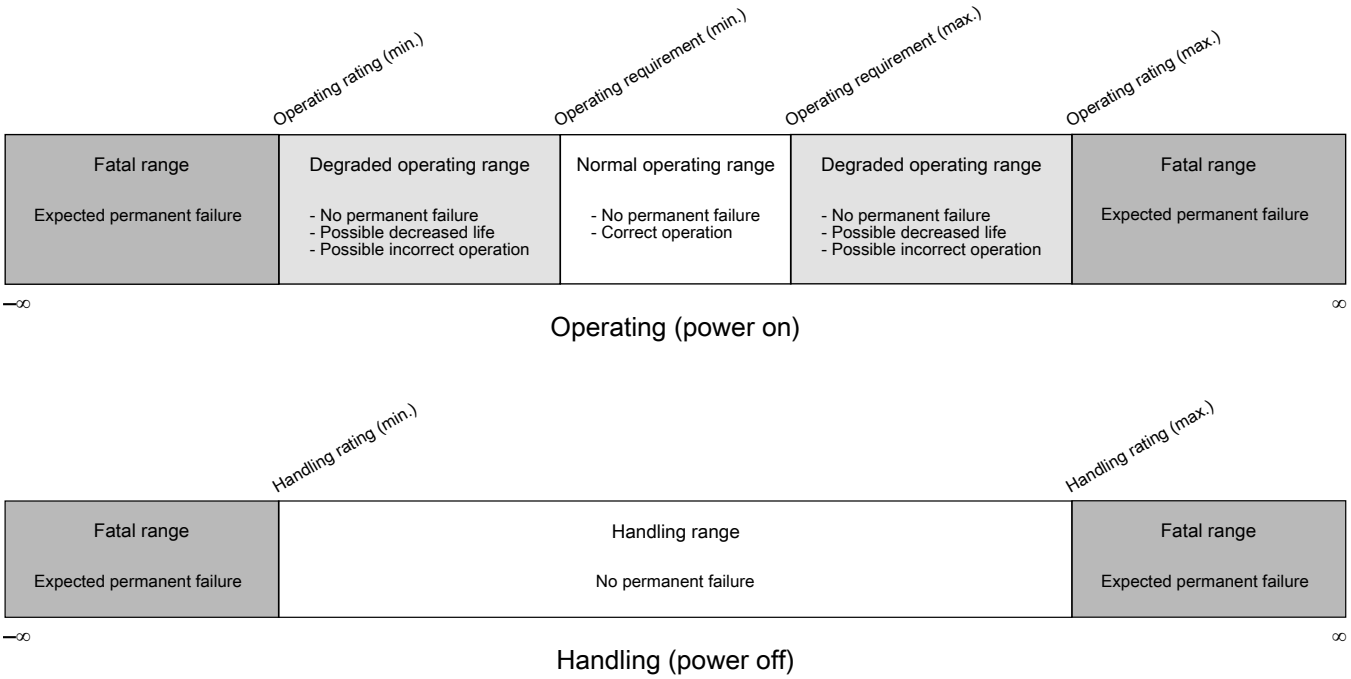
This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

5.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

5.6 Relationship between ratings and operating requirements



5.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

5.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

6 Ratings

6.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.3 ESD handling ratings

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

All latch-up testing is in conformity with AEC-Q100 Stress Test Qualification.

A device is defined as a failure if after exposure to ESD pulses, the device no longer meets the device specification. Complete DC parametric and functional testing is performed as per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 11. Current Consumption (mA)

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25°C		Maximum at 3.6 V, 105°C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
		• PLL disabled • All peripheral modules, except COP, disabled and clocks gated off • Processor core in stop mode				

1. No output switching, all ports configured as inputs, all inputs low, no DC loads.

7.3.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

7.3.7 Capacitance attributes

Table 12. Capacitance attributes

Description	Symbol	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	—	10	—	pF
Output capacitance	C_{OUT}	—	10	—	pF

7.4 Switching specifications

7.4.1 Device clock specifications

Table 13. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYSCLK}	Device (system and core) clock frequency • using relaxation oscillator • using external clock source	 0.001 0	 50 50	MHz	
f_{BUS}	Bus clock	—	50	MHz	

7.4.2 General switching timing

Table 14. Switching timing

Symbol	Description	Min	Max	Unit	Notes
	GPIO pin interrupt pulse width[1] Synchronous path	1.5		IP Bus Clock Cycles	
	Port rise and fall time (high drive strength), Slew disabled 2.7 ≤ V_{DD} ≤ 3.6V.	5.5	15.1	ns	
	Port rise and fall time (high drive strength), Slew enabled 2.7 ≤ V_{DD} ≤ 3.6V.	1.5	6.8	ns	2
	Port rise and fall time (low drive strength). Slew disabled . 2.7 ≤ V_{DD} ≤ 3.6V	8.2	17.8	ns	
	Port rise and fall time (low drive strength). Slew enabled . 2.7 ≤ V_{DD} ≤ 3.6V	3.2	9.2	ns	3

1. Applies to a pin only when it is configured as GPIO and configured to cause an interrupt by appropriately programming GPIOn_IPOLR and GPIOn_IENR.
2. 75 pF load
3. 15 pF load

7.5 Thermal specifications

7.5.1 Thermal operating requirements

Table 15. Thermal operating requirements

Symbol	Description		Min	Max	Unit
T_J	Die junction temperature		–40	125	°C
T_A	Ambient temperature		–40	105	°C

7.5.2 Thermal attributes

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To account for $P_{I/O}$ in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is very small.

Table 28. DAC parameters (continued)

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
	410 to 3891 ($19A - $F33) 5% to 95% of full range					
Differential non-linearity[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	DNL	—	+/- 0.8	+/- 0.9	LSB[3]
Monotonicity	> 6 sigma monotonicity, < 3.4 ppm non-monotonicity		guaranteed			—
Offset error[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	V_{OFFSET}	—	+/- 25	+ /- 43	mV
Gain error[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	E_{GAIN}	—	+/- 0.5	+/- 1.5	%
DAC Output						
Output voltage range	Within 40 mV of either V_{SSA} or V_{DDA}	V_{OUT}	V_{SSA} + 0.04 V	—	V_{DDA} - 0.04 V	V
AC Specifications						
Signal-to-noise ratio		SNR	—	85	—	dB
Spurious free dynamic range		SFDR	—	-72	—	dB
Effective number of bits		ENOB	—	11	—	bits

1. Settling time is swing range from V_{SSA} to V_{DDA}
2. No guaranteed specification within 5% of V_{DDA} or V_{SSA}
3. LSB = 0.806 mV

8.5.3 CMP and 6-bit DAC electrical specifications

Table 29. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	2.7	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	300	—	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	36	—	µA
V_{AIN}	Analog input voltage	V_{SS}	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis				
	• CR0[HYSTCTR] = 00[1]	—	5	13	mV
	• CR0[HYSTCTR] = 01	—	25	48	mV
	• CR0[HYSTCTR] = 10[2]	—	55	105	mV
	• CR0[HYSTCTR] = 11[2]	—	80	148	mV

Table continues on the next page...

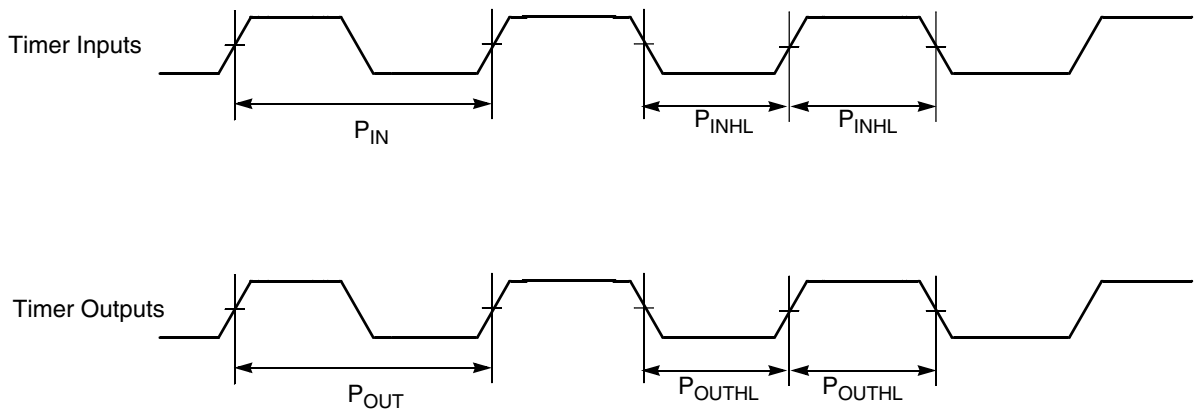


Figure 12. Timer timing

8.7 Communication interfaces

8.7.1 Queued Serial Peripheral Interface (SPI) timing

Parameters listed are guaranteed by design.

Table 31. SPI timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	60 60	— —	ns ns	Figure 13 Figure 14 Figure 15 Figure 16
Enable lead time Master Slave	t_{ELD}	— 20	— —	ns ns	Figure 16
Enable lag time Master Slave	t_{ELG}	— 20	— —	ns ns	Figure 16
Clock (SCK) high time Master Slave	t_{CH}		— —	ns ns	Figure 13 Figure 14 Figure 15 Figure 16
Clock (SCK) low time Master Slave	t_{CL}	28 28	— —	ns ns	Figure 16
Data set-up time required for inputs Master	t_{DS}	20	—	ns	Figure 13 Figure 14

Table continues on the next page...

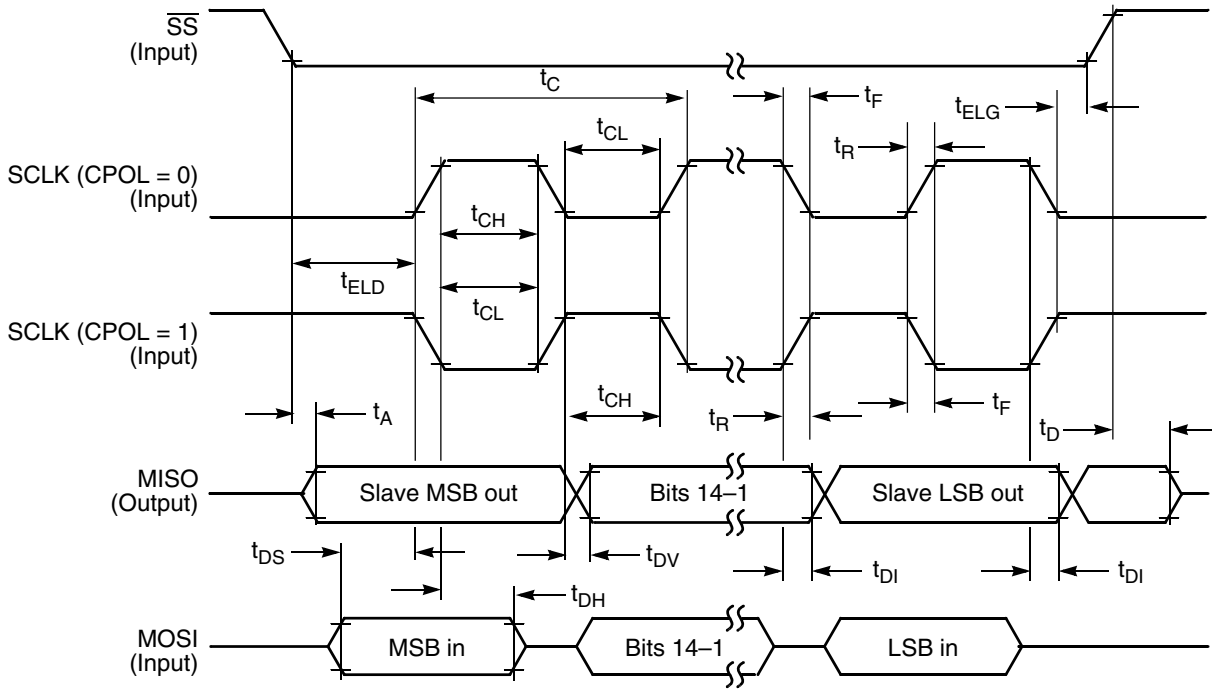


Figure 15. SPI slave timing (CPHA = 0)

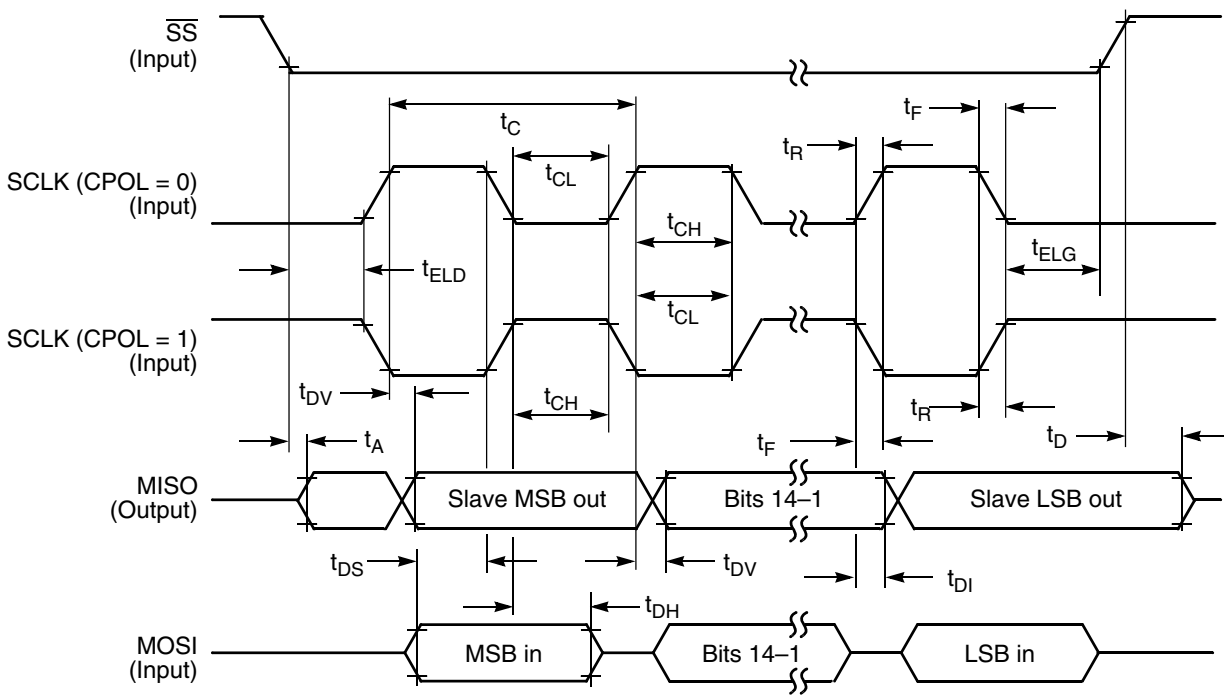


Figure 16. SPI slave timing (CPHA = 1)

- Bypass the V_{DD} and V_{SS} with approximately 100 µF, plus the number of 0.1 µF ceramic capacitors.
- PCB trace lengths should be minimal for high-frequency signals.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA}, and V_{SSA} pins.
- Using separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and V_{SSA} are recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, then connect a small inductor or ferrite bead in serial with V_{DDA}. Traces of V_{SS} and V_{SSA} should be shorted together.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Because the flash memory is programmed through the JTAG/EOnCE port, SPI, SCI, or I^2C, the designer should provide an interface to this port if in-circuit flash programming is desired.
- If desired, connect an external RC circuit to the $\overline{\text{RESET}}$ pin. The resistor value should be in the range of 4.7 kΩ–10 kΩ; the capacitor value should be in the range of 0.22 µF–4.7 µF.
- Configuring the $\overline{\text{RESET}}$ pin to GPIO output in normal operation in a high-noise environment may help to improve the performance of noise transient immunity.
- Add a 2.2 kΩ external pullup on the TMS pin of the JTAG port to keep EOnCE in a restate during normal operation if JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at tri-state.
- To eliminate PCB trace impedance effect, each ADC input should have a no less than 33 pF 10Ω RC filter.

9.3 Power-on Reset design considerations

9.3.1 Improper power-up sequence between VDD/VSS and VDDA/VSSA:

It is recommended that VDD be kept within 100 mV of VDDA at all times, including power ramp-up and ramp-down. Failure to keep VDDA within 100 mV of VDDA may cause a leakage current through the substrate, between the VDD and VDDA pad cells.

10 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **freescale.com** and perform a keyword search for the drawing's document number:

Drawing for package	Document number to be used
32LQFP	98ASH70029A
32QFN	98ASA00473D
48-pin LQFP	98ASH00962A

11 Pinout

11.1 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The SIM's GPS registers are responsible for selecting which ALT functionality is available on most pins.

NOTE

- The RESETB pin is a 3.3 V pin only.
- If the GPIOC1 pin is used as GPIO, the XOSC should be powered down.
- Not all CMPD pins are not available on 48 LQFP.

NOTE

DAC and CMPC signals are not available on 32 LQFP package.

48 LQFP	32 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
—	19	GPIOF2	GPIOF2	SCL0	XB_OUT6		
—	20	GPIOF3	GPIOF3	SDA0	XB_OUT7		
1	1	TCK	TCK	GPIOD2			
2	2	RESETB	RESETB	GPIOD4			
3	—	GPIOC0	GPIOC0	EXTAL	CLKIN0		
4	—	GPIOC1	GPIOC1	XTAL			
5	3	GPIOC2	GPIOC2	TXD0	XB_OUT11	XB_IN2	CLKO0
6	4	GPIOC3	GPIOC3	TA0	CMPA_O	RXD0	CLKIN1

48 LQFP	32 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
7	5	GPIOC4	GPIOC4	TA1	CMPB_O	XB_IN6	EWM_OUT_B
8	—	GPIOA4	GPIOA4	ANA4			
9	6	GPIOA0	GPIOA0	ANA0&CMPA_IN3	CMPC_O		
10	7	GPIOA1	GPIOA1	ANA1&CMPA_IN0			
11	8	GPIOA2	GPIOA2	ANA2&VREFHA&CMPA_IN1			
12	—	GPIOA3	GPIOA3	ANA3&VREFLA&CMPA_IN2			
13	—	GPIOC5	GPIOC5	DACA_O	XB_IN7		
14	—	GPIOB4	GPIOB4	ANB4&CMPC_IN1			
15	9	VDDA	VDDA				
16	10	VSSA	VSSA				
17	11	GPIOB0	GPIOB0	ANB0&CMPB_IN3			
18	12	GPIOB1	GPIOB1	ANB1&CMPB_IN0	DACB_O		
19	—	VCAP	VCAP				
20	13	GPIOB2	GPIOB2	ANB2&VERFHB&CMPC_IN3			
21	—	GPIOB3	GPIOB3	ANB3&VREFLB&CMPC_IN0			
22	14	VSS	VSS				
23	15	GPIOC6	GPIOC6	TA2	XB_IN3	CMP_REF	SS0_B
24	—	GPIOC7	GPIOC7	SS0_B	TXD0	XB_IN8	
25	16	GPIOC8	GPIOC8	MISO0	RXD0	XB_IN9	XB_OUT6
26	17	GPIOC9	GPIOC9	SCLK0	XB_IN4	TXD0	XB_OUT8
27	18	GPIOC10	GPIOC10	MOSI0	XB_IN5	MISO0	XB_OUT9
28	—	GPIOF0	GPIOF0	XB_IN6			
29	—	GPIOC11	GPIOC11		SCL0	TXD1	
30	—	GPIOC12	GPIOC12		SDA0	RXD1	
31	—	VSS	VSS				
32	—	VDD	VDD				
33	21	GPIOE0	GPIOE0	PWM_0B			
34	22	GPIOE1	GPIOE1	PWM_0A			
35	23	GPIOE2	GPIOE2	PWM_1B			
36	24	GPIOE3	GPIOE3	PWM_1A			
37	—	GPIOC13	GPIOC13	TA3	XB_IN6	EWM_OUT_B	
38	—	GPIOF1	GPIOF1	CLKO1	XB_IN7		
39	25	GPIOE4	GPIOE4	PWM_2B	XB_IN2		
40	26	GPIOE5	GPIOE5	PWM_2A	XB_IN3		
41	—	GPIOC14	GPIOC14	SDA0	XB_OUT4	PWM_FAULT4	
42	—	GPIOC15	GPIOC15	SCL0	XB_OUT5	PWM_FAULT5	
43	27	VCAP	VCAP				
44	28	VDD	VDD				

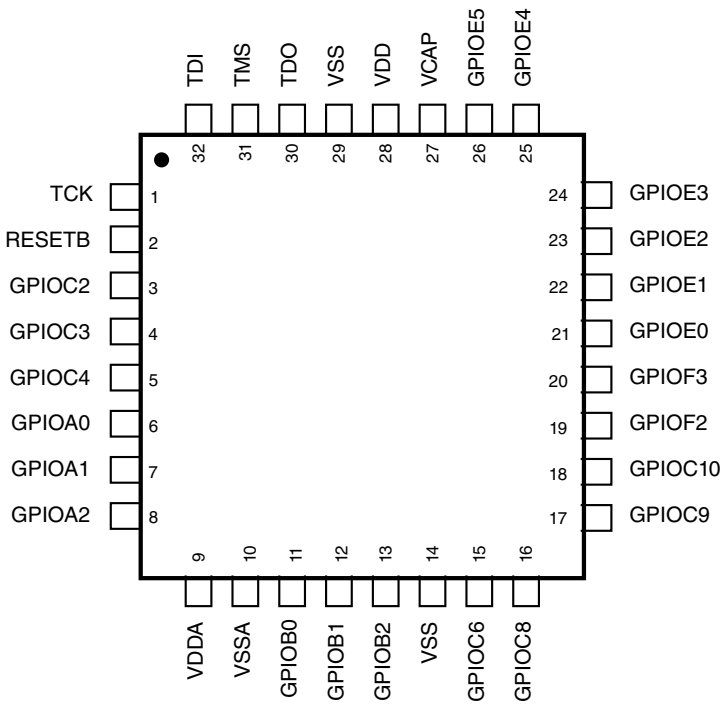


Figure 23. 32-pin LQFP and QFN

NOTE

The RESETB pin is a 3.3 V pin only.

12 Product documentation

The documents listed in Table 34 are required for a complete description and to successfully design using the device. Documentation is available from local NXP distributors, NXP sales offices, or online at **www.nxp.com**.

Table 34. Device documentation

Topic	Description	Document Number
DSP56800E/DSP56800EX Reference Manual	Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F823xx Reference Manual	Detailed functional description and programming model	MC56F823XXRM
MC56F823xx Data Sheet	Electrical and timing specifications, pin descriptions, and package information (this document)	MC56F823XX
MC56F82xxx Errata	Details any chip issues that might be present	MC56F82xxx_Errata

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