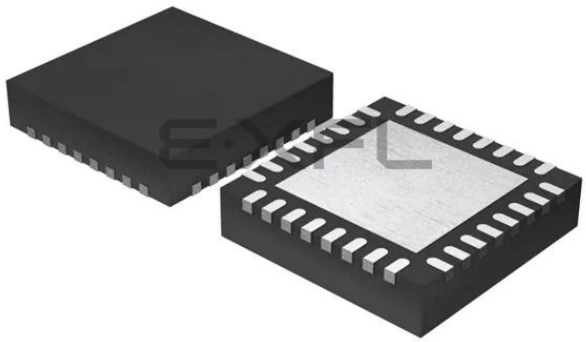

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount, Wettable Flank
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-HVQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f82323vfm

1 Overview

1.1 MC56F823xx Product Family

The following table is the comparsion of features among members of the family.

Table 1. MC56F823xx Family

Part Number	MC56F82		
	323VFM	316V LF	313V LC
Core frequency (MHz)	50	50	50
Flash memory (KB)	32	16	16
RAM (KB)	6	4	4
Interrupt Controller	Yes	Yes	Yes
Windowed Computer Operating Properly (WCOP)	1	1	1
External Watchdog Monitor (EWM)	1	1	1
Periodic Interrupt Timer (PIT)	2	2	2
Cyclic Redundancy Check (CRC)	1	1	1
Quad Timer (TMR)	1x4	1x4	1x4
12-bit Cyclic ADC channels	2x3	2x5	2x3
PWM module : Standard channel with input capture[1]	6	6	6
12-bit DAC	0	2	0
DMA	Yes	Yes	Yes
Analog Comparators (CMP)	2	4	2
QSCI	1	2	1
QSPI	1	1	1
I2C/SMBus	1	1	1
GPIO	26	39	26
Package pin count	32 QFN	48 LQFP	32 LQFP

1. Input capture shares the pin with cooresponding PWM channels.

1.2 56800EX 32-bit Digital Signal Controller (DSC) core

- Efficient 32-bit 56800EX Digital Signal Processor (DSP) engine with modified dual Harvard architecture:
  - Three internal address buses

1.6.5 Comparator

- Full rail-to-rail comparison range
- Support for high and low speed modes
- Selectable input source includes external pins and internal DACs
- Programmable output polarity
- 6-bit programmable DAC as a voltage reference per comparator
- Three programmable hysteresis levels
- Selectable interrupt on rising-edge, falling-edge, or toggle of a comparator output

1.6.6 12-bit Digital-to-Analog Converter

- 12-bit resolution
- Powerdown mode
- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms, including square, triangle, and sawtooth waveforms (for applications like slope compensation)
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, ADC, or optionally to an off-chip destination

1.6.7 Quad Timer

- Four 16-bit up/down counters, with a programmable prescaler for each counter
- Operation modes: edge count, gated count, signed count, capture, compare, PWM, signal shot, single pulse, pulse string, cascaded, quadrature decode
- Programmable input filter
- Counting start can be synchronized across counters
- Up to 100 MHz operation clock

1.6.8 Queued Serial Communications Interface (QSCI) modules

- Operating clock can be up to two times the CPU operating frequency
- Four-word-deep FIFOs available on both transmit and receive buffers
- Standard mark/space non-return-to-zero (NRZ) format
- 16-bit integer and 3-bit fractional baud rate selection
- Full-duplex or single-wire operation
- Programmable 8-bit or 9-bit data format
- Error detection capability

- Two receiver wakeup methods:
  - Idle line
  - Address mark
- 1/16 bit-time noise detection
- Up to 6.25 Mbit/s baud rate at 100 MHz operation clock

1.6.9 Queued Serial Peripheral Interface (QSPI) modules

- Maximum 12.5 Mbit/s baud rate
- Selectable baud rate clock sources for low baud rate communication
- Baud rate as low as Baudrate_Freq_in / 8192
- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four-word-deep FIFOs available on transmit and receive buffers
- Programmable length transmissions (2 bits to 16 bits)
- Programmable transmit and receive shift order (MSB as first bit transmitted)

1.6.10 Inter-Integrated Circuit (I2C)/System Management Bus (SMBus) modules

- Compatible with I2C bus standard
- Support for System Management Bus (SMBus) specification, version 2
- Multi-master operation
- General call recognition
- 10-bit address extension
- Start/Repeat and Stop indication flags
- Support for dual slave addresses or configuration of a range of slave addresses
- Programmable glitch input filter with option to clock up to 100 MHz

1.6.11 Windowed Computer Operating Properly (COP) watchdog

- Programmable windowed timeout period
- Support for operation in all power modes: run mode, wait mode, stop mode
- Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
- Selectable reference clock source in support of EN60730 and IEC61508
- Selectable clock sources:
  - External crystal oscillator/external clock source
  - On-chip low-power 200 kHz oscillator

enable straightforward generation of efficient and compact code for the DSP and control functions. The instruction set is also efficient for C compilers, to enable rapid development of optimized control applications.

The device's basic architecture appears in Figure 1 and Figure 2. Figure 1 shows how the 56800EX system buses communicate with internal memories, and the IPBus interface and the internal connections among the units of the 56800EX core. Figure 2 shows the peripherals and control blocks connected to the IPBus bridge. See the specific device's Reference Manual for details.

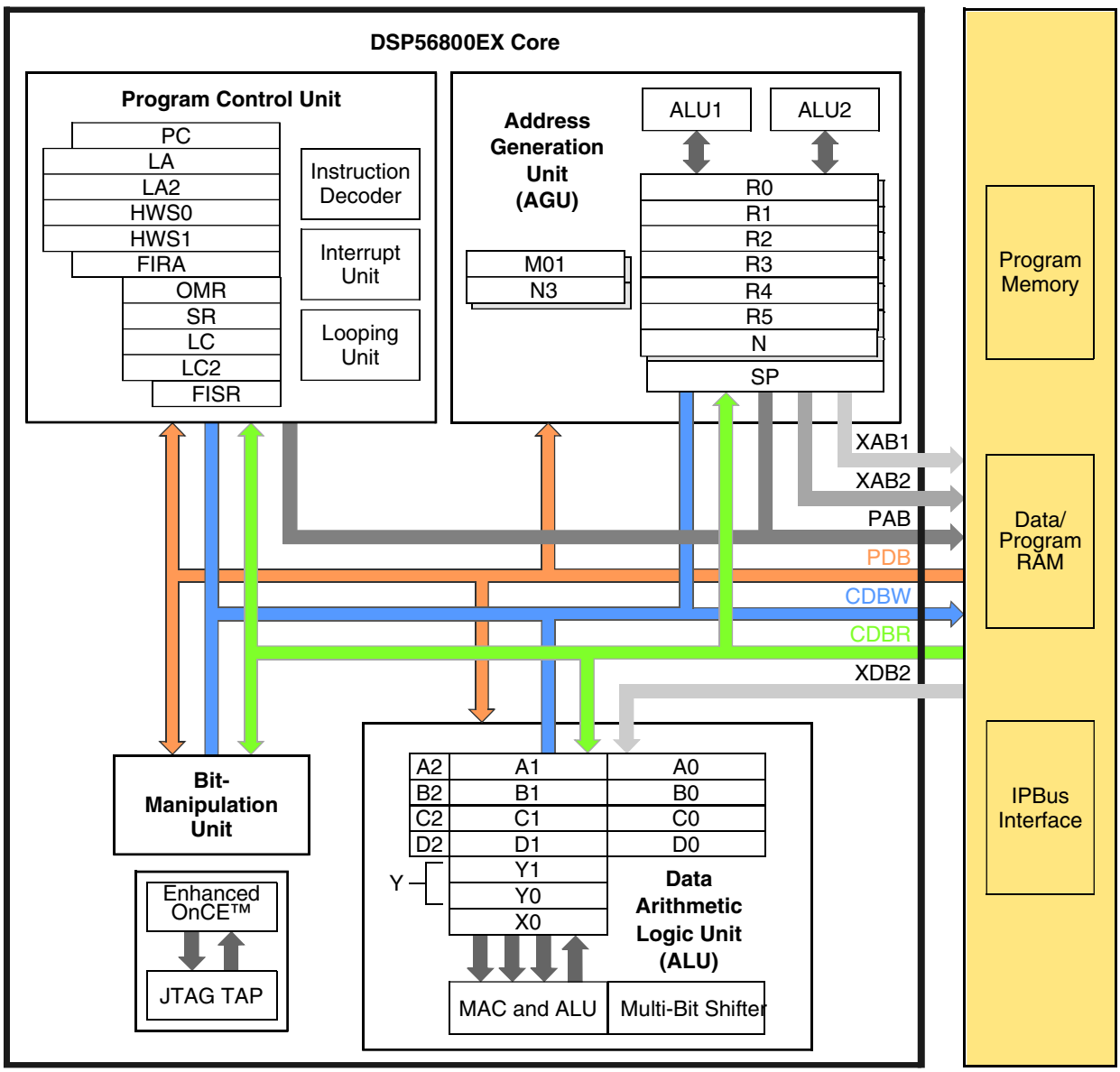


Figure 1. 56800EX basic block diagram

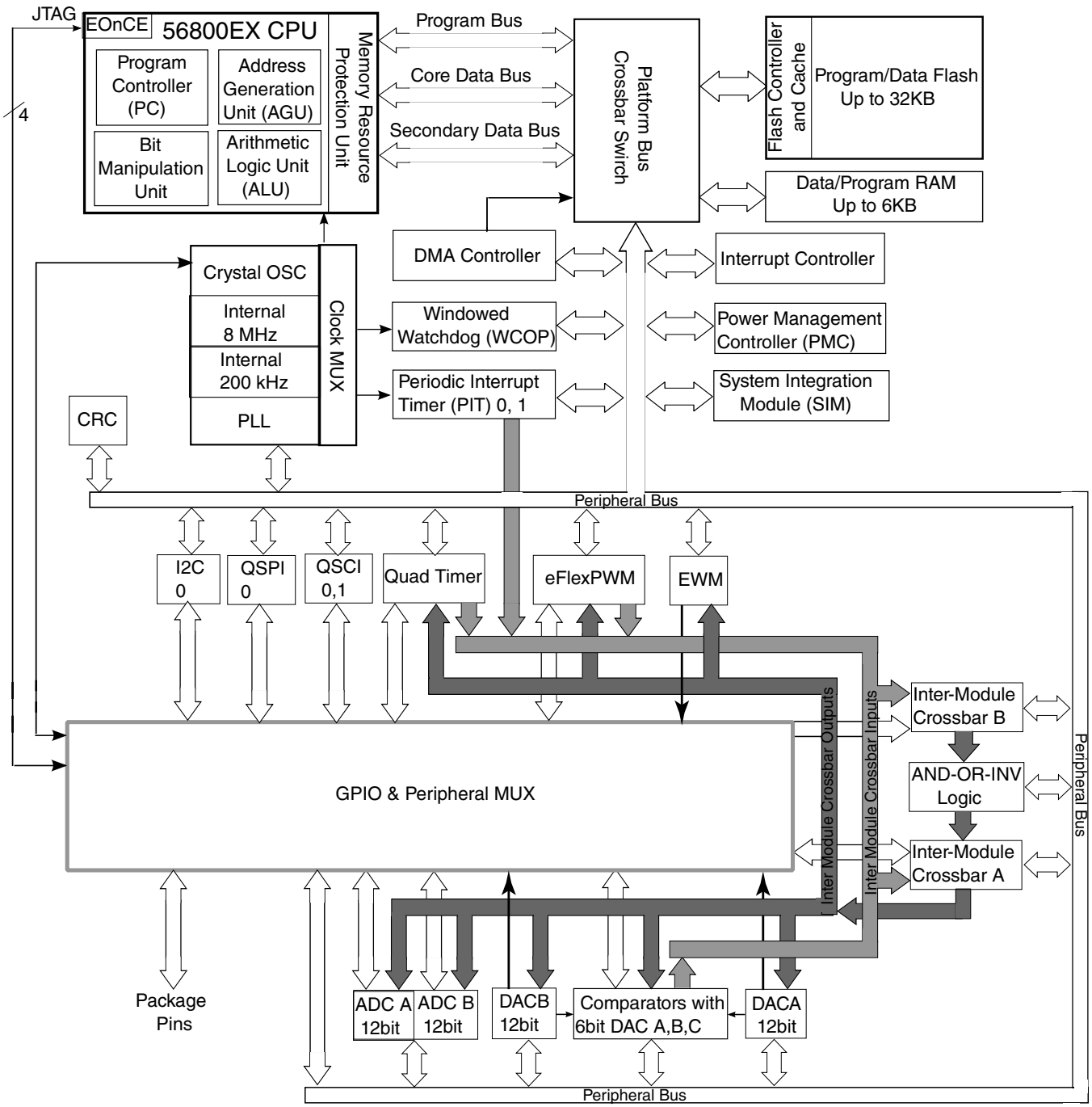


Figure 2. System diagram

Table 2. Signal descriptions (continued)

Signal Name	48 LQFP	32 LQFP	Type	State During Reset	Signal Description
(XB_IN2)			Input		Crossbar module input 2
(CLKO0)			Output		Buffered clock output 0: the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
GPIOC3	6	4	Input/ Output	Input, internal pullup enabled	GPIO Port C3: After reset, the default state is GPIOC3.
(TA0)			Input/ Output		Quad timer module A channel 0 input/output
(CMPA_O)			Output		Analog comparator A output
(RXD0)			Input		SCI0 receive data input
(CLKIN1)			Input		External clock input 1
GPIOC4	7	5	Input/ Output	Input, internal pullup enabled	GPIO Port C4: After reset, the default state is GPIOC4.
(TA1)			Input/ Output		Quad timer module A channel 1 input/output
(CMPB_O)			Output		Analog comparator B output
(XB_IN6)			Input		Crossbar module input 6
(EWM_OUT_B)			Output		External Watchdog Module output
GPIOC5	13	—	Input/ Output	Input, internal pullup enabled	GPIO Port C5: After reset, the default state is GPIOC5.
(DACA_O)			Analog Output		12-bit digital-to-analog output
(XB_IN7)			Input		Crossbar module input 7
GPIOC6	23	15	Input/ Output	Input, internal pullup enabled	GPIO Port C6: After reset, the default state is GPIOC6.
(TA2)			Input/ Output		Quad timer module A channel 2 input/output
(XB_IN3)			Input		Crossbar module input 3
(CMP_REF)			Analog Input		Positive input 3 of analog comparator A and B and C.
($\overline{\text{SS0\_B}}$)			Input/ Output		In slave mode, $\overline{\text{SS0\_B}}$ indicates to the SPI module 0 that the current transfer is to be received.
GPIOC7	24	—	Input/ Output	Input, internal pullup enable	GPIO Port C7: After reset, the default state is GPIOC7.
($\overline{\text{SS0\_B}}$)			Input/ Output		In slave mode, $\overline{\text{SS0\_B}}$ indicates to the SPI module 0 that the current transfer is to be received.
(TXD0)			Output		SCI0 transmit data output or transmit/receive in singlewire operation
(XB_IN8)			Input		Crossbar module input 8
GPIOC8	25	16	Input/ Output	Input, internal pullup enabled	GPIO Port C8: After reset, the default state is GPIOC8.
(MISO0)			Input/ Output		Master in/slave out for SPI0 — In master mode, MISO0 pin is the data input. In slave mode, MISO0 pin is the data output.

Table continues on the next page...

Table 3. Functional Group Pin Allocations

Functional Group	Number of Pins	
	32LQFP	48LQFP
Power Inputs (V_{DD}, V_{DDA}), Power output(V_{CAP})	3	5
Ground (V_{SS}, V_{SSA})	3	4
Reset	1	1
Queued Serial Peripheral Interface (QSPI0 and QSPI1) ports	4	5
Queued Serial Communications Interface (QSCI0 and QSCI1) ports	4	7
Inter-Integrated Circuit Interface (I^2C0) ports	2	4
12-bit Analog-to-Digital Converter inputs	6	10
Analog Comparator inputs/outputs	5/2	9/3
12-bit Digital-to-Analog output	0	2
Quad Timer Module (TMRA and TMRB) ports	3	4
Inter-Module Crossbar inputs/outputs	8/4	12/6
Clock inputs/outputs	1/1	2/2
JTAG / Enhanced On-Chip Emulation (EOnCE)	4	4

3 Ordering parts

3.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **freescale.com** and perform a part number search for the following device numbers: MC56F82

4 Part identification

4.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

4.2 Format

Part numbers for this device have the following format: Q 56F8 2 C F P T PP N

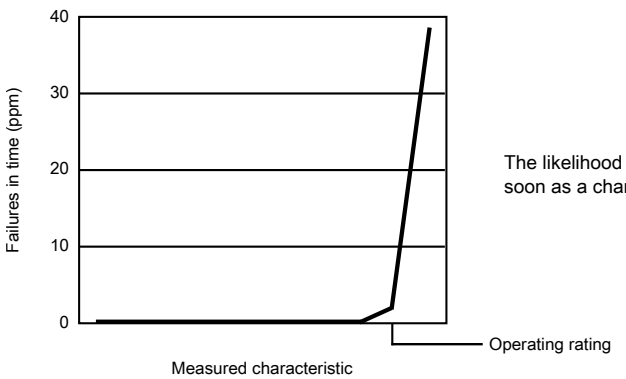
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

5.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

5.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

6 Ratings

6.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.3 ESD handling ratings

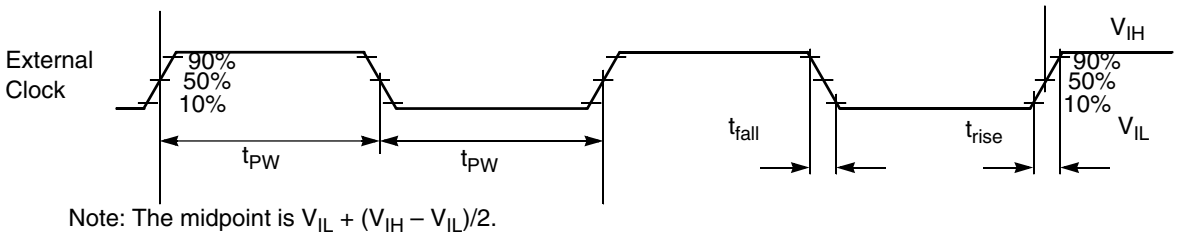
Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

All latch-up testing is in conformity with AEC-Q100 Stress Test Qualification.

A device is defined as a failure if after exposure to ESD pulses, the device no longer meets the device specification. Complete DC parametric and functional testing is performed as per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

1. See Figure 1 for detail on using the recommended connection of an external clock driver.
2. The chip may not function if the high or low pulse width is smaller than 6.25 ns.
3. External clock input rise time is measured from 10% to 90%.
4. External clock input fall time is measured from 90% to 10%.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 7. External clock timing

8.3.2 Phase-Locked Loop timing

Table 20. Phase-Locked Loop timing

Characteristic	Symbol	Min	Typ	Max	Unit
PLL input reference frequency[1]	f_{ref}	8	8	16	MHz
PLL output frequency[2]	f_{op}	200	—	400	MHz
PLL lock time[3]	t_{plls}	35.5		73.2	µs
Allowed Duty Cycle of input reference	t_{dc}	40	50	60	%

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.
2. The frequency of the core system clock cannot exceed 50 MHz. If the NanoEdge PWM is available, the PLL output must be set to 400 MHz.
3. This is the time required *after the PLL is enabled* to ensure reliable operation.

8.3.3 External crystal or resonator requirement

Table 21. Crystal or resonator requirement

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation	f_{XOSC}	4	8	16	MHz

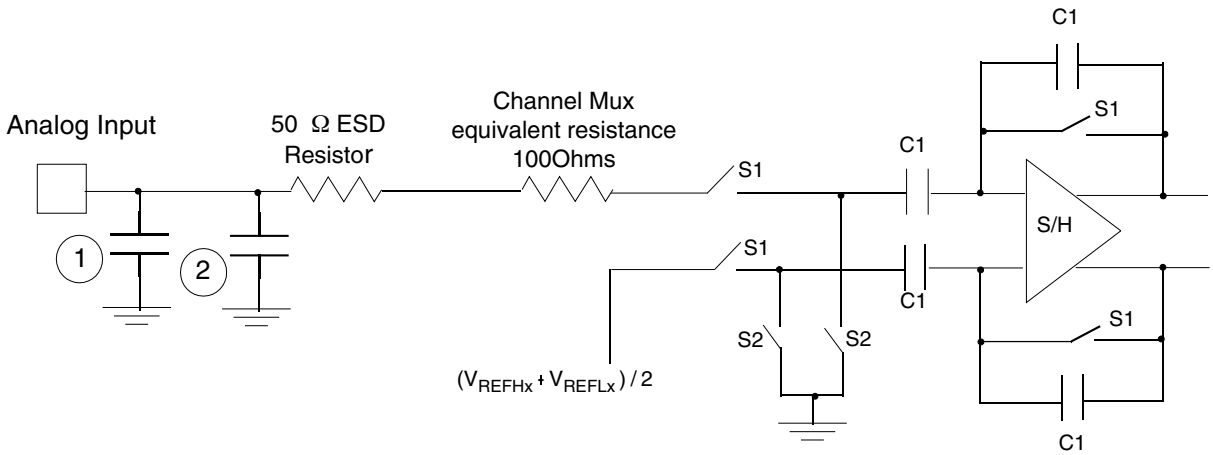
8.3.4 Relaxation Oscillator Timing

Table 22. Relaxation Oscillator Electrical Specifications

Characteristic		Symbol	Min	Typ	Max	Unit
8 MHz Output Frequency[1]						
Run Mode	0°C to 105°C		7.84	8	8.16	MHz

Table continues on the next page...

$$\frac{1}{(\text{ADC ClockRate}) \times 4.8 \times 10^{-12}} + 100\ ohm + 50\ ohm$$



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling = 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing = 2.04pF
3. S1 and S2 switch phases are non-overlapping and depend on the ADC clock frequency

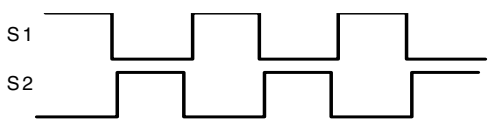


Figure 9. Equivalent circuit for A/D loading

8.5.2 12-bit Digital-to-Analog Converter (DAC) parameters

Table 28. DAC parameters

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
DC Specifications						
Resolution			12	12	12	bits
Settling time[1]	At output load RLD = 3 kΩ CLD = 400 pF		—	1		µs
Power-up time	Time from release of PWRDWN signal until DACOUT signal is valid	t_{DAPU}	—	—	11	µs
Accuracy						
Integral non-linearity[2]	Range of input digital words:	INL	—	+/- 3	+/- 4	LSB[3]

Table continues on the next page...

Table 28. DAC parameters (continued)

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
	410 to 3891 ($19A - $F33) 5% to 95% of full range					
Differential non-linearity[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	DNL	—	+/- 0.8	+/- 0.9	LSB[3]
Monotonicity	> 6 sigma monotonicity, < 3.4 ppm non-monotonicity		guaranteed			—
Offset error[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	V_{OFFSET}	—	+/- 25	+ /- 43	mV
Gain error[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	E_{GAIN}	—	+/- 0.5	+/- 1.5	%
DAC Output						
Output voltage range	Within 40 mV of either V_{SSA} or V_{DDA}	V_{OUT}	V_{SSA} + 0.04 V	—	V_{DDA} - 0.04 V	V
AC Specifications						
Signal-to-noise ratio		SNR	—	85	—	dB
Spurious free dynamic range		SFDR	—	-72	—	dB
Effective number of bits		ENOB	—	11	—	bits

1. Settling time is swing range from V_{SSA} to V_{DDA}
2. No guaranteed specification within 5% of V_{DDA} or V_{SSA}
3. LSB = 0.806 mV

8.5.3 CMP and 6-bit DAC electrical specifications

Table 29. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	2.7	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	300	—	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	36	—	µA
V_{AIN}	Analog input voltage	V_{SS}	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis				
	• CR0[HYSTCTR] = 00[1]	—	5	13	mV
	• CR0[HYSTCTR] = 01	—	25	48	mV
	• CR0[HYSTCTR] = 10[2]	—	55	105	mV
	• CR0[HYSTCTR] = 11[2]	—	80	148	mV

Table continues on the next page...

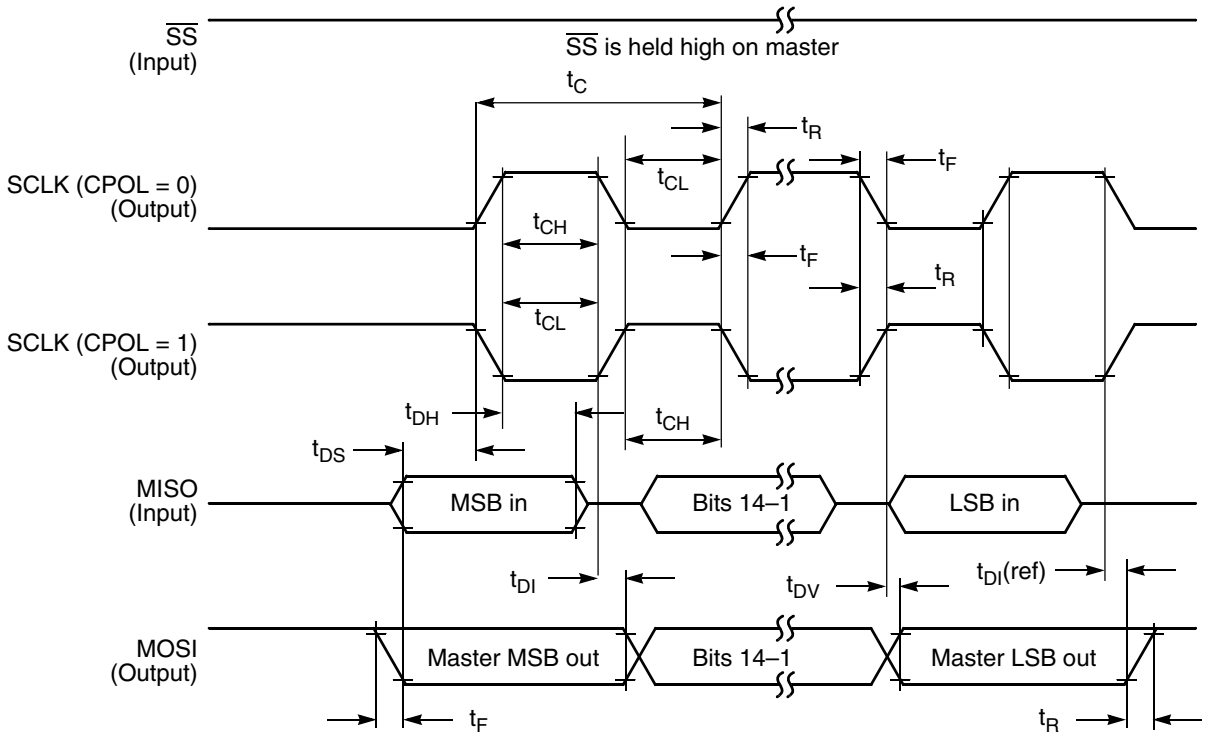


Figure 13. SPI master timing (CPHA = 0)

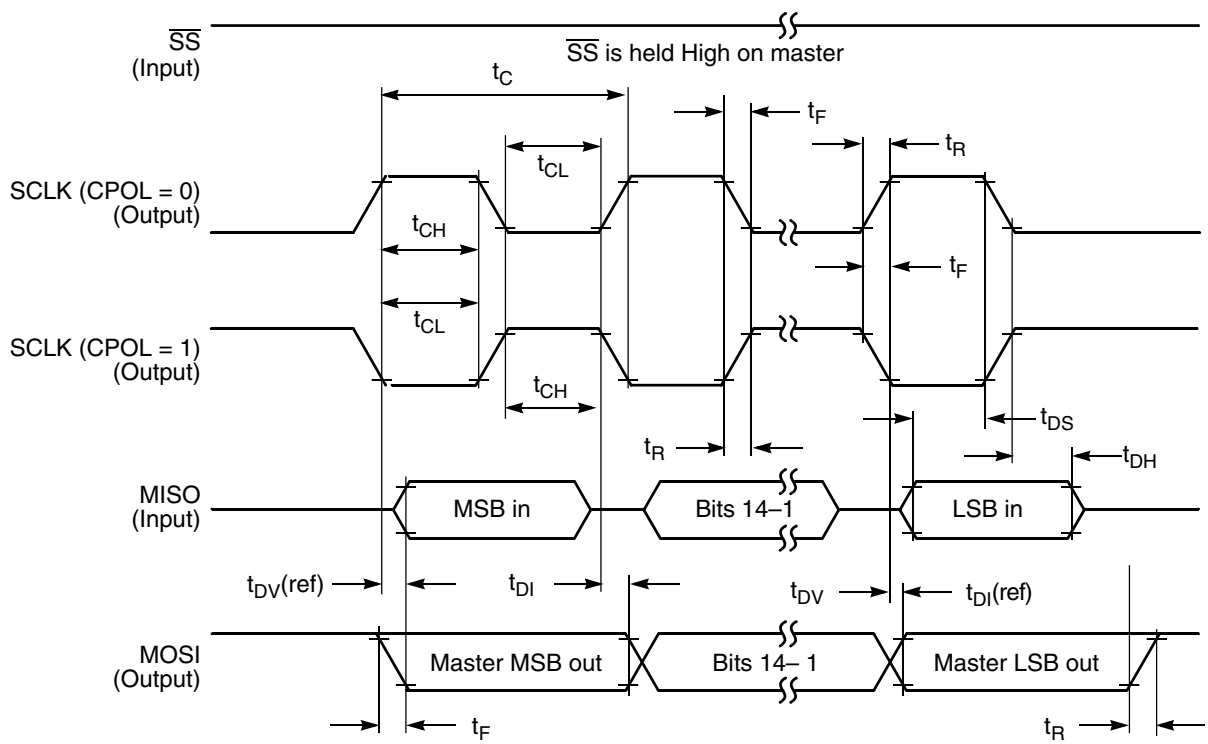


Figure 14. SPI master timing (CPHA = 1)

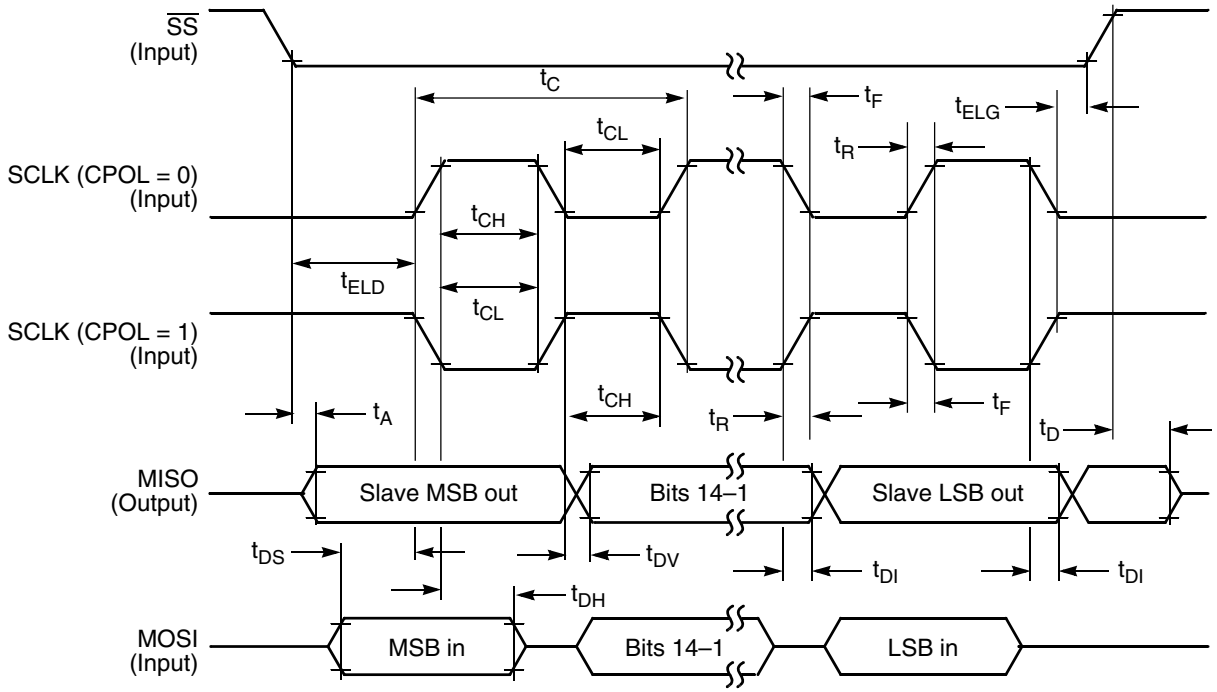


Figure 15. SPI slave timing (CPHA = 0)

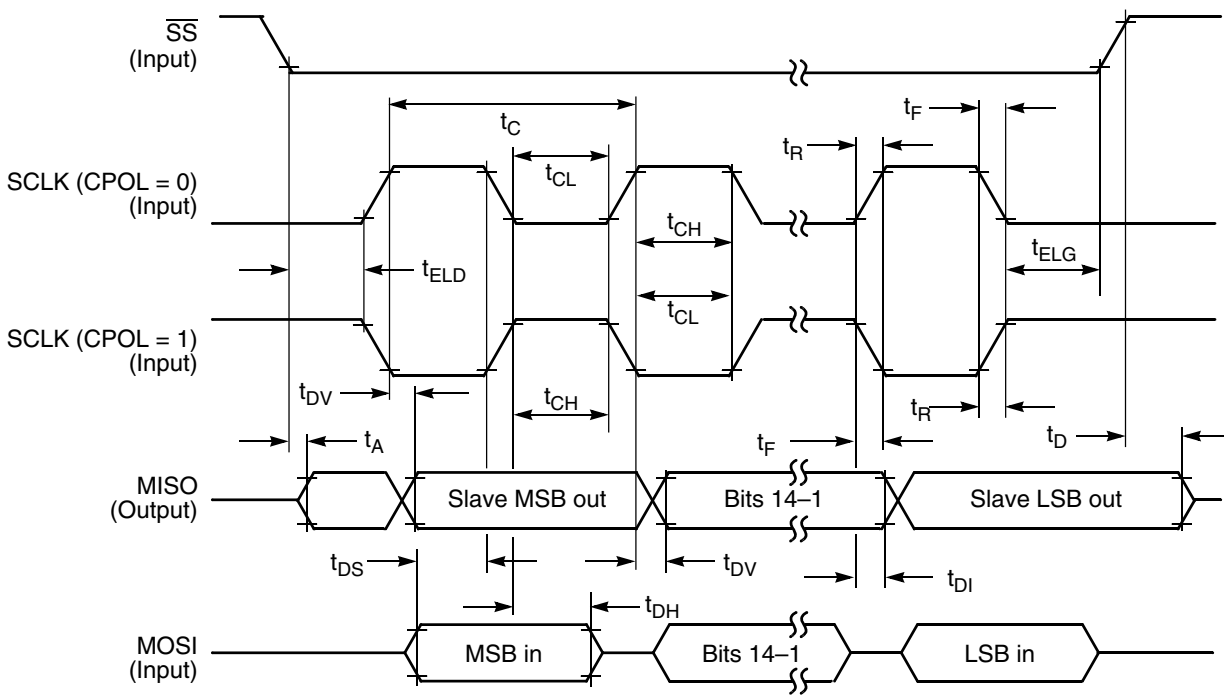


Figure 16. SPI slave timing (CPHA = 1)

Ψ_{JT} = hermal characterization parameter (°C/W)

P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51–2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

To determine the junction temperature of the device in the application when heat sinks are used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

9.2 Electrical design considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the device:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place 0.01–0.1 µF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible.

This leakage current could prevent operation of the device after it powers up. The voltage difference between VDD and VDDA must be limited to below 0.3 V at all times, to avoid permanent damage to the part (See Table 5). Also see Table 6.

9.3.2 Improperly designed protection circuit:

In many circuit designs, it is a general practice to add external clamping diodes on each analog input pin; see diode D1 and D2 in Figure 20, to prevent the surge voltage from damaging the analog input. However, in some cases, these diodes can cause the DSC to fail to start at power-on. For example, in Figure 20, the entire system is directly powered from the power grid; high voltage is fed to 12V DC/DC converter Reg1, then 12V powers DC/DC converter Reg2 and Reg3 to provide 3.3V supply voltage to VDD and VDDA. Due to the startup time delay of DC/DC converters and per-charge the capacitors on 12V and 3.3V rail, VDDA can be charged to a less than 0.5V through a path of R6->R5->R4->R2->D1. If this low voltage duration is more than 1 ms without continuing ramp-up, then it can cause the device to fail to start up.

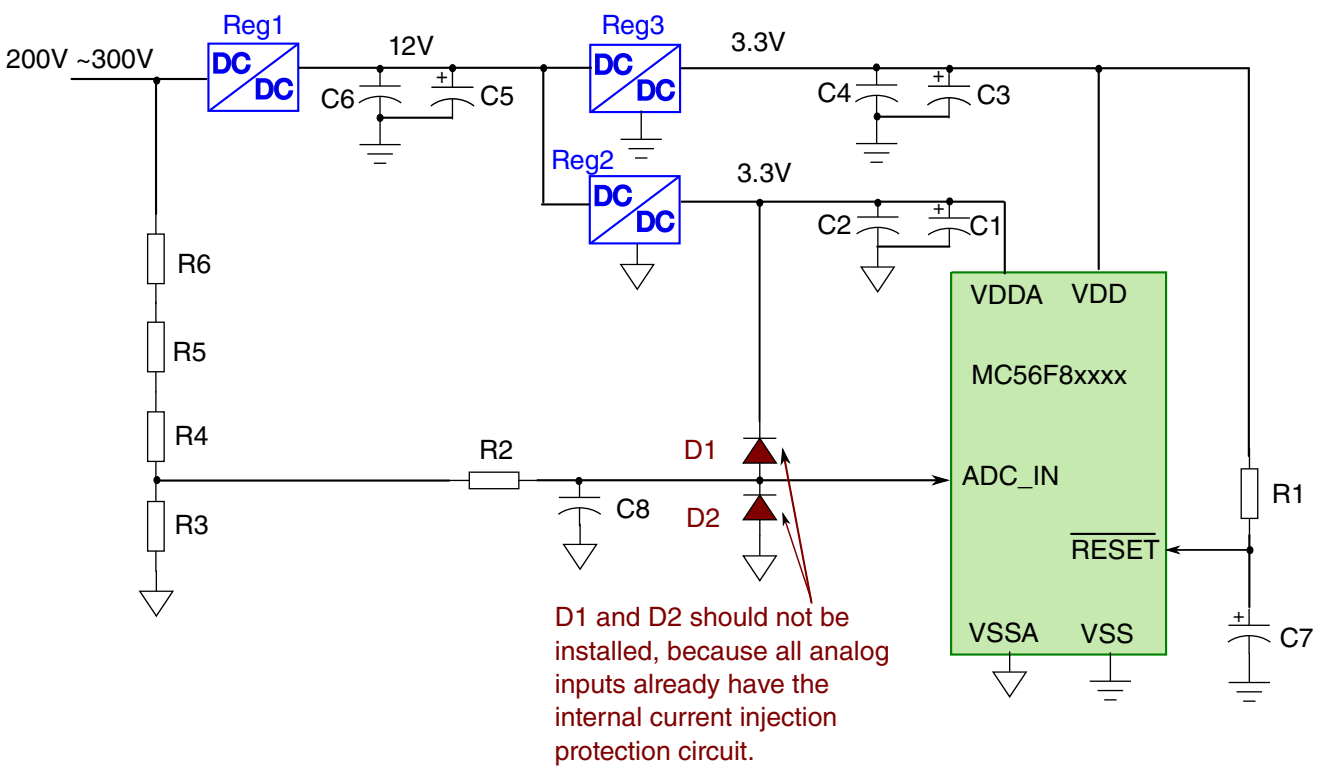


Figure 20. Protection Circuit Example

MC56F8xxxx DSC uses the 5V tolerance I/O. When the pin is configured to digital input, it can accept 5V input. Table 5. When the pin is configured to analog input, the internal integrated current injection protection circuit is enabled. The current injection protection

circuit performs the same functions as external clamp diode D1 and D2 in Figure 20. As long as the source or sink current for each analog pin is less than 3 mA, then there is no damage to the device. See Table 27.

This situation could happen if diodes D1 or D2 are used for clamping; therefore in this case, the D1 and D2 clamping diodes are not recommended to be used.

NOTE

In some designs, VDD and VDDA are powered from the same power supply. In this case, above analysis and suggestions are also applicatble.

9.3.3 Heavy capacitive load on power supply output:

In some applications, the low cost DC/DC converter may not regulate the output voltage well before it reaches the regulation point, which is roughly around 2.5V to 2.7V. However, the MC56F8xxxx DSC will exit power-on reset at around 2.3V. If the initialization code enables the PLL to run the DSC at full speed right after reset, then the high current will be pulled by DSC from the supply, which can cause the supply voltage to drop below the operation voltage; see the captured graph (Figure 21). This can cause the DSC fail to start up.

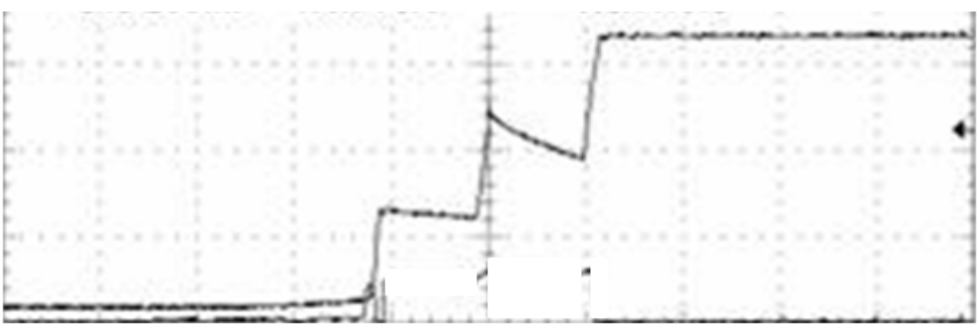


Figure 21. Supply Voltage Drop

A recommended initialization sequence during power-up is:

1. After POR is released, run a few hundred NOP instructions from the internal relaxation oscillator; this gives time for the supply voltage to stabilize.
2. Configure the peripherals (except the ADC) to the desired settings; the ADC should stay in low power mode.
3. Power up the PLL.
4. After the PLL locks, switch the clock from PLL prescale to postscale.
5. Configure the ADC.

10 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **freescale.com** and perform a keyword search for the drawing's document number:

Drawing for package	Document number to be used
32LQFP	98ASH70029A
32QFN	98ASA00473D
48-pin LQFP	98ASH00962A

11 Pinout

11.1 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The SIM's GPS registers are responsible for selecting which ALT functionality is available on most pins.

NOTE

- The RESETB pin is a 3.3 V pin only.
- If the GPIOC1 pin is used as GPIO, the XOSC should be powered down.
- Not all CMPD pins are not available on 48 LQFP.

NOTE

DAC and CMPC signals are not available on 32 LQFP package.

48 LQFP	32 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
—	19	GPIOF2	GPIOF2	SCL0	XB_OUT6		
—	20	GPIOF3	GPIOF3	SDA0	XB_OUT7		
1	1	TCK	TCK	GPIOD2			
2	2	RESETB	RESETB	GPIOD4			
3	—	GPIOC0	GPIOC0	EXTAL	CLKIN0		
4	—	GPIOC1	GPIOC1	XTAL			
5	3	GPIOC2	GPIOC2	TXD0	XB_OUT11	XB_IN2	CLKO0
6	4	GPIOC3	GPIOC3	TA0	CMPA_O	RXD0	CLKIN1

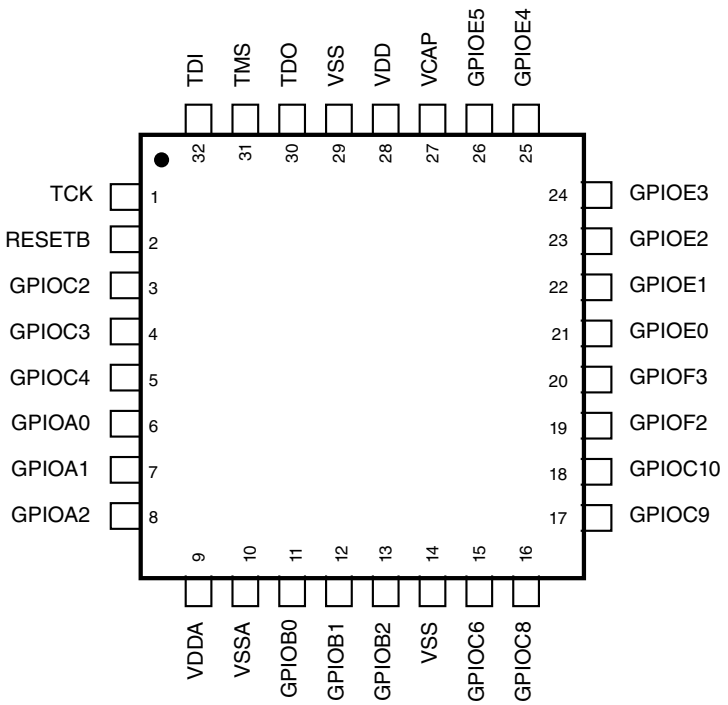


Figure 23. 32-pin LQFP and QFN

NOTE

The RESETB pin is a 3.3 V pin only.

12 Product documentation

The documents listed in Table 34 are required for a complete description and to successfully design using the device. Documentation is available from local NXP distributors, NXP sales offices, or online at **www.nxp.com**.

Table 34. Device documentation

Topic	Description	Document Number
DSP56800E/DSP56800EX Reference Manual	Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F823xx Reference Manual	Detailed functional description and programming model	MC56F823XXRM
MC56F823xx Data Sheet	Electrical and timing specifications, pin descriptions, and package information (this document)	MC56F823XX
MC56F82xxx Errata	Details any chip issues that might be present	MC56F82xxx_Errata

13 Revision History

The following table summarizes changes to this document since the release of the previous version.

Table 35. Revision History

Rev. No.	Date	Substantial Changes
2	10/2013	First public release
2.1	11/2013	• In Table 2, added DACB_O signal description. • In Obtaining package dimensions, changed 32-QFN's document number from '98ARE10566D' to '98ASA00473D'.

2.2	03/2016 - 05/2016	• In "12-bit ADC Electrical Specifications" table, corrected Max Gain Error to 0.990 to 1.010.
		• In Part identification section, in part number fields table, added the 32QFN package identifier.
		• In Electrical design considerations" section, added additional section "Power-on Reset design considerations".
		• Added new section "Power-on Reset design considerations".
		• In "Peripheral highlights" section, added
		  • Periodic Interrupt Timer (PIT) Modules
		  • External Watchdog Monitor (EWM)

3.0	09/2016	• Removed PDB (Programmable Delay Block) mentions, because PDBs are not present in these devices. • Moved "Signal groups" section under "MC56F823xx signal and pin descriptions" section. • In "Voltage and current operating ratings" section: updated note; in "Absolute Maximum Ratings" table, added Junction Temperature row, fixed broken footnotes. • In "Power consumption operating behaviors" section, in "Current Consumption" table: fixed broken footnotes; removed a footnote (#2). • In "Relaxation Oscillator Timing" section, in "Relaxation Oscillator Electrical Specifications" table: fixed broken footnotes, corrected and combined 2 footnotes.