Rohm Semiconductor - ML610Q435A-NNNTC03A7 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	nX-U8/100
Core Size	8-Bit
Speed	4.2MHz
Connectivity	I²C, SSP, UART/USART
Peripherals	LCD, Melody Driver, POR, PWM, WDT
Number of I/O	22
Program Memory Size	96KB (48K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 2x12b, 2x24b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/rohm-semi/ml610q435a-nnntc03a7

- LCD driver
  - Dot matrix can be supported.
    ML610Q435: 1024 dots max. (64 seg × 16 com)
    ML610Q436: 1536 dots max. (64 seg × 24 com)
  - 1/1 to 1/24 duty
  - 1/3 or 1/4 bias (built-in bias generation circuit)
  - Frame frequency selecable (approx. 64 Hz, 73 Hz, 85 Hz, and 102 Hz)
  - Bias voltage multiplying clock selectable (8 types)
  - Contrast adjustment (1/3 bias: 32 steps, 1/4 bias: 20 steps)
  - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
  - Programmable display allocation function (available only when 1/1~1/8 duty is selected)

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset when oscillation stop of the low-speed clock is detected
    (“A”version(ML610Q435A/Q436A) don’t have the oscilation stop function.)
  - Reset by the watchdog timer (WDT) overflow

- Power supply voltage detect function
  - Judgment voltages: One of 16 levels
  - Judgment accuracy: ±2% (Typ.)

- Clock
  - Low-speed clock: (This LSI can not guarantee the operation withoug low-speed clock)
    Crystal oscillation (32.768 kHz)
  - High-speed clock:
    Built-in RC oscillation (500 kHz)
    Built-in PLL oscillation (8.192 MHz ±TBD%), crystal/ceramic oscillation (4.096 MHz), external clock
  - Selection of high-speed clock mode by software:
    Built-in RC oscillation, built-in PLL oscillation, crystal/ceramic oscillation, external clock

- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Shipment
  - Chip
    ML610Q435-xxxWA (Blank product: ML610Q435-NNNWA)
    ML610Q436-xxxWA (Blank product: ML610Q436-NNNWA)
    ML610Q435A-xxxWA (Blank product: ML610Q435A-NNNWA)
    ML610Q436A-xxxWA (Blank product: ML610Q436A-NNNWA)
  - 144-pin plastic LQFP
    ML610Q435-xxxTCZ03A (Blank product: ML610Q435-NNNTCZ03A)
    ML610Q436-xxxTCZ03A (Blank product: ML610Q436-NNNTCZ03A)
    ML610Q435A-xxxTCZ03A (Blank product: ML610Q435A-NNNTCZ03A)
    ML610Q436A-xxxTCZ03A (Blank product: ML610Q436A-NNNTCZ03A)
    xxx: ROM code number

- Guaranteed operating range
  - Operating temperature: –20°C to 70°C
  - Operating voltage: V_{DD} = 1.1V to 3.6V, AV_{DD} = 2.2V to 3.6V

ML610Q436 Block Diagram

Figure 2 show the block diagram of the ML610Q436.
"*" indicates the secondary function of each port.

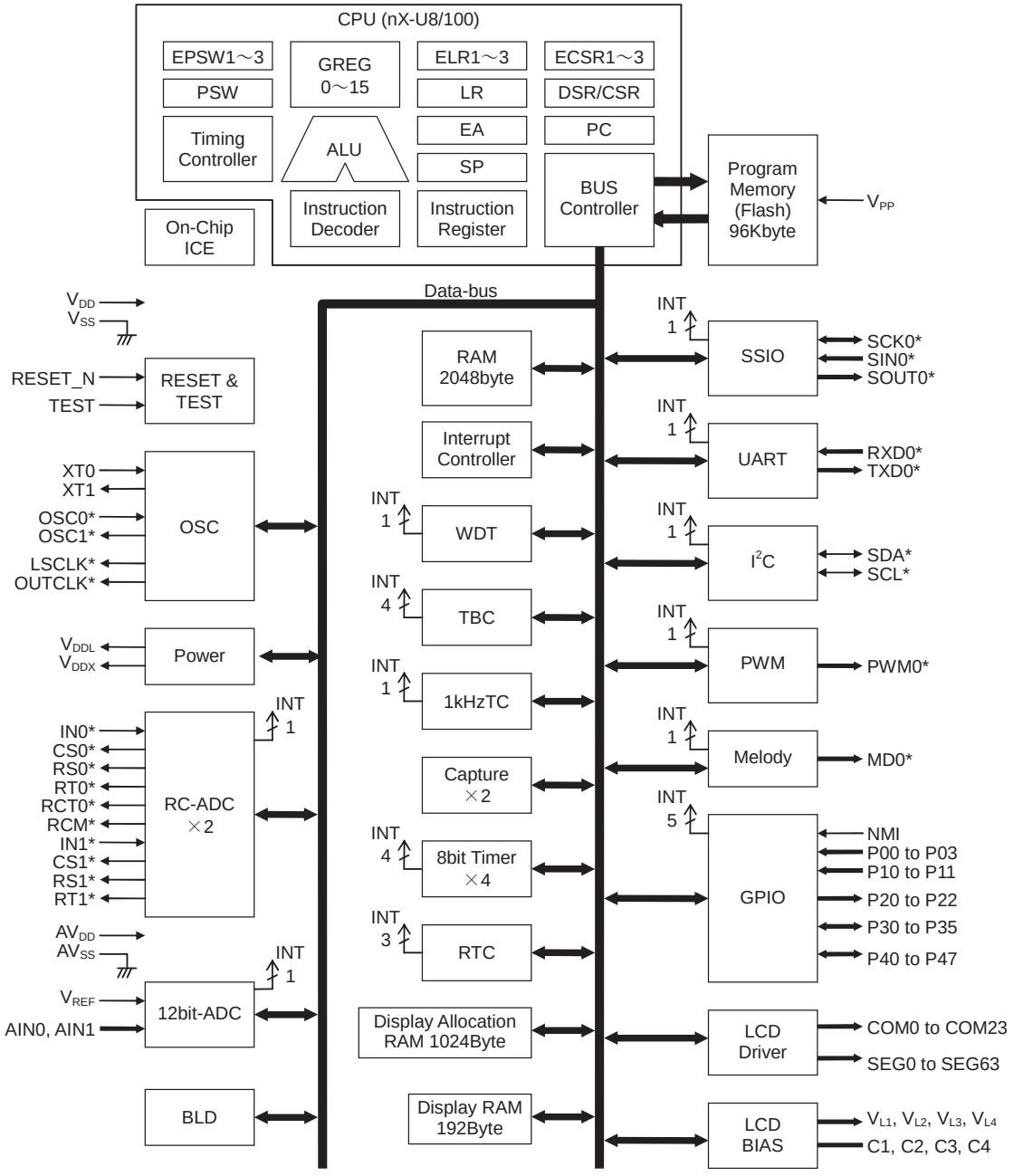
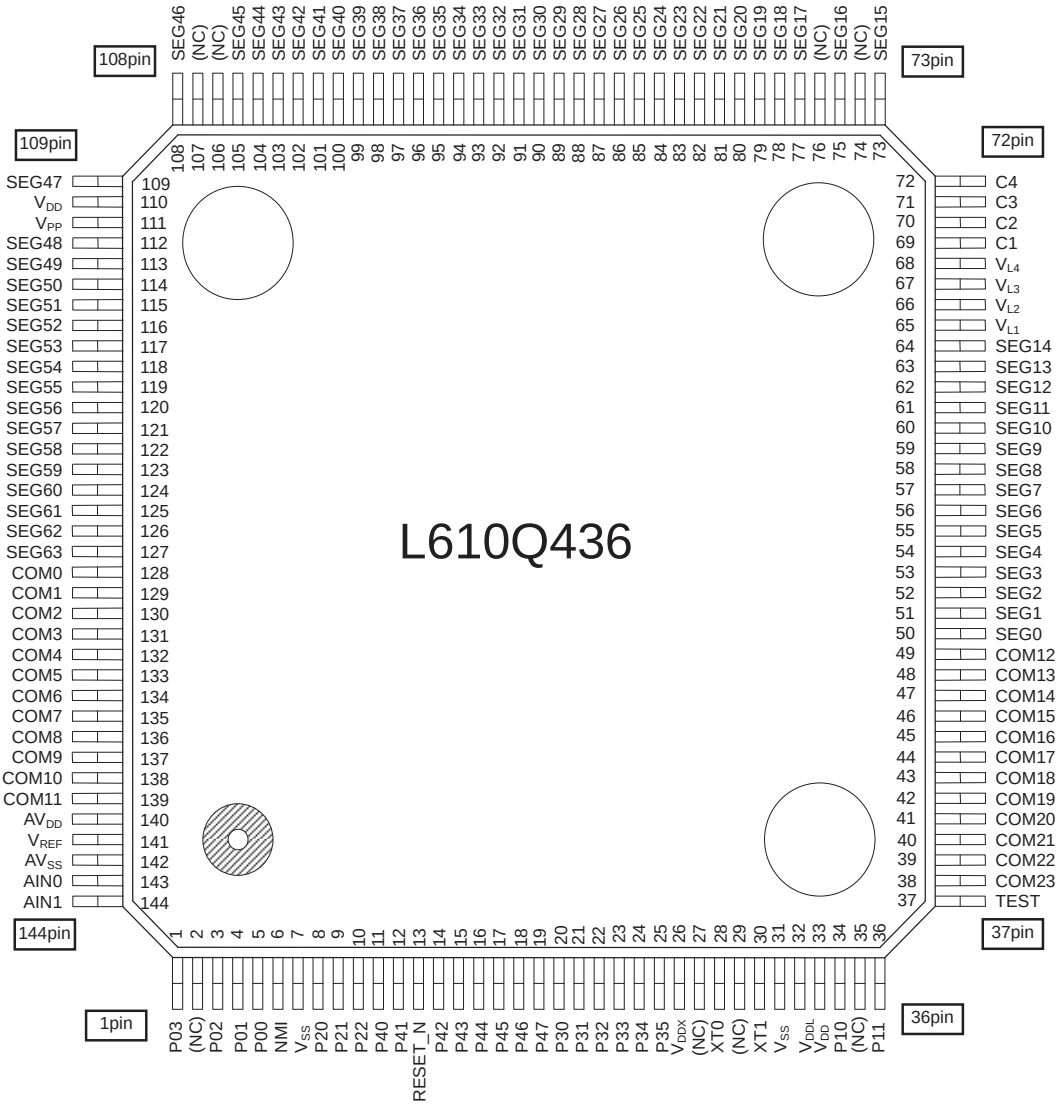


Figure 2 ML610Q436 Block Diagram

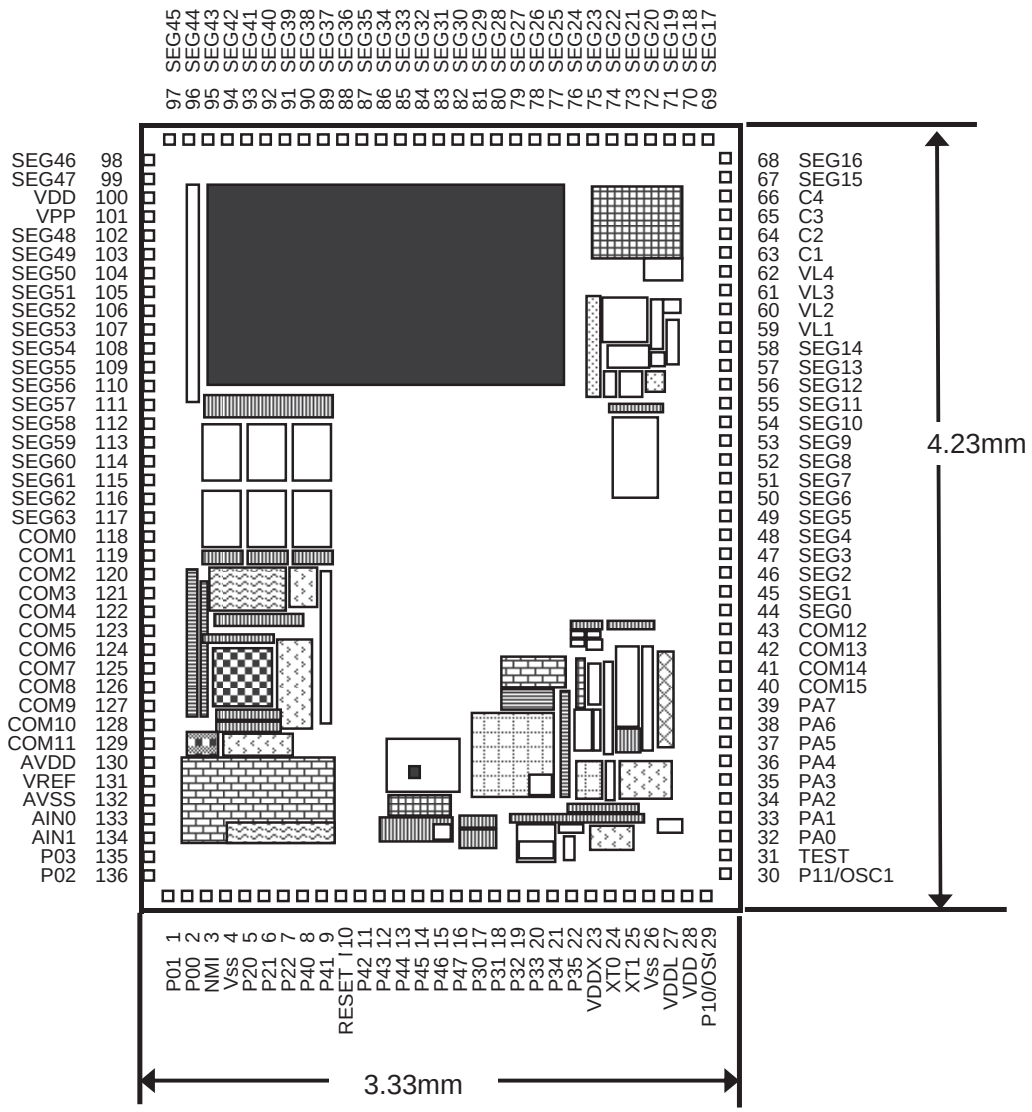
ML610Q436 LQFP144 Pin Layout



(NC): No Connection

Figure 4 ML610Q436 LQFP144 Pin Configuration

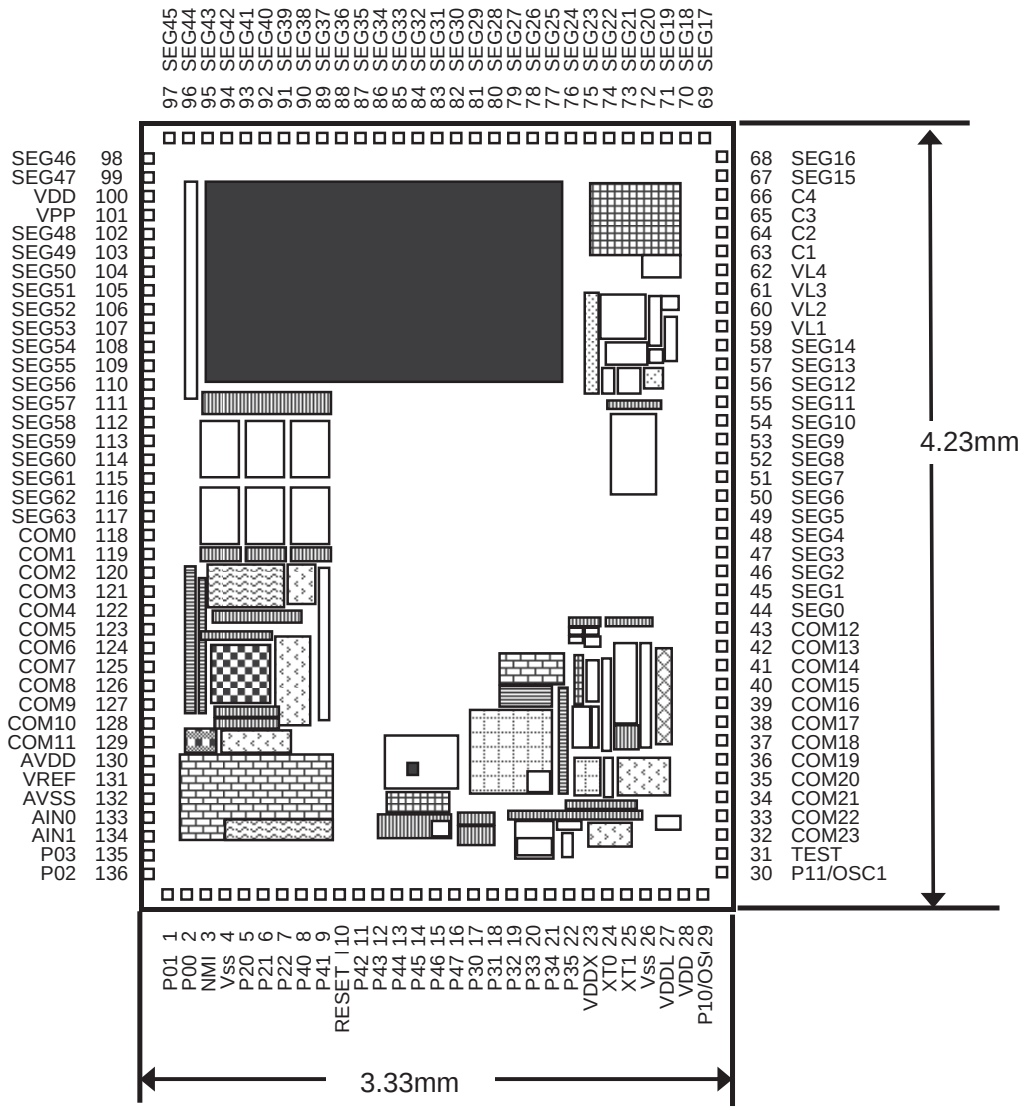
ML610Q435 Chip Pin Layout & Dimension



Chip size:	3.33 mm × 4.23 mm
PAD count:	136 pins
Minimum PAD pitch:	100 μm
PAD aperture:	80 μm × 80 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 5 ML610Q435 Chip Layout & Dimension

ML610Q436 Chip Pin Layout & Dimension



Chip size:	3.33 mm × 4.23 mm
PAD count:	136 pins
Minimum PAD pitch:	100 μm
PAD aperture:	80 μm × 80 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 6 ML610Q436 Chip Layout & Dimension

ML610Q435 Pad Coordinates

Table 1 ML610Q435 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)
1	P01	-1400	-1978	51	SEG7	1528	200	101	V_{PP}	-1528	1600
2	P00	-1300	-1978	52	SEG8	1528	300	102	SEG48	-1528	1500
3	NMI	-1200	-1978	53	SEG9	1528	400	103	SEG49	-1528	1400
4	V_{SS}	-1100	-1978	54	SEG10	1528	500	104	SEG50	-1528	1300
5	P20	-1000	-1978	55	SEG11	1528	600	105	SEG51	-1528	1200
6	P21	-900	-1978	56	SEG12	1528	700	106	SEG52	-1528	1100
7	P22	-800	-1978	57	SEG13	1528	800	107	SEG53	-1528	1000
8	P40	-700	-1978	58	SEG14	1528	900	108	SEG54	-1528	900
9	P41	-600	-1978	59	V_{L1}	1528	1000	109	SEG55	-1528	800
10	RESET_N	-500	-1978	60	V_{L2}	1528	1100	110	SEG56	-1528	700
11	P42	-400	-1978	61	V_{L3}	1528	1200	111	SEG57	-1528	600
12	P43	-300	-1978	62	V_{L4}	1528	1300	112	SEG58	-1528	500
13	P44	-200	-1978	63	C1	1528	1400	113	SEG59	-1528	400
14	P45	-100	-1978	64	C2	1528	1500	114	SEG60	-1528	300
15	P46	0	-1978	65	C3	1528	1600	115	SEG61	-1528	200
16	P47	100	-1978	66	C4	1528	1700	116	SEG62	-1528	100
17	P30	200	-1978	67	SEG15	1528	1800	117	SEG63	-1528	0
18	P31	300	-1978	68	SEG16	1528	1900	118	COM0	-1528	-100
19	P32	400	-1978	69	SEG17	1400	1978	119	COM1	-1528	-200
20	P33	500	-1978	70	SEG18	1300	1978	120	COM2	-1528	-300
21	P34	600	-1978	71	SEG19	1200	1978	121	COM3	-1528	-400
22	P35	700	-1978	72	SEG20	1100	1978	122	COM4	-1528	-500
23	V_{DDX}	800	-1978	73	SEG21	1000	1978	123	COM5	-1528	-600
24	XT0	900	-1978	74	SEG22	900	1978	124	COM6	-1528	-700
25	XT1	1000	-1978	75	SEG23	800	1978	125	COM7	-1528	-800
26	V_{SS}	1100	-1978	76	SEG24	700	1978	126	COM8	-1528	-900
27	V_{DDL}	1200	-1978	77	SEG25	600	1978	127	COM9	-1528	-1000
28	V_{DD}	1300	-1978	78	SEG26	500	1978	128	COM10	-1528	-1100
29	P10	1400	-1978	79	SEG27	400	1978	129	COM11	-1528	-1200
30	P11	1528	-1900	80	SEG28	300	1978	130	A_{VDD}	-1528	-1300
31	TEST	1528	-1800	81	SEG29	200	1978	131	V_{REF}	-1528	-1400
32	PA0	1528	-1700	82	SEG30	100	1978	132	A_{VSS}	-1528	-1500
33	PA1	1528	-1600	83	SEG31	0	1978	133	AIN0	-1528	-1600
34	PA2	1528	-1500	84	SEG32	-100	1978	134	AIN1	-1528	-1700
35	PA3	1528	-1400	85	SEG33	-200	1978	135	P03	-1528	-1800
36	PA4	1528	-1300	86	SEG34	-300	1978	136	P02	-1528	-1900
37	PA5	1528	-1200	87	SEG35	-400	1978				
38	PA6	1528	-1100	88	SEG36	-500	1978				
39	PA7	1528	-1000	89	SEG37	-600	1978				
40	COM15	1528	-900	90	SEG38	-700	1978				
41	COM14	1528	-800	91	SEG39	-800	1978				
42	COM13	1528	-700	92	SEG40	-900	1978				
43	COM12	1528	-600	93	SEG41	-1000	1978				
44	SEG0	1528	-500	94	SEG42	-1100	1978				
45	SEG1	1528	-400	95	SEG43	-1200	1978				
46	SEG2	1528	-300	96	SEG44	-1300	1978				
47	SEG3	1528	-200	97	SEG45	-1400	1978				
48	SEG4	1528	-100	98	SEG46	-1528	1900				
49	SEG5	1528	0	99	SEG47	-1528	1800				
50	SEG6	1528	100	100	V_{DD}	-1528	1700				

ML610Q436 Pad Coordinates

Table 2 ML610Q436 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)
1	P01	-1400	-1978	51	SEG7	1528	200	101	V_{PP}	-1528	1600
2	P00	-1300	-1978	52	SEG8	1528	300	102	SEG48	-1528	1500
3	NMI	-1200	-1978	53	SEG9	1528	400	103	SEG49	-1528	1400
4	V_{SS}	-1100	-1978	54	SEG10	1528	500	104	SEG50	-1528	1300
5	P20	-1000	-1978	55	SEG11	1528	600	105	SEG51	-1528	1200
6	P21	-900	-1978	56	SEG12	1528	700	106	SEG52	-1528	1100
7	P22	-800	-1978	57	SEG13	1528	800	107	SEG53	-1528	1000
8	P40	-700	-1978	58	SEG14	1528	900	108	SEG54	-1528	900
9	P41	-600	-1978	59	V_{L1}	1528	1000	109	SEG55	-1528	800
10	RESET_N	-500	-1978	60	V_{L2}	1528	1100	110	SEG56	-1528	700
11	P42	-400	-1978	61	V_{L3}	1528	1200	111	SEG57	-1528	600
12	P43	-300	-1978	62	V_{L4}	1528	1300	112	SEG58	-1528	500
13	P44	-200	-1978	63	C1	1528	1400	113	SEG59	-1528	400
14	P45	-100	-1978	64	C2	1528	1500	114	SEG60	-1528	300
15	P46	0	-1978	65	C3	1528	1600	115	SEG61	-1528	200
16	P47	100	-1978	66	C4	1528	1700	116	SEG62	-1528	100
17	P30	200	-1978	67	SEG15	1528	1800	117	SEG63	-1528	0
18	P31	300	-1978	68	SEG16	1528	1900	118	COM0	-1528	-100
19	P32	400	-1978	69	SEG17	1400	1978	119	COM1	-1528	-200
20	P33	500	-1978	70	SEG18	1300	1978	120	COM2	-1528	-300
21	P34	600	-1978	71	SEG19	1200	1978	121	COM3	-1528	-400
22	P35	700	-1978	72	SEG20	1100	1978	122	COM4	-1528	-500
23	V_{DDX}	800	-1978	73	SEG21	1000	1978	123	COM5	-1528	-600
24	XT0	900	-1978	74	SEG22	900	1978	124	COM6	-1528	-700
25	XT1	1000	-1978	75	SEG23	800	1978	125	COM7	-1528	-800
26	V_{SS}	1100	-1978	76	SEG24	700	1978	126	COM8	-1528	-900
27	V_{DDL}	1200	-1978	77	SEG25	600	1978	127	COM9	-1528	-1000
28	V_{DD}	1300	-1978	78	SEG26	500	1978	128	COM10	-1528	-1100
29	P10	1400	-1978	79	SEG27	400	1978	129	COM11	-1528	-1200
30	P11	1528	-1900	80	SEG28	300	1978	130	A_{VDD}	-1528	-1300
31	TEST	1528	-1800	81	SEG29	200	1978	131	V_{REF}	-1528	-1400
32	COM23	1528	-1700	82	SEG30	100	1978	132	A_{VSS}	-1528	-1500
33	COM22	1528	-1600	83	SEG31	0	1978	133	AIN0	-1528	-1600
34	COM21	1528	-1500	84	SEG32	-100	1978	134	AIN1	-1528	-1700
35	COM20	1528	-1400	85	SEG33	-200	1978	135	P03	-1528	-1800
36	COM19	1528	-1300	86	SEG34	-300	1978	136	P02	-1528	-1900
37	COM18	1528	-1200	87	SEG35	-400	1978				
38	COM17	1528	-1100	88	SEG36	-500	1978				
39	COM16	1528	-1000	89	SEG37	-600	1978				
40	COM15	1528	-900	90	SEG38	-700	1978				
41	COM14	1528	-800	91	SEG39	-800	1978				
42	COM13	1528	-700	92	SEG40	-900	1978				
43	COM12	1528	-600	93	SEG41	-1000	1978				
44	SEG0	1528	-500	94	SEG42	-1100	1978				
45	SEG1	1528	-400	95	SEG43	-1200	1978				
46	SEG2	1528	-300	96	SEG44	-1300	1978				
47	SEG3	1528	-200	97	SEG45	-1400	1978				
48	SEG4	1528	-100	98	SEG46	-1528	1900				
49	SEG5	1528	0	99	SEG47	-1528	1800				
50	SEG6	1528	100	100	V_{DD}	-1528	1700				

PIN LIST

PAD No.		Primary function			Secondary function			Tertiary function		
Q435	Q436	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
4,26	4,26	Vss	—	Negative power supply pin	—	—	—	—	—	—
28, 100	28, 100	V_{DD}	—	Positive power supply pin	—	—	—	—	—	—
27	27	V_{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—	—	—
23	23	V_{DDX}	—	Power supply pin for low-speed oscillation (internally generated)	—	—	—	—	—	—
101	101	V_{PP}	—	Power supply pin for Flash ROM	—	—	—	—	—	—
132	132	AV_{SS}	—	Negative power supply pin for successive approximation type ADC	—	—	—	—	—	—
130	130	AV_{DD}	—	Positive power supply pin for successive approximation type ADC	—	—	—	—	—	—
59	59	V_{L1}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
60	60	V_{L2}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
61	61	V_{L3}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
62	62	V_{L4}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
63	63	C1	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
64	64	C2	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
65	65	C3	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
66	66	C4	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
31	31	TEST	I/O	Input/output pin for testing	—	—	—	—	—	—
10	10	RESET_N	I	Reset input pin	—	—	—	—	—	—
24	24	XT0	I	Low-speed clock oscillation pin	—	—	—	—	—	—
25	25	XT1	O	Low-speed clock oscillation pin	—	—	—	—	—	—
131	131	V_{REF}	—	Reference power supply pin for successive approximation type ADC	—	—	—	—	—	—

PAD No.		Primary function			Secondary function			Tertiary function		
Q435	Q436	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
133	133	AIN0	I	Successive approximation type ADC input	—	—	—	—	—	—
134	134	AIN1	I	Successive approximation type ADC input	—	—	—	—	—	—
3	3	NMI	I	Non-maskable interrupt pin	—	—	—	—	—	—
2	2	P00/EXI 0/CAP0	I	Input port, External interrupt 0, Capture 0 input	—	—	—	—	—	—
1	1	P01/EXI 1/CAP1	I	Input port, External interrupt 1, Capture 1 input	—	—	—	—	—	—
136	136	P02/EXI 2/RXD0	I	Input port, External interrupt 2, UART0 receive	—	—	—	—	—	—
135	135	P03/EXI 3	I	Input port, External interrupt 3	—	—	—	—	—	—
29	29	P10	I	Input port	OSC0	I	High-speed oscillation	—	—	—
30	30	P11	I	Input port	OSC1	O	High-speed oscillation	—	—	—
5	5	P20/LE D0	O	Output port	LSCLK	O	Low-speed clock output	—	—	—
6	6	P21LED 1	O	Output port	OUTCLK	O	High-speed clock output	—	—	—
7	7	P22/LE D2	O	Output port	MD0	O	Melody output	—	—	—
17	17	P30	I/O	Input/output port	IN0	I	RC type ADC0 oscillation input pin	—	—	—
18	18	P31	I/O	Input/output port	CS0	O	RC type ADC0 reference capacitor connection pin	—	—	—
19	19	P32	I/O	Input/output port	RS0	O	RC type ADC0 reference resistor connection pin	—	—	—
20	20	P33	I/O	Input/output port	RT0	O	RC type ADC0 resistor sensor connection pin	—	—	—
21	21	P34	I/O	Input/output port	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin	PWM0	O	PWM output
22	22	P35	I/O	Input/output port	RCM	O	RC type ADC oscillation monitor	—	—	—
8	8	P40	I/O	Input/output port	SDA	I/O	I^2C data input/output	SIN0	I	SSIO data input
9	9	P41	I/O	Input/output port	SCL	I/O	I^2C clock input/output	SCK0	I/O	SSIO synchronous clock
11	11	P42	I/O	Input/output port	RXD0	I	UART data input	SOUT0	O	SSIO data output
12	12	P43	I/O	Input/output port	TXD0	O	UART data output	PWM0	O	PWM output
13	13	P44/T02 P0CK	I/O	Input/output port, Timer 0/Timer 2/PWM0 external clock input	IN1	I	RC type ADC1 oscillation input pin	SIN0	I	SSIO0 data input
14	14	P45/T13 P1CK	I/O	Input/output port, Timer 1/Timer 3 external clock input	CS1	O	RC type ADC1 reference capacitor connection pin	SCK0	I/O	SSIO0 synchronous clock
15	15	P46	I/O	Input/output port	RS1	O	RC type ADC1 reference resistor connection pin	SOUT0	O	SSIO0 data output
16	16	P47	I/O	Input/output port	RT1	O	RC type ADC1 resistor sensor connection pin	—	—	—
—	32	PA0	I/O	Input/output port	—	—	—	—	—	—
—	33	PA1	I/O	Input/output port	—	—	—	—	—	—
—	34	PA2	I/O	Input/output port	—	—	—	—	—	—
—	35	PA3	I/O	Input/output port	—	—	—	—	—	—
—	36	PA4	I/O	Input/output port	—	—	—	—	—	—
—	37	PA5	I/O	Input/output port	—	—	—	—	—	—

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock.	—	—
XT1	O	A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V_{SS} as required.	—	—
OSC0	I	Crystal/ceramic connection pin for high-speed clock.	Secondary	—
OSC1	O	A crystal or ceramic is connected to this pin (4.1 MHz max.). Capacitors CDH and CGH (see measuring circuit 1) are connected across this pin and V_{SS}. This pin is used as the secondary function of the P10 pin(OSC0) and P11 pin(OSC1).	Secondary	—
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00-P03	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P10-P11	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose output port				
P20-P22	O	General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30-P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
PA0-PA7	I/O	General-purpose input/output port. These pins are for the ML610Q435, but are not provided in the ML610Q436.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/Secondary	Positive
I^2C bus interface				
SDA	I/O	I^2C data input/output pin. This pin is used as the secondary function of the P40 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
SCL	O	I^2C clock output pin. This pin is used as the secondary function of the P41 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
Synchronous serial (SSIO)				
SCK0	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin.	Tertiary	—
SIN0	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44 pin.	Tertiary	Positive
SOUT0	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin.	Tertiary	Positive
PWM				
PWM0	O	PWM0 output pin. This pin is used as the tertiary function of the P43 or P34 pin.	Tertiary	Positive
T02P0CK	I	PWM0 external clock input pin. This pin is used as the primary function of the P44 pin.	Primary	—
External interrupt				
NMI	I	External non-maskable interrupt input pin. An interrupt is generated on both edges.	Primary	Positive/ negative
EXI0-3	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P03 pins.	Primary	Positive/ negative
Capture				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software. These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	Positive/ negative
CAP1	I		Primary	Positive/ negative
Timer				
T02P0CK	I	External clock input pin used for both Timer 0 and Timer 2. The clocks for these timers are selected by software. This pin is used as the primary function of the P44 pin.	Primary	—
T13P1CK	I	External clock input pin used for both Timer 1 and Timer 3. The clocks for these timers are selected by software. This pin is used as the primary function of the P45 pin.	Primary	—
Melody				
MD0	O	Melody/buzzer signal output pin. This pin is used as the secondary function of the P22 pin.	Secondary	Positive/ negative
LED drive				
LED0-2	O	NMOS open drain output pins to drive LED. These pins are used as the primary function of the P20-P22 pins.	Primary	Positive/ negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
RC oscillation type A/D converter				
IN0	I	Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin.	Secondary	—
CS0	O	Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin.	Secondary	—
RS0	O	This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0.	Secondary	—
RT0	O	Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin.	Secondary	—
RCT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin.	Secondary	—
RCM	O	RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.	Secondary	—
IN1	I	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	—
CS1	O	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	—
RS1	O	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	—
RT1	O	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—
Successive approximation type A/D converter				
AV_{SS}	—	Negative power supply pin for successive approximation type A/D converter.	—	—
AV_{DD}	—	Positive power supply pin for successive approximation type A/D converter.	—	—
V_{REF}	—	Reference power supply pin for successive approximation type A/D converter.	—	—
AIN0	I	Channel 0 analog input for successive approximation type A/D converter.	—	—
AIN1	I	Channel 1 analog input for successive approximation type A/D converter.	—	—
LCD drive signal				
COM0-15	O	Common output pins.	—	—
COM16-23	O	Common output pins. These pins are for the ML610Q436, but are not provided in the ML610Q435.	—	—
SEG0-63	O	Segment output pin.	—	—
LCD driver power supply				
V_{L1}	—	Power supply pins for LCD bias (internally generated). Capacitors Ca, Cb, Cc, and Cd (see measuring circuit 1) are connected between V_{SS} and V_{L1}, V_{L2}, V_{L3}, and V_{L4}, respectively.	—	—
V_{L2}	—		—	—
V_{L3}	—		—	—
V_{L4}	—		—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitors C12 and C34 (see measuring circuit 1) are connected between C1 and C2 and between C3 and C4, respectively.	—	—
C2	—		—	—
C3	—		—	—
C4	—		—	—
For testing				
TEST	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	—	—
Power supply				
V_{SS}	—	Negative power supply pin.	—	—
V_{DD}	—	Positive power supply pin.	—	—
V_{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitors CL0 and CL1 (see measuring circuit 1) are connected between this pin and V_{SS}.	—	—
V_{DDX}	—	Plus-side power supply pin (internally generated) for low-speed oscillation. Capacitor Cx (see measuring circuit 1) is connected between this pin and V_{SS}.	—	—
V_{PP}	—	Power supply pin for programming Flash ROM. A pull-up resistor is internally connected.	—	—

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	–0.3 to +4.6	V
Power supply voltage 2	AV_{DD}	Ta = 25°C	–0.3 to +4.6	V
Power supply voltage 3	V_{PP}	Ta = 25°C	–0.3 to +9.5	V
Power supply voltage 4	V_{DDL}	Ta = 25°C	–0.3 to +3.6	V
Power supply voltage 5	V_{DDX}	Ta = 25°C	–0.3 to +3.6	V
Power supply voltage 6	V_{L1}	Ta = 25°C	–0.3 to +1.75	V
Power supply voltage 7	V_{L2}	Ta = 25°C	–0.3 to +3.5	V
Power supply voltage 8	V_{L3}	Ta = 25°C	–0.3 to +5.25	V
Power supply voltage 9	V_{L4}	Ta = 25°C	–0.3 to +7.0	V
Input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port3–A, Ta = 25°C	–12 to +11	mA
Output current 2	I_{OUT2}	Port2, Ta = 25°C	–12 to +20	mA
Power dissipation	PD	Ta = 25°C	122	mW
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	–20 to +70	°C
Operating voltage	V_{DD}	—	1.1 to 3.6	V
	AV_{DD}	—	2.2 to 3.6	
Operating frequency (CPU)	f_{OP}	V_{DD} = 1.1 to 3.6V	30k to 36k	Hz
		V_{DD} = 1.3 to 3.6V	30k to 650k	
		V_{DD} = 1.8 to 3.6V	30k to 4.2M	
Low-speed crystal oscillation frequency	f_{XTL}	—	32.768k	Hz
Low-speed crystal oscillation external capacitor	C_{DL}	—	0 to 12	pF
	C_{GL}	—	0 to 12	
High-speed crystal/ceramic oscillation frequency	f_{XTH}	—	4.0M / 4.096M	Hz
High-speed crystal oscillation external capacitor	C_{DH}	—	24	pF
	C_{GH}	—	24	
Capacitor externally connected to V_{DDL} pin	C_{L0}	—	1.0±30%	µF
	C_{L1}	—	0.1±30%	
Capacitor externally connected to V_{DDX} pin	C_X	—	0.1±30%	µF
Capacitors externally connected to $V_{L1, 2, 3, 4}$ pins	$C_{a, b, c, d}$	—	1.0±30%	µF
Capacitors externally connected across C1 and C2 pins and across C3 and C4 pins	C_{12}, C_{34}	—	1.0±30%	µF

DC CHARACTERISTICS (2/5)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified) (2/5)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
V_{L1} voltage	V_{L1}	V_{DD} = 3.0V, Tj = 25°C	CN4–0 = 00H	0.89	0.94	0.99	V	1
			CN4–0 = 01H	0.91	0.96	1.01		
			CN4–0 = 02H	0.93	0.98	1.03		
			CN4–0 = 03H	0.95	1.00	1.05		
			CN4–0 = 04H	0.97	1.02	1.07		
			CN4–0 = 05H	0.99	1.04	1.09		
			CN4–0 = 06H	1.01	1.06	1.11		
			CN4–0 = 07H	1.03	1.08	1.13		
			CN4–0 = 08H	1.05	1.10	1.15		
			CN4–0 = 09H	1.07	1.12	1.17		
			CN4–0 = 0AH	1.09	1.14	1.19		
			CN4–0 = 0BH	1.11	1.16	1.21		
			CN4–0 = 0CH	1.13	1.18	1.23		
			CN4–0 = 0DH	1.15	1.20	1.25		
			CN4–0 = 0EH	1.17	1.22	1.27		
			CN4–0 = 0FH	1.19	1.24	1.29		
			CN4–0 = 10H	1.21	1.26	1.31		
			CN4–0 = 11H	1.23	1.28	1.33		
			CN4–0 = 12H	1.25	1.30	1.35		
			CN4–0 = 13H	1.27	1.32	1.37		
			CN4–0 = 14H *1	1.29	1.34	1.39		
			CN4–0 = 15H *1	1.31	1.36	1.41		
			CN4–0 = 16H *1	1.33	1.38	1.43		
			CN4–0 = 17H *1	1.35	1.40	1.45		
			CN4–0 = 18H *1	1.37	1.42	1.47		
			CN4–0 = 19H *1	1.39	1.44	1.49		
			CN4–0 = 1AH *1	1.41	1.46	1.51		
			CN4–0 = 1BH *1	1.43	1.48	1.53		
			CN4–0 = 1CH *1	1.45	1.50	1.55		
			CN4–0 = 1DH *1	1.47	1.52	1.57		
			CN4–0 = 1EH *1	1.49	1.54	1.59		
			CN4–0 = 1FH *1	1.51	1.56	1.61		
V_{L1} temperature deviation	ΔV_{L1}	V_{DD} = 3.0V		—	–1.5	—	mV/°C	
V_{L1} voltage dependency	ΔV_{L1}	V_{DD} = 1.3 to 3.6V		—	5	20	mV/V	
V_{L2} voltage	V_{L2}	V_{DD} = 3.0V, Tj = 25°C, 300kΩ load (V_{L4}–V_{SS})		Typ. –10%	V_{L1}×2	Typ. +4%	V	
V_{L3} voltage	V_{L3}	V_{DD} = 3.0V, Tj = 25°C, 300kΩ load (V_{L4}–V_{SS})	1/3 bias	Typ. –10%	V_{L1}×2	Typ. +4%		
			1/4 bias		V_{L1}×3			
V_{L4} voltage	V_{L4}		1/3 bias	Typ. –10%	V_{L1}×3	Typ. +5%		
			1/4 bias		V_{L1}×4			
LCD bias voltage generation time	T_{BIAS}	—		—	—	600	ms	

*1: When using 1/4 bias, the V_{L1} voltage is set to typ. 1.32 V (same voltage as in CN4–0 = 13H).

DC CHARACTERISTICS (3/5)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified) (3/5)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
BLD threshold voltage	V_{BLD}	V_{DD} = 1.35 to 3.6V	LD2–0 = 0H	Typ. –2%	1.35	Typ. +2%	V	1
			LD2–0 = 1H		1.4			
			LD2–0 = 2H		1.45			
			LD2–0 = 3H		1.5			
			LD2–0 = 4H		1.6			
			LD2–0 = 5H		1.7			
			LD2–0 = 6H		1.8			
			LD2–0 = 7H		1.9			
			LD2–0 = 8H		2.0			
			LD2–0 = 9H		2.1			
			LD2–0 = 0AH		2.2			
			LD2–0 = 0BH		2.3			
			LD2–0 = 0CH		2.4			
			LD2–0 = 0DH		2.5			
			LD2–0 = 0EH		2.7			
			LD2–0 = 0FH		2.9			
BLD threshold voltage temperature deviation	ΔV_{BLD}	V_{DD} = 1.35 to 3.6V		—	0.1	—	%/°C	
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped.	Ta = 25°C	—	0.15	0.50	μA	
			Ta = -20 to +70°C	—	—	2.50		
Supply current 2	IDD2	CPU: In HALT state (LTBC, RTC: Operating*3*5). High-speed oscillation: Stopped. LCD/BIAS circuits: Stopped.	Ta = 25°C	—	0.5	1.3	μA	
			Ta = -20 to +70°C	—	—	3.5		
Supply current 3	IDD3	CPU: In 32.768kHz operating state.*1*3 High-speed oscillation: Stopped. LCD/BIAS circuits: Operating.*2	Ta = 25°C	—	5	7	μA	
			Ta = -20 to +70°C	—	—	12		
Supply current 4	IDD4	CPU: In 500kHz CR operating state. LCD/BIAS circuits: Operating.*2	Ta = 25°C	—	70	85	μA	
			Ta = -20 to +70°C	—	—	100		
Supply current 5	IDD5	CPU: In 4.096MHz operating state.*2*3 PLL: In oscillating state. LCD/BIAS circuits: Operating. *2 V_{DD} = 1.8 to 3.6V	Ta = 25°C	—	0.8	1.0	mA	
			Ta = -20 to +70°C	—	—	1.2		
Supply current 6	IDD6	CPU: In 4.096MHz operating state.*2 PLL: In oscillating state. *3*4 A/D: In operating state. LCD/BIAS circuits: Operating. *2 V_{DD} = AV_{DD} = 3.0V	Ta = 25°C	—	1.5	1.6	mA	
			Ta = -20 to +70°C	—	—	2.5		

*1: When the CPU operating rate is 100% (No HALT state).
*2: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)
*3 : Use 32.768KHz Crystal Oscillator C-001R (Epson Toyocom) with capacitance C_{GL}/C_{DL}=0pF.
*4 : Use 4.096MHz Crystal Oscillator HC49SFWB (Kyocera).
*5 : Significant bits of BLKCON0~BLKCON4 registers are all “1”.

DC CHARACTERISTICS (4/5)

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified) (4/5)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Output voltage 1 (P20–P22/2nd function is selected) (P30–P35) (P40–P47) (PA0–PA7)*1	VOH1	IOH1 = –0.5mA, V_{DD} = 1.8 to 3.6V		V_{DD} –0.5	—	—	V	2
		IOH1 = -0.1mA, V_{DD} = 1.3 to 3.6V		V_{DD} –0.3	—	—		
		IOH1 = -0.03mA, V_{DD} = 1.1 to 3.6V		V_{DD} –0.3				
	VOL1	IOL1 = +0.5mA, V_{DD} = 1.8 to 3.6V		—	—	0.5		
		IOL1 = +0.1mA, V_{DD} = 1.3 to 3.6V		—	—	0.5		
		IOL1 = +0.03mA, V_{DD} = 1.1 to 3.6V		—	—	0.3		
Output voltage 2 (P20–P22/2nd function is Not selected)	VOH2	IOH1 = –0.5mA, V_{DD} = 1.8 to 3.6V		V_{DD} –0.5	—	—		
		IOH1 = -0.1mA, V_{DD} = 1.3 to 3.6V		V_{DD} –0.3	—	—		
		IOH1 = -0.03mA, V_{DD} = 1.1 to 3.6V		V_{DD} –0.3	—	—		
	VOL2	IOL2 = +5mA, V_{DD} = 1.8 to 3.6V		—	—	0.5		
Output voltage 3 (P40–P41)	VOL3	IOL3 = +3mA, V_{DD} = 2.0 to 3.6V (when I^2C mode is selected)		—	—	0.4		
Output voltage 4 (COM0–15) (COM16–23)*2 (SEG0–63)	VOH4	IOH4 = –0.2mA, VL1=1.2V		V_{L4} –0.2	—	—		
	VOMH4	IOMH4 = +0.2mA, VL1=1.2V		—	—	V_{L3} +0.2		
	VOMH4S	IOMH4S = –0.2mA, VL1=1.2V		V_{L3} –0.2	—	—		
	VOM4	IOM4 = +0.2mA, VL1=1.2V		—	—	V_{L2} +0.2		
	VOM4S	IOM4S = –0.2mA, VL1=1.2V		V_{L2} –0.2	—	—		
	VOML4	IOML4 = +0.2mA, VL1=1.2V		—	—	V_{L1} +0.2		
	VOML4S	IOML4S = –0.2mA, VL1=1.2V		V_{L1} –0.2	—	—		
	VOL4	IOL4 = +0.2mA, VL1=1.2V		—	—	0.2		
Output leakage (P20–P22) (P30–P35) (P40–P47) (PA0–PA7)*1	IOOH	VOH = V_{DD} (in high-impedance state)		—	—	1	μA	3
	IOOL	VOL = V_{SS} (in high-impedance state)		–1	—	—		
Input current 1 (RESET_N)	IIH1	VIH1 = V_{DD}		0	—	1	μA	4
	IIL1	VIL1 = V_{SS}	V_{DD} = 1.8 to 3.6V	–600	–300	–20		
			V_{DD} = 1.3 to 3.6V	–600	–300	-10		
			V_{DD} = 1.1 to 3.6V	–600	–300	-2		
Input current 1 (TEST)	IIH1	VIH1 = V_{DD}	V_{DD} = 1.8 to 3.6V	20	300	600		
			V_{DD} = 1.3 to 3.6V	10	300	600		
			V_{DD} = 1.1 to 3.6V	2	300	600		
	IIL1	VIL1 = V_{ss}		-1	—	—		
Input current 2 (NMI) (P00–P03)	IIH2	VIH2 = V_{DD} (when pulled-down)	V_{DD} = 1.8 to 3.6V	2	30	200		
			V_{DD} = 1.3 to 3.6V	0.2	30	200		
			V_{DD} = 1.1 to 3.6V	0.01	30	200		

(P10–P11) (P30–P35) (P40–P47) (PA0–PA7)*1	IIL2	VIL2 = V_{SS} (when pulled-up)	V_{DD} = 1.8 to 3.6V	–200	–30	–2		
			V_{DD} = 1.3 to 3.6V	–200	–30	-0.2		
			V_{DD} = 1.1 to 3.6V	–200	–30	-0.01		
	IIH2Z	VIH2 = V_{DD} (in high-impedance state)		—	—	1		
	IIL2Z	VIL2 = V_{SS} (in high-impedance state)		–1	—	—		

*1: ML610Q435 only
*2: ML610Q436 only

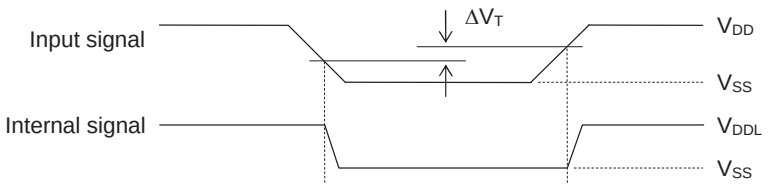
DC CHARACTERISTICS (5/5))

(V_{DD} = 1.1 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified) (5/5)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST) (NMI) (P00–P03) (P10–P11) (P31–P35) (P40–P43) (P45–P47) (PA0–PA7)*1	VIH1	V_{DD} = 1.3 to 3.6V	0.7 ×V_{DD}	—	V_{DD}	V	5
		V_{DD} = 1.1 to 3.6V	0.7 ×V_{DD}	—	V_{DD}		
	VIL1	V_{DD} = 1.3 to 3.6V	0	—	0.3 ×V_{DD}		
		V_{DD} = 1.1 to 3.6V	0	—	0.2 ×V_{DD}		
Hysteresis width (RESET_N) (TEST_N) (NMI) (P00–P03) (P10–P11) (P31–P35) (P40–P43) (P45–P47) (PA0–PA7)*1	ΔVT	V_{DD} = 2.0 to 3.6V	0.05 ×V_{DD}	0.18 ×V_{DD}	0.4 ×V_{DD}		
		V_{DD} = 1.1 to 3.6V	0.02 ×V_{DD}	0.18 ×V_{DD}	0.4 ×V_{DD}		
Input voltage 2 (P30, P44)	VIH2	—	0.7 ×V_{DD}	—	V_{DD}		
	VIL2	—	0	—	0.3 ×V_{DD}		
Input pin capacitance (NMI) (P00–P03) (P10–P11) (P30–P35) (P40–P47) (PA0–PA7)*1	CIN	f = 10kHz V_{rms} = 50mV Ta = 25°C	—	—	5	pF	—

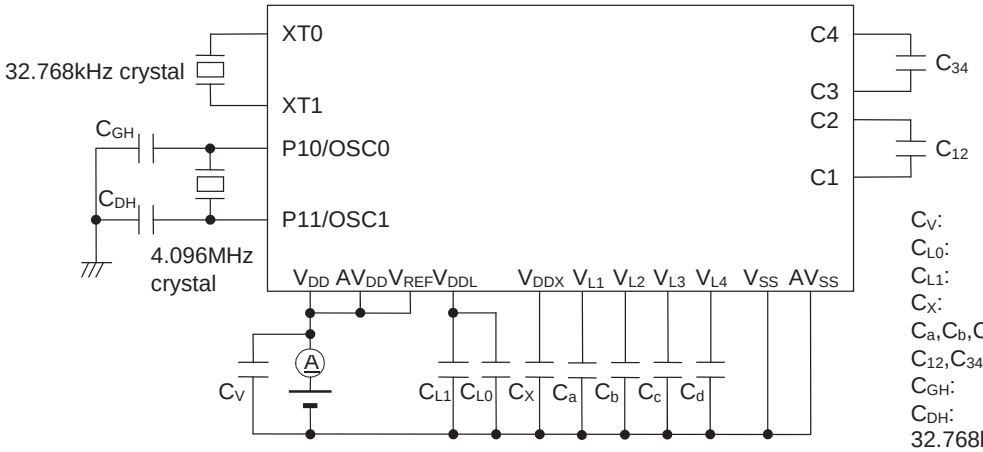
*1: ML610Q435 only

HYSTERESIS WIDTH



MEASURING CIRCUITS

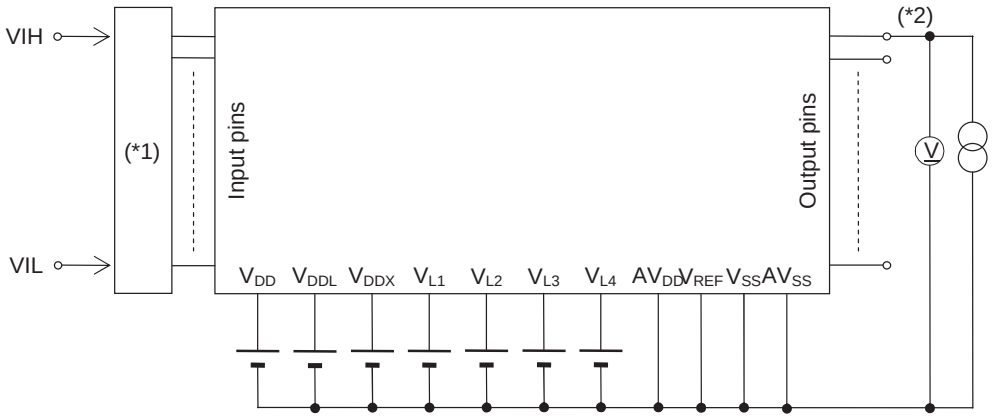
MEASURING CIRCUIT 1



C_V:	1µF
C_{L0}:	1µF
C_{L1}:	0.1µF
C_X:	0.1µF
C_a,C_b,C_c,C_d:	1µF
C_{12},C_{34}:	1µF
C_{GH}:	24pF
C_{DH}:	24pF

32.768kHz crystal:
C-001R (Epson Toyocom)
4.096MHz crystal:
HC49SFWB (Kyocera)

MEASURING CIRCUIT 2



(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

AC CHARACTERISTICS (I^2C Bus Interface: Standard Mode 100kHz)

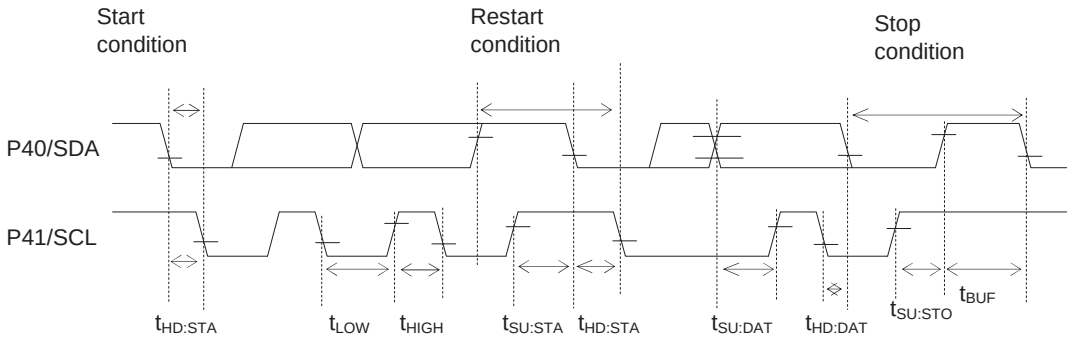
(V_{DD} = 1.8 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCL "L" level time	t_{LOW}	—	4.7	—	—	µs
SCL "H" level time	t_{HIGH}	—	4.0	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	3.45	µs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus-free time	t_{BUF}	—	4.7	—	—	µs

AC CHARACTERISTICS (I2C Bus Interface: Fast Mode 400kHz)

(V_{DD} = 1.8 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL "L" level time	t_{LOW}	—	1.3	—	—	µs
SCL "H" level time	t_{HIGH}	—	0.6	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	0.9	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus-free time	t_{BUF}	—	1.3	—	—	µs



Electrical Characteristics of Successive Approximation Type A/D Converter

(V_{DD} = 1.8 to 3.6V, AV_{DD} = 2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n	—	—	—	12	bit
Integral non-linearity error	IDL	2.7V ≤ V_{REF} ≤ 3.6V	–4	—	+4	LSB
		2.2V ≤ V_{REF} ≤ 2.7V	–6	—	+6	
Differential non-linearity error	DNL	2.7V ≤ V_{REF} ≤ 3.6V	–3	—	+3	
		2.2V ≤ V_{REF} ≤ 2.7V	–5	—	+5	
Zero-scale error	V_{OFF}	—	–6	—	+6	
Full-scale error	FSE	—	–6	—	+6	
Reference voltage	V_{REF}	—	2.2	—	AV_{DD}	V
Conversion time	t_{CONV}	SACK = 0 (HSCLK = 375kHz to 625kHz)	—	25	—	ϕ/CH
		SACK = 1 (HSCLK = 1.5MHz to 4.2MHz)	—	112	—	

ϕ: Period of high-speed clock (HSCLK)