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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc8358ecvvagdga

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



- 10/100 Mbps Ethernet/IEEE Std. 802.3TM CDMA/CS interface through a media-independent interface (MII, RMII, RGMII)¹
- 1000 Mbps Ethernet/IEEE 802.3 CDMA/CS interface through a media-independent interface (GMII, RGMII, TBI, RTBI) on UCC1 and UCC2
- 9.6-Kbyte jumbo frames
- ATM full-duplex SAR, up to 622 Mbps (OC-12/STM-4), AAL0, AAL1, and AAL5 in accordance ITU-T I.363.5
- ATM AAL2 CPS, SSSAR, and SSTED up to 155 Mbps (OC-3/STM-1) Mbps full duplex (with 4 CPS packets per cell) in accordance ITU-T I.366.1 and I.363.2
- ATM traffic shaping for CBR, VBR, UBR, and GFR traffic types compatible with ATM forum TM4.1 for up to 64-Kbyte simultaneous ATM channels
- ATM AAL1 structured and unstructured circuit emulation service (CES 2.0) in accordance with ITU-T I.163.1 and ATM Forum af-vtoa-00-0078.000
- IMA (Inverse Multiplexing over ATM) for up to 31 IMA links over 8 IMA groups in accordance with the ATM forum AF-PHY-0086.000 (Version 1.0) and AF-PHY-0086.001 (Version 1.1)
- ATM Transmission Convergence layer support in accordance with ITU-T I.432
- ATM OAM handling features compatible with ITU-T I.610
- PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686, and 3153
- IP support for IPv4 packets including TOS, TTL, and header checksum processing
- Ethernet over first mile IEEE 802.3ah
- Shim header
- Ethernet-to-Ethernet/AAL5/AAL2 inter-working
- L2 Ethernet switching using MAC address or IEEE Std. 802.1P/Q[™] VLAN tags
- ATM (AAL2/AAL5) to Ethernet (IP) interworking in accordance with RFC2684 including bridging of ATM ports to Ethernet ports
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- AAL2 protocol rate up to 4 CPS at OC-3/STM-1 rate
- Packet over Sonet (POS) up to 622-Mbps full-duplex 124 MultiPHY
- POS hardware; microcode must be loaded as an IRAM package
- Transparent up to 70-Mbps full-duplex
- HDLC up to 70-Mbps full-duplex
- HDLC BUS up to 10 Mbps
- Asynchronous HDLC
- UART
- BISYNC up to 2 Mbps
- User-programmable Virtual FIFO size
- QUICC multichannel controller (QMC) for 64 TDM channels
- One multichannel communication controller (MCC) only on the MPC8360E supporting the following:
 - 256 HDLC or transparent channels
 - 128 SS7 channels
 - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces
- Two UTOPIA/POS interfaces on the MPC8360E supporting 124 MultiPHY each (optional 2*128 MultiPHY with extended address) and one UTOPIA/POS interface on the MPC8358E supporting 31/124 MultiPHY
- Two serial peripheral interfaces (SPI); SPI2 is dedicated to Ethernet PHY management

1.SMII or SGMII media-independent interface is not currently supported.



Table 1.	Absolute	Maximum	Ratings ¹	(continued)
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Characteristic	Symbol	Max Value	Unit	Notes
Storage temperature range	T _{STG}	-55 to 150	°C	_

Notes:

- 1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- 2. Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
- 3. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
- 4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
- 5. (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 3.
- 6. OV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 4.

2.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for the device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2.	Recommended	Operating	Conditions
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Characteristic	Symbol	Recommended Value	Unit	Notes
Core and PLL supply voltage for	V _{DD} & AV _{DD}	1.2 V ± 60 mV	V	1, 3
MPC8358 Device Part Number with Processor Frequency label of AD=266MHz and AG=400MHz & QUICC Engine Frequency label of E=300MHz & G=400MHz				
MPC8360 Device Part Number with Processor Frequency label of AG=400MHz and AJ=533MHz & QUICC Engine Frequency label of G=400MHz				
Core and PLL supply voltage for	V _{DD} & AV _{DD}	1.3 V ± 50 mV	V	1, 3
MPC8360 Device Part Number with Processor Frequency label of AL=667MHz and QUICC Engine Frequency label of H=500MHz				
DDR and DDR2 DRAM I/O supply voltage DDR DDR2	GV _{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	_
Three-speed Ethernet I/O supply voltage	LV _{DD} 0	3.3 V ± 330 mV 2.5 V ± 125 mV	V	_
Three-speed Ethernet I/O supply voltage	LV _{DD} 1	3.3 V ± 330 mV 2.5 V ± 125 mV	V	_
Three-speed Ethernet I/O supply voltage	LV _{DD} 2	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—



GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

8.2.1.2 GMII Receive AC Timing Specifications

This table provides the GMII receive AC timing specifications.

Table 28. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
RX_CLK clock period	t _{GRX}	_	8.0	—	ns	_
RX_CLK duty cycle	t _{GRXH} /t _{GRX}	40		60	%	—
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{GRDVKH}	2.0		—	ns	—
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t _{GRDXKH}	0.2		—	ns	2
RX_CLK clock rise time, (20% to 80%)	t _{GRXR}	_		1.0	ns	—
RX_CLK clock fall time, (80% to 20%)	t _{GRXF}	_	_	1.0	ns	—

Notes:

- 1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- In rev. 2.0 silicon, due to errata, t_{GRDXKH} minimum is 0.5 which is not compliant with the standard. Refer to Errata QE_ENET18 in Chip Errata for the MPC8360E, Rev. 1.

This figure shows the GMII receive AC timing diagram.



Figure 11. GMII Receive AC Timing Diagram



GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

Table 32. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with $\text{LV}_{\text{DD}}/\text{OV}_{\text{DD}}$ of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	t _{RMRDVKH}	4.0	_	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	t _{RMRDXKH}	2.0	_	—	ns
REF_CLK clock rise time	t _{RMXR}	1.0	_	4.0	ns
REF_CLK clock fall time	t _{RMXF}	1.0	_	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first three letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{RMRDVKH} symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, t_{RMRDXKL} symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}

This figure provides the AC test load.



Figure 16. AC Test Load

This figure shows the RMII receive AC timing diagram.



Figure 17. RMII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.



8.2.5 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 35. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
Data to clock output skew (at transmitter)	t _{SKRGTKHDX} t _{SKRGTKHDV}	-0.5 		— 0.5	ns	7
Data to clock input skew (at receiver)	t _{SKRGDXKH} t _{SKRGDVKH}	1.0		 2.6	ns	2
Clock cycle duration	t _{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	t _{RGTH} /t _{RGT}	45	50	55	%	4, 5
Duty cycle for 10BASE-T and 100BASE-TX	t _{RGTH} /t _{RGT}	40	50	60	%	3, 5
Rise time (20–80%)	t _{RGTR}	—		0.75	ns	
Fall time (20–80%)	t _{RGTF}	—	_	0.75	ns	
GTX_CLK125 reference clock period	t _{G125}	—	8.0	_	ns	6
GTX_CLK125 reference clock duty cycle	t _{G125H} /t _{G125}	47		53	%	

Notes:

- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (Rx) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- 2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns can be added to the associated clock signal.
- 3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
- 4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- 5. Duty cycle reference is LV_{DD}/2.
- 6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
- 7. In rev. 2.0 silicon, due to errata, t_{SKRGTKHDX} minimum is –2.3 ns and t_{SKRGTKHDV} maximum is 1 ns for UCC1, 1.2 ns for UCC2 option 1, and 1.8 ns for UCC2 option 2. In rev. 2.1 silicon, due to errata, t_{SKRGTKHDX} minimum is –0.65 ns for UCC2 option 1 and –0.9 for UCC2 option 2, and t_{SKRGTKHDV} maximum is 0.75 ns for UCC1 and UCC2 option 1 and 0.85 for UCC2 option 2. Refer to Errata QE_ENET10 in *Chip Errata for the MPC8360E, Rev. 1*. UCC1 does meet t_{SKRGTKHDX} minimum for rev. 2.1 silicon.



Ethernet Management Interface Electrical Characteristics

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.



Figure 20. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI, and RTBI are specified in Section 8.1, "Three-Speed Ethernet Controller (10/100/1000 Mbps)— GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage (3.3 V)	OV _{DD}	—		2.97	3.63	V
Output high voltage	V _{OH}	$I_{OH} = -1.0 \text{ mA}$	$OV_{DD} = Min$	2.10	OV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	$OV_{DD} = Min$	GND	0.50	V
Input high voltage	V _{IH}	—		2.00	—	V
Input low voltage	V _{IL}	—		—	0.80	V
Input current	I _{IN}	0 V ≤V _{IN}	₁≤OV _{DD}	—	±10	μA

Table 36. MII Management DC Electrica	I Characteristics When Powered at 3.3 V
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JTAG DC Electrical Characteristics



Figure 28. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (DLL Enabled)

10 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8360E/58E.

10.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface of the device.

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	—	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V
Input high voltage	V _{IH}	—	2.5	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	$0 V \leq V_{IN} \leq OV_{DD}$	_	±10	μA



I2C AC Electrical Specifications

11.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interface of the device.

Table 45. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 44).

Parameter	Symbol ¹	Min	Max	Unit	Note
SCL clock frequency	f _{I2C}	0	400	kHz	2
Low period of the SCL clock	t _{I2CL}	1.3	_	μs	—
High period of the SCL clock	t _{I2CH}	0.6	_	μs	—
Setup time for a repeated START condition	t _{I2SVKH}	0.6	_	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL}	0.6	_	μs	_
Data setup time	t _{I2DVKH}	100	_	ns	3
Data hold time: CBUS compatible masters I ² C bus devices	t _{I2DXKL}	$\frac{1}{0^2}$	 0.9 ³	μs	—
Rise time of both SDA and SCL signals	t _{I2CR}	20 + 0.1 C _b ⁴	300	ns	—
Fall time of both SDA and SCL signals	t _{I2CF}	20 + 0.1 C _b ⁴	300	ns	—
Set-up time for STOP condition	t _{I2PVKH}	0.6	_	μs	—
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	_	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times \text{OV}_{\text{DD}}$	_	V	_
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times \text{OV}_{\text{DD}}$	_	V	_

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional}

block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

 The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of the falling edge of SCL.

3. The maximum t_{12DVKH} has only to be met if the device does not stretch the LOW period (t_{12CL}) of the SCL signal.

4. C_B = capacitance of one bus line in pF.



This figure provides the AC test load for the I^2C .



Figure 34. I²C AC Test Load

This figure shows the AC timing diagram for the I^2C bus.



12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8360E/58E.

12.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface of the device.

Table 46. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Мах	Unit
High-level input voltage	V _{IH}	$V_{OUT} \ge V_{OH}$ (min) or	$0.5\times\text{OV}_\text{DD}$	OV _{DD} + 0.5	V
Low-level input voltage	V _{IL}	V _{OUT} ≤V _{OL} (max)	-0.5	$0.3 imes OV_{DD}$	V
High-level output voltage	V _{OH}	I _{OH} = -500 μA	$0.9 imes OV_{DD}$	—	V
Low-level output voltage	V _{OL}	l _{OL} = 1500 μA	—	$0.1 imes OV_{DD}$	V
Input current	I _{IN}	0 V ≤V _{IN} ¹ ≤OV _{DD}	—	±10	μA

12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the device. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. This table provides the PCI AC timing specifications at 66 MHz.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Clock to output valid	t _{PCKHOV}	_	6.0	ns	2, 5
Output hold from clock	t _{PCKHOX}	1	—	ns	2

Table 47. PCI AC Timing Specifications at 66 MHz



HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

This figure shows the UTOPIA timing with internal clock.





18 HDLC, BISYNC, Transparent, and Synchronous UART

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent, and synchronous UART protocols of the MPC8360E/58E.

18.1 HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

This table provides the DC electrical characteristics for the device HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 61. HDLC, BISYNC,	Transparent, and Synchronous UART DC Electrical Characteristics
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Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V _{OH}	I _{OH} = -2.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.5	V
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	0 V ≤V _{IN} ≤OV _{DD}	—	±10	μA

18.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

These tables provide the input and output AC timing specifications for HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 62. HDLC, BISYNC, and Transparent AC Timing Specifications¹

Characteristic	Symbol ²	Min	Мах	Unit
Outputs—Internal clock delay	t _{HIKHOV}	0	11.2	ns
Outputs—External clock delay	t _{HEKHOV}	1	10.8	ns



USB DC Electrical Characteristics

19 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8360E/58E.

19.1 USB DC Electrical Characteristics

This table provides the DC electrical characteristics for the USB interface.

Table 64. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
High-level output voltage, $I_{OH} = -100 \ \mu A$	V _{OH}	OV _{DD} - 0.4	—	V
Low-level output voltage, I _{OL} = 100 μA	V _{OL}	—	0.2	V
Input current	I _{IN}	—	±10	μA

19.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface of the device.

Table 65. USB General Timing Parameters

Parameter	Symbol ¹	Min	Мах	Unit	Notes	Note
USB clock cycle time	t _{USCK}	20.83	—	ns	Full speed 48 MHz	_
USB clock cycle time	t _{USCK}	166.67	—	ns	Low speed 6 MHz	_
Skew between TXP and TXN	t _{USTSPN}	_	5	ns	—	2
Skew among RXP, RXN, and RXD	t _{USRSPND}	_	10	ns	Full speed transitions	2
Skew among RXP, RXN, and RXD	t _{USRPND}		100	ns	Low speed transitions	2

Notes:

The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(state)(signal)} for receive signals and t_{(first two letters of functional block)(state)(signal)} for transmit signals. For example, t_{USRSPND} symbolizes USB timing (US) for the USB receive signals skew (RS) among RXP, RXN, and RXD (PND). Also, t_{USTSPN} symbolizes USB timing (US) for the USB transmit signals skew (TS) between TXP and TXN (PN).

2. Skew measurements are done at $OV_{DD}/2$ of the rising or falling edge of the signals.

This figure provide the AC test load for the USB.



Figure 52. USB AC Test Load



20 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8360E/58E is available in a tape ball grid array (TBGA), see Section 20.1, "Package Parameters for the TBGA Package," and Section 20.2, "Mechanical Dimensions of the TBGA Package," for information on the package.

20.1 Package Parameters for the TBGA Package

The package parameters for rev. 2.0 silicon are as provided in the following list. The package type is $37.5 \text{ mm} \times 37.5 \text{ mm}$, 740 tape ball grid array (TBGA).

Package outline	$37.5 \text{ mm} \times 37.5 \text{ mm}$
Interconnects	740
Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder Balls	62 Sn/36 Pb/2 Ag (ZU package)
	95.5 Sn/0.5 Cu/4Ag (VV package)
Ball diameter (typical)	0.64 mm



able 66. MPC8360E TBGA	Pinout Listing	(continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Notes
CE_PA[22]	AF3	I/O	OV _{DD}	—
CE_PA[23:26]	C18, D18, E18, A18	I/O	LV _{DD} 1	—
CE_PA[27:28]	AF2, AE6	I/O	OV _{DD}	—
CE_PA[29]	B19	I/O	LV _{DD} 1	—
CE_PA[30]	AE5	I/O	OV _{DD}	—
CE_PA[31]	F16	I/O	LV _{DD} 1	—
CE_PB[0:27]	AE2, AE1, AD5, AD3, AD2, AC6, AC5, AC4, AC2, AC1, AB5, AB4, AB3, AB1, AA6, AA4, AA2, Y6, Y4, Y3, Y2, Y1, W6, W5, W2, V5, V3, V2	I/O	OV _{DD}	_
CE_PC[0:1]	V1, U6	I/O	OV _{DD}	—
CE_PC[2:3]	C16, A15	I/O	LV _{DD} 1	
CE_PC[4:6]	U4, U3, T6	I/O	OV _{DD}	—
CE_PC[7]	C19	I/O	LV _{DD} 2	_
CE_PC[8:9]	A4, C5	I/O	LV _{DD} 0	_
CE_PC[10:30]	T5, T4, T2, T1, R5, R3, R1, C11, D12, F13, B10, C10, E12, A9, B8, D10, A14, E15, B14, D15, AH2	I/O	OV _{DD}	
CE_PD[0:27]	E11, D9, C8, F11, A7, E9, C7, A6, F10, B6, D7, E8, B5, A5, C2, E4, F5, B1, D2, G5, D1, E2, H6, F3, E1, F2, G3, H4	I/O	OV _{DD}	_
CE_PE[0:31]	K3, J2, F1, G2, J5, H3, G1, H2, K6, J3, K5, K4, L6, P6, P4, P3, P1, N4, N5, N2, N1, M2, M3, M5, M6, L1, L2, L4, E14, C13, C14, B13	I/O	OV _{DD}	_
CE_PF[0:3]	F14, D13, A12, A11	I/O	OV _{DD}	—
	Clocks			
PCI_CLK_OUT[0]/CE_PF[26]	B22	I/O	LV _{DD} 2	
PCI_CLK_OUT[1:2]/CE_PF[27:28]	D22, A23	I/O	OV _{DD}	
CLKIN	E37	I	OV _{DD}	
PCI_CLOCK/PCI_SYNC_IN	M36	I	OV _{DD}	_
PCI_SYNC_OUT/CE_PF[29]	D37	I/O	OV _{DD}	3
	JTAG			
тск	K33	I	OV _{DD}	_
TDI	K34	I	OV _{DD}	4
TDO	H37	0	OV _{DD}	3
TMS	J36	I	OV _{DD}	4
TRST	L32	I	OV _{DD}	4
	Test		1	
TEST	L35	I	OV _{DD}	7
TEST_SEL	AU34	I	GV _{DD}	7



Pinout Listings

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
No Connect				
NC	AM20, AU19	—	—	—

Notes:

- 1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}
- 2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
- 3. This output is actively driven during reset rather than being three-stated during reset.
- 4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- 5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
- 6. These are On Die Termination pins, used to control DDR2 memories internal termination resistance.
- 7. This pin must always be tied to GND.
- 8. This pin must always be left not connected.
- 9. Refer to MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual section on "RGMII Pins," for information about the two UCC2 Ethernet interface options.
- 10.It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor for DDR2.

This table shows the pin list of the MPC8358E TBGA package.

Table 67. MPC8358E TBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	DDR SDRAM Memory Controller Interface			
MEMC1_MDQ[0:63]	AJ34, AK33, AL33, AL35, AJ33, AK34, AK32, AM36, AN37, AN35, AR34, AT34, AP37, AP36, AR36, AT35, AP34, AR32, AP32, AM31, AN33, AM34, AM33, AM30, AP31, AM27, AR30, AT32, AN29, AP29, AN27, AR29, AN8, AN7, AM8, AM6, AP9, AN9, AT7, AP7, AU6, AP6, AR4, AR3, AT6, AT5, AR5, AT3, AP4, AM5, AP3, AN3, AN5, AL5, AN4, AM2, AL2, AH5, AK3, AJ2, AJ3, AH4, AK4, AH3	I/O	GV _{DD}	_
MEMC_MECC[0:4]/MSRCID[0:4]	AP24, AN22, AM19, AN19, AM24	I/O	GV _{DD}	—
MEMC_MECC[5]/MDVAL	AM23	I/O	GV _{DD}	—
MEMC_MECC[6:7]	AM22, AN18	I/O	GV _{DD}	—
MEMC_MDM[0:8]	AL36, AN34, AP33, AN28,AT9, AU4, AM3, AJ6,AP27	0	GV _{DD}	
MEMC_MDQS[0:8]	AK35, AP35, AN31, AM26,AT8, AU3, AL4, AJ5, AP26	I/O	GV _{DD}	—
MEMC_MBA[0:1]	AU29, AU30	0	GV _{DD}	
MEMC_MBA[2]	AT30	0	GV _{DD}	_
MEMC_MA[0:14]	AU21, AP22, AP21, AT21, AU25, AU26, AT23, AR26, AU24, AR23, AR28, AU23, AR22, AU20, AR18	0	GV _{DD}	
MEMC_MODT[0:3]	AG33, AJ36, AT1, AK2	0	GV _{DD}	6



Pinout Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes
CE_PB[0:27]	AE2, AE1, AD5, AD3, AD2, AC6, AC5, AC4, AC2, AC1, AB5, AB4, AB3, AB1, AA6, AA4, AA2, Y6, Y4, Y3, Y2, Y1, W6, W5, W2, V5, V3, V2	I/O	OV _{DD}	_
CE_PC[0:1]	V1, U6	I/O	OV _{DD}	
CE_PC[2:3]	C16, A15	I/O	LV _{DD} 1	—
CE_PC[4:6]	U4, U3, T6	I/O	OV _{DD}	—
CE_PC[7]	C19	I/O	LV _{DD} 2	—
CE_PC[8:9]	A4, C5	I/O	LV _{DD} 0	—
CE_PC[10:30]	T5, T4, T2, T1, R5, R3, R1, C11, D12, F13, B10, C10, E12, A9, B8, D10, A14, E15, B14, D15, AH2	I/O	OV _{DD}	_
CE_PD[0:27]	E11, D9, C8, F11, A7, E9, C7, A6, F10, B6, D7, E8, B5, A5, C2, E4, F5, B1, D2, G5, D1, E2, H6, F3, E1, F2, G3, H4	I/O	OV _{DD}	—
CE_PE[0:31]	K3, J2, F1, G2, J5, H3, G1, H2, K6, J3, K5, K4, L6, P6, P4, P3, P1, N4, N5, N2, N1, M2, M3, M5, M6, L1, L2, L4, E14, C13, C14, B13	I/O	OV _{DD}	—
CE_PF[0:3]	F14, D13, A12, A11	I/O	OV _{DD}	—
	Clocks			
PCI_CLK_OUT[0]/CE_PF[26]	B22	I/O	LV _{DD} 2	—
PCI_CLK_OUT[1:2]/CE_PF[27:28]	D22, A23	I/O	OV _{DD}	—
CLKIN	E37		OV _{DD}	—
PCI_CLOCK/PCI_SYNC_IN	N M36		OV _{DD}	—
PCI_SYNC_OUT/CE_PF[29]	D37	I/O	OV _{DD}	3
JTAG				
ТСК	K33	I	OV _{DD}	_
TDI	К34	I	OV _{DD}	4
TDO	H37	0	OV _{DD}	3
TMS	J36	I	OV _{DD}	4
TRST	L32	I	OV _{DD}	4
Test				
TEST	L35	I	OV _{DD}	7
TEST_SEL	AU34	I	GV _{DD}	10
PMC				
QUIESCE	B36	0	OV _{DD}	—
System Control				

Table 67. MPC8358E TBGA Pinout Listing (continued)



Pinout Listings

21 Clocking

This figure shows the internal distribution of clocks within the MPC8360E.



Figure 54. MPC8360E Clock Subsystem





ordered, see Section 24.1, "Part Numbers Fully Addressed by this Document," for part ordering details and contact your Freescale sales representative or authorized distributor for more information.

Characteristic ¹	400 MHz	533 MHz	667 MHz ²	Unit
e300 core frequency (<i>core_clk</i>)	266–400	266–533	266–667	MHz
Coherent system bus frequency (<i>csb_clk</i>)	133–333			MHz
QUICC Engine frequency ³ (<i>ce_clk</i>)		MHz		
DDR and DDR2 memory bus frequency (MCLK) ⁴	100–166.67			MHz
Local bus frequency (LCLK <i>n</i>) ⁵	16.67–133			MHz
PCI input frequency (CLKIN or PCI_CLK)	25–66.67		MHz	
Security core maximum internal operating frequency	133	133	166	MHz

Table 69. Operating Frequencies for the TBGA Package

Notes:

- 1. The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
- 2. The 667 MHz core frequency is based on a 1.3 V V_{DD} supply voltage.
- 3. The 500 MHz QE frequency is based on a 1.3 V V_{DD} supply voltage.
- 4. The DDR data rate is 2x the DDR memory bus frequency.
- 5. The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWL[LBCM]).

21.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] and RCWL[SVCOD] parameters. This table shows the multiplication factor encodings for the system PLL.

RCWL[SPMF]	System PLL Multiplication Factor
0000	× 16
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11

Table 70. System PLL Multiplication Factors



Table 77. Package Thermal Characteristics for the TBGA Package (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-package natural convection on top		1	° C/W	6

Notes

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
- 2. Per JEDEC JESD51-2 and SEMI G38-87 with the single layer board horizontal.
- 3. Per JEDEC JESD51-6 with the board horizontal. 1 m/sec is approximately equal to 200 linear feet per minute (LFM).
- 4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

22.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See Table 6 for typical power dissipations values.

22.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

 T_J = junction temperature (° C)

 T_A = ambient temperature for the package (° C)

 $R_{\theta IA}$ = junction-to-ambient thermal resistance (° C/W)

 P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

22.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. Additionally, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device. At a known board temperature, the junction temperature is estimated using the following equation:



where:

 T_I = junction temperature (° C)

 $T_I = T_B + (R_{\theta IB} \times P_D)$

 T_B = board temperature at the package perimeter (° C)

 $R_{\theta JA}$ = junction to board thermal resistance (° C/W) per JESD51-8

 P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

22.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

 T_J = junction temperature (° C)

 T_T = thermocouple temperature on top of package (° C)

 Ψ_{IT} = junction-to-ambient thermal resistance (° C/W)

 P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

22.2.4 Heat Sinks and Junction-to-Ambient Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

 $R_{\theta JA}$ = junction-to-ambient thermal resistance (° C/W)

 $R_{\theta JC}$ = junction-to-case thermal resistance (° C/W)

 $R_{\theta CA}$ = case-to-ambient thermal resistance (° C/W)

 $R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.



Table 82.	Revision	History	(continued)
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Rev. Number	Date	Substantive Change(s)
3	03/2010	 Changed references to RCWH[PCICKEN] to RCWH[PCICKDRV]. In Table 2, added extended temperature characteristics. Added Figure 6, "DDR Input Timing Diagram." In Figure 53, "Mechanical Dimensions and Bottom Surface Nomenclature of the TBGA Package," removed watermark. Updated the title of Table 19,"DDR SDRAM Input AC Timing Specifications." In Table 20, "DDR and DDR2 SDRAM Input AC Timing Specifications Mode," changed table subtitle. In Table 20, "DDR and DDR2 SDRAM Input AC Timing Specifications Mode," changed table subtitle. In Table 27–Table 30, and Table 33—Table 34, changed the rise and fall time specifications to reference 20–80% and 80–20% of the voltage supply, respectively. In Table 38, "IEEE 1588 Timer AC Specifications," changed units to "ns" for t_{I2DVKH}. In Table 45, "I2C AC Electrical Specifications," changed units to "ns" for t_{I2DVKH}. In Table 66, "MPC8360E TBGA Pinout Listing," and Table 67 "MPC8358E TBGA Pinout Listing, added note 7: "This pin must always be tied to GND" to the TEST pin and added a note to SPARE1 stating: "This pin must always be left not connected." In Section 4, "Clock Input Timing," added note regarding rise/fall time on QUICC Engine block input pins. Added Section 4.1, "injol/100/1000 Ethernet DC Electrical Characteristics." In Section 2.1, "Pinout Listing," added sentence stating "Refer to AN3097, 'MPC8360/MPC8358E PowerQUICC Design Checklist,' for proper pin termination and usage." In Section 21, "Clocking," removed statement: "The OCCR[PCICDn] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUTn signals." In Section 21.1, "System PLL Configuration," updated the system VCO frequency conditions. In Table 80, added extended temperature characteristics.
2	12/2007	Initial release.