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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8358ecvvagdg

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



wide range of protocols including ATM, Ethernet, HDLC, and POS. The QUICC Engine module's enhanced interworking eases the transition and reduces investment costs from ATM to IP based systems. The other major features include a dual DDR SDRAM memory controller for the MPC8360E, which allows equipment providers to partition system parameters and data in an extremely efficient way, such as using one 32-bit DDR memory controller for control plane processing and the other for data plane processing. The MPC8358E has a single DDR SDRAM memory controller. The MPC8360E/58E also offers a 32-bit PCI controller, a flexible local bus, and a dedicated security engine.

This figure shows the MPC8360Eblock diagram.



Figure 1. MPC8360E Block Diagram



This figure shows the MPC8358E block diagram.



Figure 2. MPC8358E Block Diagram

Major features of the MPC8360E/58E are as follows:

- e300 PowerPC processor core (enhanced version of the MPC603e core)
 - Operates at up to 667 MHz (for the MPC8360E) and 400 MHz (for the MPC8358E)
 - High-performance, superscalar processor core
 - Floating-point, integer, load/store, system register, and branch processing units
 - 32-Kbyte instruction cache, 32-Kbyte data cache
 - Lockable portion of L1 cache
 - Dynamic power management
 - Software-compatible with the Freescale processor families implementing the Power Architecture[™] technology
- QUICC Engine unit
 - Two 32-bit RISC controllers for flexible support of the communications peripherals, each operating up to 500 MHz (for the MPC8360E) and 400 MHz (for the MPC8358E)
 - Serial DMA channel for receive and transmit on all serial channels
 - QUICC Engine module peripheral request interface (for SEC, PCI, IEEE Std. 1588TM)
 - Eight universal communication controllers (UCCs) on the MPC8360E and six UCCs on the MPC8358E supporting the following protocols and interfaces (not all of them simultaneously):
 - IEEE 1588 protocol supported



- 10/100 Mbps Ethernet/IEEE Std. 802.3TM CDMA/CS interface through a media-independent interface (MII, RMII, RGMII)¹
- 1000 Mbps Ethernet/IEEE 802.3 CDMA/CS interface through a media-independent interface (GMII, RGMII, TBI, RTBI) on UCC1 and UCC2
- 9.6-Kbyte jumbo frames
- ATM full-duplex SAR, up to 622 Mbps (OC-12/STM-4), AAL0, AAL1, and AAL5 in accordance ITU-T I.363.5
- ATM AAL2 CPS, SSSAR, and SSTED up to 155 Mbps (OC-3/STM-1) Mbps full duplex (with 4 CPS packets per cell) in accordance ITU-T I.366.1 and I.363.2
- ATM traffic shaping for CBR, VBR, UBR, and GFR traffic types compatible with ATM forum TM4.1 for up to 64-Kbyte simultaneous ATM channels
- ATM AAL1 structured and unstructured circuit emulation service (CES 2.0) in accordance with ITU-T I.163.1 and ATM Forum af-vtoa-00-0078.000
- IMA (Inverse Multiplexing over ATM) for up to 31 IMA links over 8 IMA groups in accordance with the ATM forum AF-PHY-0086.000 (Version 1.0) and AF-PHY-0086.001 (Version 1.1)
- ATM Transmission Convergence layer support in accordance with ITU-T I.432
- ATM OAM handling features compatible with ITU-T I.610
- PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686, and 3153
- IP support for IPv4 packets including TOS, TTL, and header checksum processing
- Ethernet over first mile IEEE 802.3ah
- Shim header
- Ethernet-to-Ethernet/AAL5/AAL2 inter-working
- L2 Ethernet switching using MAC address or IEEE Std. 802.1P/Q[™] VLAN tags
- ATM (AAL2/AAL5) to Ethernet (IP) interworking in accordance with RFC2684 including bridging of ATM ports to Ethernet ports
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- AAL2 protocol rate up to 4 CPS at OC-3/STM-1 rate
- Packet over Sonet (POS) up to 622-Mbps full-duplex 124 MultiPHY
- POS hardware; microcode must be loaded as an IRAM package
- Transparent up to 70-Mbps full-duplex
- HDLC up to 70-Mbps full-duplex
- HDLC BUS up to 10 Mbps
- Asynchronous HDLC
- UART
- BISYNC up to 2 Mbps
- User-programmable Virtual FIFO size
- QUICC multichannel controller (QMC) for 64 TDM channels
- One multichannel communication controller (MCC) only on the MPC8360E supporting the following:
 - 256 HDLC or transparent channels
 - 128 SS7 channels
 - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces
- Two UTOPIA/POS interfaces on the MPC8360E supporting 124 MultiPHY each (optional 2*128 MultiPHY with extended address) and one UTOPIA/POS interface on the MPC8358E supporting 31/124 MultiPHY
- Two serial peripheral interfaces (SPI); SPI2 is dedicated to Ethernet PHY management

1.SMII or SGMII media-independent interface is not currently supported.



- DRAM chip configurations from 64 Mbits to 1 Gigabit with $\times 8/\times 16$ data ports
- Full ECC support (when the MPC8360E is configured as 2×32-bit DDR memory controllers, both support ECC)
- Page mode support (up to 16 simultaneous open pages for DDR1, up to 32 simultaneous open pages for DDR2)
- Contiguous or discontiguous memory mapping
- Read-modify-write support
- Sleep mode support for self refresh SDRAM
- Supports auto refreshing
- Supports source clock mode
- On-the-fly power management using CKE
- Registered DIMM support
- 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
- External driver impedance calibration
- On-die termination (ODT)
- PCI interface
 - PCI Specification Revision 2.3 compatible
 - Data bus widths:
 - Single 32-bit data PCI interface that operates at up to 66 MHz
 - PCI 3.3-V compatible (not 5-V compatible)
 - PCI host bridge capabilities on both interfaces
 - PCI agent mode supported on PCI interface
 - Support for PCI-to-memory and memory-to-PCI streaming
 - Memory prefetching of PCI read accesses and support for delayed read transactions
 - Support for posting of processor-to-PCI and PCI-to-memory writes
 - On-chip arbitration, supporting five masters on PCI
 - Support for accesses to all PCI address spaces
 - Parity support
 - Selectable hardware-enforced coherency
 - Address translation units for address mapping between host and peripheral
 - Dual address cycle supported when the device is the target
 - Internal configuration registers accessible from PCI
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data operating at up to 133 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
 - Three protocol engines available on a per chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)
 - Dedicated single data rate SDRAM controller
 - Parity support
 - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
 - Functional and programming compatibility with the MPC8260 interrupt controller
 - Support for 8 external and 35 internal discrete interrupt sources
 - Support for one external (optional) and seven internal machine checkstop interrupt sources



Power Sequencing

This figure shows the undershoot and overshoot voltage of the PCI interface of the device for the 3.3-V signals, respectively.



Figure 4. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	OV _{DD} = 3.3 V
PCI signals	25	
PCI output clocks (including PCI_SYNC_OUT)	42	
DDR signal	20 36 (half-strength mode) ¹	GV _{DD} = 2.5 V
DDR2 signal	18 36 (half-strength mode) ¹	GV _{DD} = 1.8 V
10/100/1000 Ethernet signals	42	LV _{DD} = 2.5/3.3 V
DUART, system control, I ² C, SPI, JTAG	42	OV _{DD} = 3.3 V
GPIO signals	42	OV _{DD} = 3.3 V LV _{DD} = 2.5/3.3 V

Note:

1. DDR output impedance values for half strength mode are verified by design and not tested.

2.2 Power Sequencing

This section details the power sequencing considerations for the MPC8360E/58E.



RESET DC Electrical Characteristics

Table 9. GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV (continued)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
GTX_CLK rise and fall time $\label{eq:VDD} \begin{array}{l} \text{LV}_{\text{DD}} = 2.5 \text{ V} \\ \text{LV}_{\text{DD}} = 3.3 \text{ V} \end{array}$	t _{G125R} /t _{G125F}	—	_	0.75 1.0	ns	1
GTX_CLK125 duty cycle GMII & TBI 1000Base-T for RGMII & RTBI	t _{G125H} /t _{G125}	45 47	—	55 53	%	2
GTX_CLK125 jitter	—	—	—	±150	ps	2

Notes:

- 1. Rise and fall times for GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
- GTX_CLK125 is used to generate the GTX clock for the UCC Ethernet transmitter with 2% degradation. The GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by GTX_CLK. See Section 8.2.2, "MII AC Timing Specifications," Section 8.2.3, "RMII AC Timing Specifications," and Section 8.2.5, "RGMII and RTBI AC Timing Specifications" for the duty cycle for 10Base-T and 100Base-T reference clock.

5 **RESET Initialization**

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8360E/58E.

5.1 **RESET DC Electrical Characteristics**

This table provides the DC electrical characteristics for the RESET pins of the device.

Characteristic	Symbol Condition		Min	Max	Unit
Input high voltage	V _{IH}	_	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	_	-0.3	0.8	V
Input current	I _{IN}	_	_	±10	μA
Output high voltage	V _{OH} ²	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V

Table 10. RESET Pins DC Electrical Characteristics ¹

Notes:

1. This table applies for pins PORESET, HRESET, SRESET, and QUIESCE.

2. HRESET and SRESET are open drain pins, thus V_{OH} is not relevant for those pins.



5.2 **RESET AC Electrical Characteristics**

This section describes the AC electrical specifications for the reset initialization timing requirements of the device. This table provides the reset initialization AC timing specifications for the DDR SDRAM component(s).

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of HRESET or SRESET (input) to activate reset flow	32	_	t _{PCI_SYNC_IN}	1
Required assertion time of PORESET with stable clock applied to CLKIN when the device is in PCI host mode	32		^t CLKIN	2
Required assertion time of PORESET with stable clock applied to PCI_SYNC_IN when the device is in PCI agent mode	32	_	^t PCI_SYNC_IN	1
HRESET/SRESET assertion (output)	512	_	t _{PCI_SYNC_IN}	1
HRESET negation to SRESET negation (output)	16	-	t _{PCI_SYNC_IN}	1
Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the device is in PCI host mode	4	_	^t CLKIN	2
Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the device is in PCI agent mode	4	_	^t PCI_SYNC_IN	1
Input hold time for POR config signals with respect to negation of HRESET	0	-	ns	_
Time for the <u>device to</u> turn off POR config signals with respect to the assertion of HRESET		4	ns	3
Time for the device to turn on POR config signals with respect to the negation of HRESET	1	_	^t PCI_SYNC_IN	1, 3

Table 11. RESET Initialization Timing Specifications

Notes:

- t_{PCI_SYNC_IN} is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. Refer MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual for more details.
- t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the device is in PCI host mode. Refer MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual for more details.
- 3. POR config signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

This table provides the PLL and DLL lock times.

Table 12. PLL and DLL Lock Times

Parameter/Condition	Min	Мах	Unit	Notes	
PLL lock times	—	100	μs		
DLL lock times	7680	122,880	csb_clk cycles	1, 2	

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.

2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 21, "Clocking," for more information.



QUICC Engine Block Operating Frequency Limitations

5.3 QUICC Engine Block Operating Frequency Limitations

This section specify the limits of the AC electrical characteristics for the operation of the QUICC Engine block's communication interfaces.

NOTE

The settings listed below are required for correct hardware interface operation. Each protocol by itself requires a minimal QUICC Engine block operating frequency setting for meeting the performance target. Because the performance is a complex function of all the QUICC Engine block settings, the user should make use of the QUICC Engine block performance utility tool provided by Freescale to validate their system.

This table lists the maximal QUICC Engine block I/O frequencies and the minimal QUICC Engine block core frequency for each interface.

Interface	Interface Operating Frequency (MHz)	Max Interface Bit Rate (Mbps)	Min QUICC Engine Operating Frequency ¹ (MHz)	Notes
Ethernet Management: MDC/MDIO	10 (max)	10	20	_
MII	25 (typ)	100	50	_
RMII	50 (typ)	100	50	_
GMII/RGMII/TBI/RTBI	125 (typ)	1000	250	_
SPI (master/slave)	10 (max)	10	20	_
UCC through TDM	50 (max)	70	8 imes F	2
MCC	25 (max)	16.67	16 × F	2, 4
UTOPIA L2	50 (max)	800	$2 \times F$	2
POS-PHY L2	50 (max)	800	$2 \times F$	2
HDLC bus	10 (max)	10	20	_
HDLC/transparent	50 (max)	50	8/3 × F	2, 3
UART/async HDLC	3.68 (max internal ref clock)	115 (Kbps)	20	—
BISYNC	2 (max)	2	20	
USB	48 (ref clock)	12	96	_

Table 13. QUICC Engine Block Operating Frequency Limitations

Notes:

1. The QUICC Engine module needs to run at a frequency higher than or equal to what is listed in this table.

2. 'F' is the actual interface operating frequency.\

3. The bit rate limit is independent of the data bus width (that is, the same for serial, nibble, or octal interfaces).

4. TDM in high-speed mode for serial data interface.

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR and DDR2 SDRAM interface of the MPC8360E/58E.



DDR and DDR2 SDRAM AC Electrical Characteristics

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input high voltage	V _{IH}	MV _{REF} + 0.18	GV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.18	V	—
Output leakage current	I _{OZ}	—	±10	μA	4
Output high current (V _{OUT} = 1.95 V)	I _{ОН}	-15.2	-	mA	—
Output low current (V _{OUT} = 0.35 V)	I _{OL}	15.2	_	mA	—
MV _{REF} input leakage current	I _{VREF}	—	±10	μA	—
Input current (0 V ≰⁄ _{IN} ≤OV _{DD})	I _{IN}	—	±10	μA	_

Table 16. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V (continued)

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.

- 2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
- 3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
- 4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

This table provides the DDR capacitance when $GV_{DD}(typ) = 2.5$ V.

Table 17. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C _{DIO}	_	0.5	pF	1

Note:

1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25° C, V_{OUT} = $GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM interface when $GV_{DD}(typ) = 1.8 V$.

Table 18. DDR2 SDRAM Input AC Timing Specifications for GV_{DD}(typ) = 1.8 V

At recommended operating conditions with GV_{DD} of 1.8 V ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V _{IL}	—	MV _{REF} – 0.25	V	—
AC input high voltage	V _{IH}	MV _{REF} + 0.25	_	V	_



GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

8.2.2.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 30. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
RX_CLK clock period 10 Mbps	t _{MRX}	—	400	_	ns
RX_CLK clock period 100 Mbps	t _{MRX}	—	40	—	ns
RX_CLK duty cycle	t _{MRXH} /t _{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t _{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t _{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise time, (20% to 80%)	t _{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time, (80% to 20%)	t _{MRXF}	1.0	—	4.0	ns

Note:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

This figure provides the AC test load.





This figure shows the MII receive AC timing diagram.



Figure 14. MII Receive AC Timing Diagram



GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

8.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

Table 34. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
PMA_RX_CLK clock period	t _{TRX}	_	16.0	_	ns	—
PMA_RX_CLK skew	t _{SKTRX}	7.5	_	8.5	ns	—
RX_CLK duty cycle	t _{TRXH} /t _{TRX}	40	_	60	%	—
RCG[9:0] setup time to rising PMA_RX_CLK	t _{TRDVKH}	2.5	—		ns	2
RCG[9:0] hold time to rising PMA_RX_CLK	t _{trdxkh}	1.0	_	_	ns	2
RX_CLK clock rise time, $V_{IL}(min)$ to $V_{IH}(max)$	t _{TRXR}	0.7	_	2.4	ns	—
RX_CLK clock fall time, $V_{IH}(max)$ to $V_{IL}(min)$	t _{TRXF}	0.7	_	2.4	ns	—

Notes:

- 1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).}
- 2. Setup and hold time of even numbered RCG are measured from riding edge of PMA_RX_CLK1. Setup and hold time of odd numbered RCG are measured from riding edge of PMA_RX_CLK0.

This figure shows the TBI receive AC timing diagram.



Figure 19. TBI Receive AC Timing Diagram



I2C AC Electrical Specifications

11.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interface of the device.

Table 45. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 44).

Parameter	Symbol ¹	Min	Max	Unit	Note
SCL clock frequency	f _{I2C}	0	400	kHz	2
Low period of the SCL clock	t _{I2CL}	1.3	_	μs	—
High period of the SCL clock	t _{I2CH}	0.6	_	μs	—
Setup time for a repeated START condition	t _{I2SVKH}	0.6	_	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL}	0.6	_	μs	_
Data setup time	t _{I2DVKH}	100	_	ns	3
Data hold time: CBUS compatible masters I ² C bus devices	t _{I2DXKL}	$\frac{1}{0^2}$	 0.9 ³	μs	—
Rise time of both SDA and SCL signals	t _{I2CR}	20 + 0.1 C _b ⁴	300	ns	—
Fall time of both SDA and SCL signals	t _{I2CF}	20 + 0.1 C _b ⁴	300	ns	—
Set-up time for STOP condition	t _{l2PVKH}	0.6	_	μs	—
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	_	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times \text{OV}_{\text{DD}}$	_	V	_
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times \text{OV}_{\text{DD}}$	_	V	_

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional}

block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

 The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of the falling edge of SCL.

3. The maximum t_{12DVKH} has only to be met if the device does not stretch the LOW period (t_{12CL}) of the SCL signal.

4. C_B = capacitance of one bus line in pF.



This figure shows the PCI input AC timing conditions.



Figure 37. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.



13 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8360E/58E.

13.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the device timer pins, including TIN, TOUT, TGATE, and RTC_CLK.

Table 49. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	_	V
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	$0 V \leq V_{IN} \leq OV_{DD}$	_	±10	μA



IPIC AC Timing Specifications

15.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 54. IPIC Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
IPIC inputs—minimum pulse width	t _{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any
external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when
working in edge triggered mode.

16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8360E/58E.

16.1 SPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the device SPI.

Table 55. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	0 V ≤V _{IN} ≤OV _{DD}	_	±10	μA

16.2 SPI AC Timing Specifications

This table and provide the SPI input and output AC timing specifications.

Table 56. SPI AC Timing Specifications¹

Characteristic	Symbol ²	Min	Мах	Unit
SPI outputs—Master mode (internal clock) delay	t _{NIKHOX} t _{NIKHOV}	0.3	8	ns
SPI outputs—Slave mode (external clock) delay	t _{NEKHOX} t _{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t _{NIIVKH}	8	—	ns
SPI inputs—Master mode (internal clock) input hold time	t _{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t _{NEIVKH}	4	—	ns



Mechanical Dimensions of the TBGA Package

20.2 Mechanical Dimensions of the TBGA Package

This figure depicts the mechanical dimensions and bottom surface nomenclature of the device, 740-TBGA package.



Figure 53. Mechanical Dimensions and Bottom Surface Nomenclature of the TBGA Package



able 66. MPC8360E TBGA	Pinout Listing	(continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Notes
CE_PA[22]	AF3	I/O	OV _{DD}	—
CE_PA[23:26]	C18, D18, E18, A18	I/O	LV _{DD} 1	—
CE_PA[27:28]	AF2, AE6	I/O	OV _{DD}	—
CE_PA[29]	B19	I/O	LV _{DD} 1	—
CE_PA[30]	AE5	I/O	OV _{DD}	—
CE_PA[31]	F16	I/O	LV _{DD} 1	—
CE_PB[0:27]	AE2, AE1, AD5, AD3, AD2, AC6, AC5, AC4, AC2, AC1, AB5, AB4, AB3, AB1, AA6, AA4, AA2, Y6, Y4, Y3, Y2, Y1, W6, W5, W2, V5, V3, V2	I/O	OV _{DD}	_
CE_PC[0:1]	V1, U6	I/O	OV _{DD}	—
CE_PC[2:3]	C16, A15	I/O	LV _{DD} 1	—
CE_PC[4:6]	U4, U3, T6	I/O	OV _{DD}	—
CE_PC[7]	C19	I/O	LV _{DD} 2	_
CE_PC[8:9]	A4, C5	I/O	LV _{DD} 0	_
CE_PC[10:30]	T5, T4, T2, T1, R5, R3, R1, C11, D12, F13, B10, C10, E12, A9, B8, D10, A14, E15, B14, D15, AH2	I/O	OV _{DD}	
CE_PD[0:27]	E11, D9, C8, F11, A7, E9, C7, A6, F10, B6, D7, E8, B5, A5, C2, E4, F5, B1, D2, G5, D1, E2, H6, F3, E1, F2, G3, H4	I/O	OV _{DD}	_
CE_PE[0:31]	K3, J2, F1, G2, J5, H3, G1, H2, K6, J3, K5, K4, L6, P6, P4, P3, P1, N4, N5, N2, N1, M2, M3, M5, M6, L1, L2, L4, E14, C13, C14, B13	I/O	OV _{DD}	_
CE_PF[0:3]	F14, D13, A12, A11	I/O	OV _{DD}	—
	Clocks			
PCI_CLK_OUT[0]/CE_PF[26]	B22	I/O	LV _{DD} 2	
PCI_CLK_OUT[1:2]/CE_PF[27:28]	D22, A23	I/O	OV _{DD}	
CLKIN	E37	I	OV _{DD}	
PCI_CLOCK/PCI_SYNC_IN	M36	I	OV _{DD}	_
PCI_SYNC_OUT/CE_PF[29]	D37	I/O	OV _{DD}	3
	JTAG			
тск	K33	I	OV _{DD}	_
TDI	K34	I	OV _{DD}	4
TDO	H37	0	OV _{DD}	3
TMS	J36	I	OV _{DD}	4
TRST	L32		OV _{DD}	4
	Test		1	
TEST	L35	I	OV _{DD}	7
TEST_SEL	AU34	I	GV _{DD}	7



Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV _{DD} 0	D5, D6	Power for UCC1 Ethernet interface (2.5 V, 3.3 V)	LV _{DD} 0	
LV _{DD} 1	C17, D16	Power for UCC2 Ethernet interface option 1 (2.5 V, 3.3 V)	LV _{DD} 1	9
LV _{DD} 2	B18, E21	Power for UCC2 Ethernet interface option 2 (2.5 V, 3.3 V)	LV _{DD} 2	9
V _{DD}	C36, D29, D35, E16, F9, F12, F15, F17, F18, F20, F21, F23, F25, F26, F29, F31, F32, F33, G6, J6, K32, M32, N6, P33, R6, R32, U32, V6, Y5, Y32, AB6, AB33, AD6, AF32, AK6, AL6, AM7, AM9, AM10, AM11, AM12, AM13, AM14, AM15, AM18, AM21, AM25, AM28, AM32, AN15, AN21, AN26, AU9, AU17	Power for core (1.2 V)	V _{DD}	_
OV _{DD}	A10, B9, B15, B32, C1, C12, C22, C29, D24, E3, E10, E27, G4, H35, J1, J35, K2, M4, N3, N34, R2, R37, T36, U2, U33, V4, V34, W3, Y35, Y37, AA1, AA36, AB2, AB34	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV _{DD}	_
MVREF1	AN20	I	DDR reference voltage	—
MVREF2	AU32	I	DDR reference voltage	_
SPARE1	B11	I/O	OV _{DD}	8
SPARE3	AH32		GV _{DD}	8
SPARE4	AU18	_	GV _{DD}	7
SPARE5	AP1	_	GV _{DD}	8

Table 66. MPC8360E TBGA Pinout Listing (continued)



Core PLL Configuration

21.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). This table shows the encodings for RCWL[COREPLL]. COREPLL values not listed in this table should be considered reserved.

RC	WL[COREP	LL]	core_clk:csb_clk	VCO divider	
0–1	2–5	6	Ratio		
nn	0000	n	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)	
00	0001	0	1:1	÷2	
01	0001	0	1:1	÷4	
10	0001	0	1:1	÷8	
11	0001	0	1:1	÷8	
00	0001	1	1.5:1	÷2	
01	0001	1	1.5:1	÷4	
10	0001	1	1.5:1	÷8	
11	0001	1	1.5:1	÷8	
00	0010	0	2:1	÷2	
01	0010	0	2:1	÷4	
10	0010	0	2:1	÷8	
11	0010	0	2:1	÷8	
00	0010	1	2.5:1	÷2	
01	0010	1	2.5:1	÷4	
10	0010	1	2.5:1	÷8	
11	0010	1	2.5:1	÷8	
00	0011	0	3:1	÷2	
01	0011	0	3:1	÷4	
10	0011	0	3:1	÷8	
11	0011	0	3:1	÷8	

Table 73. e300 Core PLL Configuration

NOTE

Core VCO frequency = Core frequency \times VCO divider. The VCO divider (RCWL[COREPLL[0:1]]) must be set properly so that the core VCO frequency is in the range of 800–1800 MHz. Having a core frequency below the CSB frequency is not a possible option because the core frequency must be equal to or greater than the CSB frequency.



QUICC Engine Block PLL Configuration

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF])
11101	0	× 29
11110	0	× 30
11111	0	× 31
00011	1	× 1.5
00101	1	× 2.5
00111	1	× 3.5
01001	1	× 4.5
01011	1	× 5.5
01101	1	× 6.5
01111	1	× 7.5
10001	1	× 8.5
10011	1	× 9.5
10101	1	× 10.5
10111	1	× 11.5
11001	1	× 12.5
11011	1	× 13.5
11101	1	× 14.5

Table 74. QUICC Engine Block PLL Multiplication Factors (continued)

Note:

1. Reserved modes are not listed.

The RCWL[CEVCOD] denotes the QUICC Engine Block PLL VCO internal frequency as shown in this table.

Table 75. QUICC Engine Block PLL VCO Divider

RCWL[CEVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine block VCO frequency is in the range of 600–1400 MHz. The QUICC Engine block frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine block frequencies should be selected according to the performance requirements.



This figure shows the PLL power supply filter circuit.



Figure 56. PLL Power Supply Filter Circuit

23.3 Decoupling Recommendations

Due to large address and data buses as well as high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the device system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pins of the device. These decoupling capacitors should receive their power from separate V_{DD} , OV_{DD} , GV_{DD} , and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

Additionally, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , OV_{DD} , GV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μ F (AVX TPS tantalum or Sanyo OSCON).

23.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD} , GV_{DD} , or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and GND pins of the device.

23.5 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 57). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_p is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_p then becomes the resistance of the pull-up devices. R_p and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.