NXP USA Inc. - KMPC8358EVVAGDG Datasheet





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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8358evvagdg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



This figure shows the MPC8358E block diagram.



Figure 2. MPC8358E Block Diagram

Major features of the MPC8360E/58E are as follows:

- e300 PowerPC processor core (enhanced version of the MPC603e core)
 - Operates at up to 667 MHz (for the MPC8360E) and 400 MHz (for the MPC8358E)
 - High-performance, superscalar processor core
 - Floating-point, integer, load/store, system register, and branch processing units
 - 32-Kbyte instruction cache, 32-Kbyte data cache
 - Lockable portion of L1 cache
 - Dynamic power management
 - Software-compatible with the Freescale processor families implementing the Power Architecture[™] technology
- QUICC Engine unit
 - Two 32-bit RISC controllers for flexible support of the communications peripherals, each operating up to 500 MHz (for the MPC8360E) and 400 MHz (for the MPC8358E)
 - Serial DMA channel for receive and transmit on all serial channels
 - QUICC Engine module peripheral request interface (for SEC, PCI, IEEE Std. 1588TM)
 - Eight universal communication controllers (UCCs) on the MPC8360E and six UCCs on the MPC8358E supporting the following protocols and interfaces (not all of them simultaneously):
 - IEEE 1588 protocol supported



- 10/100 Mbps Ethernet/IEEE Std. 802.3TM CDMA/CS interface through a media-independent interface (MII, RMII, RGMII)¹
- 1000 Mbps Ethernet/IEEE 802.3 CDMA/CS interface through a media-independent interface (GMII, RGMII, TBI, RTBI) on UCC1 and UCC2
- 9.6-Kbyte jumbo frames
- ATM full-duplex SAR, up to 622 Mbps (OC-12/STM-4), AAL0, AAL1, and AAL5 in accordance ITU-T I.363.5
- ATM AAL2 CPS, SSSAR, and SSTED up to 155 Mbps (OC-3/STM-1) Mbps full duplex (with 4 CPS packets per cell) in accordance ITU-T I.366.1 and I.363.2
- ATM traffic shaping for CBR, VBR, UBR, and GFR traffic types compatible with ATM forum TM4.1 for up to 64-Kbyte simultaneous ATM channels
- ATM AAL1 structured and unstructured circuit emulation service (CES 2.0) in accordance with ITU-T I.163.1 and ATM Forum af-vtoa-00-0078.000
- IMA (Inverse Multiplexing over ATM) for up to 31 IMA links over 8 IMA groups in accordance with the ATM forum AF-PHY-0086.000 (Version 1.0) and AF-PHY-0086.001 (Version 1.1)
- ATM Transmission Convergence layer support in accordance with ITU-T I.432
- ATM OAM handling features compatible with ITU-T I.610
- PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686, and 3153
- IP support for IPv4 packets including TOS, TTL, and header checksum processing
- Ethernet over first mile IEEE 802.3ah
- Shim header
- Ethernet-to-Ethernet/AAL5/AAL2 inter-working
- L2 Ethernet switching using MAC address or IEEE Std. 802.1P/Q[™] VLAN tags
- ATM (AAL2/AAL5) to Ethernet (IP) interworking in accordance with RFC2684 including bridging of ATM ports to Ethernet ports
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- AAL2 protocol rate up to 4 CPS at OC-3/STM-1 rate
- Packet over Sonet (POS) up to 622-Mbps full-duplex 124 MultiPHY
- POS hardware; microcode must be loaded as an IRAM package
- Transparent up to 70-Mbps full-duplex
- HDLC up to 70-Mbps full-duplex
- HDLC BUS up to 10 Mbps
- Asynchronous HDLC
- UART
- BISYNC up to 2 Mbps
- User-programmable Virtual FIFO size
- QUICC multichannel controller (QMC) for 64 TDM channels
- One multichannel communication controller (MCC) only on the MPC8360E supporting the following:
 - 256 HDLC or transparent channels
 - 128 SS7 channels
 - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces
- Two UTOPIA/POS interfaces on the MPC8360E supporting 124 MultiPHY each (optional 2*128 MultiPHY with extended address) and one UTOPIA/POS interface on the MPC8358E supporting 31/124 MultiPHY
- Two serial peripheral interfaces (SPI); SPI2 is dedicated to Ethernet PHY management

1.SMII or SGMII media-independent interface is not currently supported.



- Eight TDM interfaces on the MPC8360E and four TDM interfaces on the MPC8358E with 1-bit mode for E3/T3 rates in clear channel
- Sixteen independent baud rate generators and 30 input clock pins for supplying clocks to UCC and MCC serial channels (MCC is only available on the MPC8360E)
- Four independent 16-bit timers that can be interconnected as four 32-bit timers
- Interworking functionality:
 - Layer 2 10/100-Base T Ethernet switch
 - ATM-to-ATM switching (AAL0, 2, 5)
 - Ethernet-to-ATM switching with L3/L4 support
 - PPP interworking
- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, 802.11i®, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs).
 - Public key execution unit (PKEU) supporting the following:
 - RSA and Diffie-Hellman
 - Programmable field size up to 2048 bits
 - Elliptic curve cryptography
 - F2m and F(p) modes
 - Programmable field size up to 511 bits
 - Data encryption standard execution unit (DEU)
 - DES, 3DES
 - Two key (K1, K2) or three key (K1, K2, K3)
 - ECB and CBC modes for both DES and 3DES
 - Advanced encryption standard unit (AESU)
 - Implements the Rinjdael symmetric key cipher
 - Key lengths of 128, 192, and 256 bits, two key
 - ECB, CBC, CCM, and counter modes
 - ARC four execution unit (AFEU)
 - Implements a stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
 - Message digest execution unit (MDEU)
 - SHA with 160-, 224-, or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either SHA or MD5 algorithm
 - Random number generator (RNG)
 - Four crypto-channels, each supporting multi-command descriptor chains
 - Static and/or dynamic assignment of crypto-execution units via an integrated controller
 - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
 - Storage/NAS XOR parity generation accelerator for RAID applications
- Dual DDR SDRAM memory controllers on the MPC8360E and a single DDR SDRAM memory controller on the MPC8358E
 - Programmable timing supporting both DDR1 and DDR2 SDRAM
 - On the MPC8360E, the DDR buses can be configured as two 32-bit buses or one 64-bit bus; on the MPC8358E, the DDR bus can be configured as a 32- or 64-bit bus
 - 32- or 64-bit data interface, up to 333 MHz (for the MPC8360E) and 266 MHz (for the MPC8358E) data rate
 - Four banks of memory, each up to 1 Gbyte



- Programmable highest priority request
- Four groups of interrupts with programmable priority
- External and internal interrupts directed to communication processor
- Redirects interrupts to external INTA pin when in core disable mode
- Unique vector number for each interrupt source
- Dual industry-standard I²C interfaces
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
 - System initialization data is optionally loaded from I²C-1 EPROM by boot sequencer embedded hardware
- DMA controller
 - Four independent virtual channels
 - Concurrent execution across multiple channels with programmable bandwidth control
 - All channels accessible by local core and remote PCI masters
 - Misaligned transfer capability
 - Data chaining and direct mode
 - Interrupt on completed segment and chain
 - DMA external handshake signals: DMA_DREQ[0:3]/DMA_DACK[0:3]/DMA_DONE[0:3]. There is one set for each DMA channel. The pins are multiplexed to the parallel IO pins with other QE functions.
- DUART
 - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
 - Programming model compatible with the original 16450 UART and the PC16550D
- System timers
 - Periodic interrupt timer
 - Real-time clock
 - Software watchdog timer
 - Eight general-purpose timers
- IEEE Std. 1149.1[™]-compliant, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8360E/58E. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.



DDR and DDR2 SDRAM AC Electrical Characteristics

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 21 and Table 22 provide the output AC timing specifications and measurement conditions for the DDR and DDR2 SDRAM interface.

Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter ⁸	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time, (MCK[n]/MCK[n] crossing)	t _{MCK}	6	10	ns	2
Skew between any MCK to ADDR/CMD 333 MHz 266 MHz 200 MHz	t _{AOSKEW}	-1.0 -1.1 -1.2	0.2 0.3 0.4	ns	3
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz 200 MHz	^t DDKHAS	2.1 2.8 3.5	_	ns	4
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz—DDR1 266 MHz—DDR2 200 MHz	t _{DDKHAX}	2.0 2.7 2.8 3.5		ns	4
MCS(n) output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t _{DDKHCS}	2.1 2.8 3.5	_	ns	4
MCS(n) output hold with respect to MCK 333 MHz 266 MHz 200 MHz	t _{DDKHCX}	2.0 2.7 3.5	_	ns	4
MCK to MDQS	t _{DDKHMH}	-0.8	0.7	ns	5, 9
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	t _{DDKHDS} , t _{DDKLDS}	0.7 1.0 1.2	_	ns	6
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	t _{DDKHDX} , t _{DDKLDX}	0.7 1.0 1.2	_	ns	6
MDQS preamble start	t _{DDKHMP}	$-0.5\timest_{MCK}-0.6$	$-0.5\timest_{\text{MCK}}\text{+}0.6$	ns	7



DDR and DDR2 SDRAM AC Electrical Characteristics

This figure provides the AC test load for the DDR bus.



Figure 8. DDR AC Test Load

Table 22. DDR and DDR2 SDRAM Measurement Conditions

Symbol	DDR	DDR2	Unit	Notes
V _{TH}	MV _{REF} ± 0.31 V	MV _{REF} ± 0.25 V	V	1
V _{OUT}	$0.5 \times \text{ GV}_{\text{DD}}$	$0.5 \times \text{ GV}_{\text{DD}}$	V	2

Notes:

1. Data input threshold measurement point.

2. Data output measurement point.

This figure shows the DDR SDRAM output timing diagram for source synchronous mode.



Figure 9. DDR SDRAM Output Timing Diagram for Source Synchronous Mode



Local Bus DC Electrical Characteristics

8.3.3 IEEE 1588 Timer AC Specifications

This table provides the IEEE 1588 timer AC specifications.

Table 38. IEEE 1588 Timer AC Specifications

Parameter	Symbol	Min	Мах	Unit	Notes
Timer clock frequency	t _{TMRCK}	0	70	MHz	1
Input setup to timer clock	t _{TMRCKS}	—	—	—	2, 3
Input hold from timer clock	t _{TMRCKH}	—	—	—	2, 3
Output clock to output valid	t _{GCLKNV}	0	6	ns	_
Timer alarm to output valid	t _{TMRAL}	_	_	_	2

Notes:

1. The timer can operate on rtc_clock or tmr_clock. These clocks get muxed and any one of them can be selected. The minimum and maximum requirement for both rtc_clock and tmr_clock are the same.

- 2. These are asynchronous signals.
- 3. Inputs need to be stable at least one TMR clock.

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8360E/58E.

9.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface.

Table 39. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
High-level output voltage, I _{OH} = −100 μA	V _{OH}	OV _{DD} - 0.4	—	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V _{OL}	—	0.2	V
Input current	I _{IN}	—	±10	μA

9.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface of the device.

Table 40. Local Bus General Timing Parameters—DLL Enabled

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus cycle time	t _{LBK}	7.5	_	ns	2
Input setup to local bus clock (except LUPWAIT)	t _{LBIVKH1}	1.7	_	ns	3, 4
LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.9	_	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	t _{LBIXKH1}	1.0		ns	3, 4



This figure provides the AC test load for the I^2C .



Figure 34. I²C AC Test Load

This figure shows the AC timing diagram for the I^2C bus.



12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8360E/58E.

12.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface of the device.

Table 46. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Мах	Unit
High-level input voltage	V _{IH}	$V_{OUT} \ge V_{OH}$ (min) or	$0.5\times\text{OV}_\text{DD}$	OV _{DD} + 0.5	V
Low-level input voltage	V _{IL}	V _{OUT} ≤V _{OL} (max)	-0.5	$0.3 imes OV_{DD}$	V
High-level output voltage	V _{OH}	I _{OH} = -500 μA	$0.9 imes OV_{DD}$	—	V
Low-level output voltage	V _{OL}	l _{OL} = 1500 μA	—	$0.1 imes OV_{DD}$	V
Input current	I _{IN}	0 V ≤V _{IN} ¹ ≤OV _{DD}	—	±10	μA

12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the device. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. This table provides the PCI AC timing specifications at 66 MHz.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Clock to output valid	t _{PCKHOV}	_	6.0	ns	2, 5
Output hold from clock	t _{PCKHOX}	1	—	ns	2

Table 47. PCI AC Timing Specifications at 66 MHz

PCI AC Electrical Specifications

Table 47. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Clock to output high impedance	t _{PCKHOZ}	_	14	ns	2, 3
Input setup to clock	t _{PCIVKH}	3.0	_	ns	2, 4
Input hold from clock	t _{PCIXKH}	0.3	_	ns	2, 4, 6

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
 </sub>
- 2. See the timing measurement conditions in the PCI 2.2 Local Bus Specifications.
- 3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.
- 5. In rev. 2.0 silicon, due to errata, t_{PCIHOV} maximum is 6.6 ns. Refer to Errata PCI21 in Chip Errata for the MPC8360E, Rev. 1.
- 6. In rev. 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Refer to Errata PCI17 in Chip Errata for the MPC8360E, Rev. 1.

Table 48. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	t _{PCKHOV}	_	11	ns	2
Output hold from clock	t _{PCKHOX}	2	-	ns	2
Clock to output high impedance	t _{PCKHOZ}	_	14	ns	2, 3
Input setup to clock	t _{PCIVKH}	7.0	_	ns	2, 2
Input hold from clock	t _{PCIXKH}	0.3	_	ns	2, 4, 5

Notes:

- The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
- 2. See the timing measurement conditions in the PCI 2.2 Local Bus Specifications.
- 3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.
- 5. In rev. 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Refer to Errata PCI17 in Chip Errata for the MPC8360E, Rev. 1.

This figure provides the AC test load for PCI.



Figure 36. PCI AC Test Load



20 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8360E/58E is available in a tape ball grid array (TBGA), see Section 20.1, "Package Parameters for the TBGA Package," and Section 20.2, "Mechanical Dimensions of the TBGA Package," for information on the package.

20.1 Package Parameters for the TBGA Package

The package parameters for rev. 2.0 silicon are as provided in the following list. The package type is $37.5 \text{ mm} \times 37.5 \text{ mm}$, 740 tape ball grid array (TBGA).

Package outline	$37.5 \text{ mm} \times 37.5 \text{ mm}$
Interconnects	740
Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder Balls	62 Sn/36 Pb/2 Ag (ZU package)
	95.5 Sn/0.5 Cu/4Ag (VV package)
Ball diameter (typical)	0.64 mm



Pinout Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC1_MCKE[0:1]	AL32, AU33	0	GV _{DD}	3
MEMC1_MCK[0:1]	AK37, AT37	0	GV _{DD}	—
MEMC1_MCK[2:3]/ MEMC2_MCK[0:1]	AN1, AR2	0	GV _{DD}	—
MEMC1_MCK[4:5]/ MEMC2_MCKE[0:1]	AN25, AK1	0	GV _{DD}	
MEMC1_MCK[0:1]	AL37, AT36	0	GV _{DD}	_
MEMC1_MCK[2:3]/ MEMC2_MCK[0:1]	AP2, AT2	0	GV _{DD}	_
MEMC1_MCK[4]/ MEMC2_MDM[8]	AN24	0	GV _{DD}	_
MEMC1_MCK[5]/ MEMC2_MDQS[8]	AL1	0	GV _{DD}	
MDIC[0:1]	АН6, АР30	I/O	GV _{DD}	10
Sec	ondary DDR SDRAM Memory Controller Interface			
MEMC2_MECC[0:7]	AN16, AP18, AM16, AM17, AN17, AP13, AP15, AN13	I/O	GV _{DD}	—
MEMC2_MBA[0:2]	AU12, AU15, AU13	0	GV _{DD}	—
MEMC2_MA[0:14]	AT12, AP11, AT13, AT14, AR13, AR15, AR16, AT16, AT18, AT17, AP10, AR20, AR17, AR14, AR11	0	GV _{DD}	_
MEMC2_MWE	AU10	0	GV _{DD}	_
MEMC2_MRAS	AT11	0	GV _{DD}	—
MEMC2_MCAS	AU11	0	GV _{DD}	—
	PCI			
PCI_INTA/IRQ_OUT/CE_PF[5]	A20	I/O	LV _{DD} 2	2
PCI_RESET_OUT/CE_PF[6]	E19	I/O	LV _{DD} 2	—
PCI_AD[31:30]/CE_PG[31:30]	D20, D21	I/O	LV _{DD} 2	—
PCI_AD[29:25]/CE_PG[29:25]	A24, B23, C23, E23, A26	I/O	OV _{DD}	_
PCI_AD[24]/CE_PG[24]	B21	I/O	LV _{DD} 2	
PCI_AD[23:0]/CE_PG[23:0]	C24, C25, D25, B25, E24, F24, A27, A28, F27, A30, C30, D30, E29, B31, C31, D31, D32, A32, C33, B33, F30, E31, A34, D33	I/O	OV _{DD}	
PCI_C/BE[3:0]/CE_PF[10:7]	E22, B26, E28, F28	I/O	OV _{DD}	—
PCI_PAR/CE_PF[11]	D28	I/O	OV _{DD}	—
PCI_FRAME/CE_PF[12]	D26	I/O	OV _{DD}	5
PCI_TRDY/CE_PF[13]	C27	I/O	OV _{DD}	5
PCI_IRDY/CE_PF[14]	C28	I/O	OV _{DD}	5
PCI_STOP/CE_PF[15]	B28	I/O	OV_{DD}	5



Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_DEVSEL/CE_PF[16]	E26	I/O	OV _{DD}	5
PCI_IDSEL/CE_PF[17]	F22	I/O	OV _{DD}	
PCI_SERR/CE_PF[18]	B29	I/O	OV _{DD}	5
PCI_PERR/CE_PF[19]	A29	I/O	OV _{DD}	5
PCI_REQ[0]/CE_PF[20]	F19	I/O	LV _{DD} 2	—
PCI_REQ[1]/CPCI_HS_ES/ CE_PF[21]	A21	I/O	LV _{DD} 2	—
PCI_REQ[2]/CE_PF[22]	C21	I/O	LV _{DD} 2	
PCI_GNT[0]/CE_PF[23]	E20	I/O	LV _{DD} 2	
PCI_GNT[1]/CPCI1_HS_LED/ CE_PF[24]	B20	I/O	LV _{DD} 2	
PCI_GNT[2]/CPCI1_HS_ENUM/ CE_PF[25]	C20	I/O	LV _{DD} 2	
PCI_MODE	D36	I	OV _{DD}	
M66EN/CE_PF[4]	B37	I/O	OV _{DD}	—
	Local Bus Controller Interface			
LAD[0:31]	N32, N33, N35, N36, P37, P32, P34, R36, R35, R34, R33, T37, T35, T34, T33, U37, T32, U36, U34, V36, V35, W37, W35, V33, V32, W34, Y36, W32, AA37, Y33, AA35, AA34	I/O	OV _{DD}	_
LDP[0]/CKSTOP_OUT	AB37	I/O	OV _{DD}	
LDP[1]/CKSTOP_IN	AB36	I/O	OV _{DD}	
LDP[2]/LCS[6]	AB35	I/O	OV _{DD}	
LDP[3]/LCS[7]	AA33	I/O	OV _{DD}	
LA[27:31]	AC37, AA32, AC36, AC34, AD36	0	OV _{DD}	
LCS[0:5]	AD33, AG37, AF34, AE33, AD32, AH37	0	OV_{DD}	
LWE[0:3]/LSDDQM[0:3]/LBS[0:3]	AG35, AG34, AH36, AE32	0	OV_{DD}	
LBCTL	AD35	0	OV_{DD}	
LALE	M37	0	OV_{DD}	
LGPL0/LSDA10/cfg_reset_source0	AB32	I/O	OV_{DD}	
LGPL1/LSDWE/cfg_reset_source1	AE37	I/O	OV_{DD}	
LGPL2/LSDRAS/LOE	AC33	0	OV_{DD}	
LGPL3/LSDCAS/cfg_reset_source2	AD34	I/O	OV_{DD}	
LGPL4/LGTA/LUPWAIT/LPBSE	AE35	I/O	OV_{DD}	
LGPL5/cfg_clkin_div	AF36	I/O	OV_{DD}	
LCKE	G36	0	OV _{DD}	_
LCLK[0]	J33	0	OV _{DD}	—
LCLK[1]/LCS[6]	J34	0	OV _{DD}	—



Pinout Listings

21 Clocking

This figure shows the internal distribution of clocks within the MPC8360E.



Figure 54. MPC8360E Clock Subsystem





ordered, see Section 24.1, "Part Numbers Fully Addressed by this Document," for part ordering details and contact your Freescale sales representative or authorized distributor for more information.

Characteristic ¹	400 MHz	533 MHz	667 MHz ²	Unit
e300 core frequency (<i>core_clk</i>)	266–400	MHz		
Coherent system bus frequency (<i>csb_clk</i>)		133–333		MHz
QUICC Engine frequency ³ (<i>ce_clk</i>)	266–500			MHz
DDR and DDR2 memory bus frequency (MCLK) ⁴	100–166.67			
Local bus frequency (LCLK <i>n</i>) ⁵	ency (LCLK <i>n</i>) ⁵ 16.67–133			MHz
PCI input frequency (CLKIN or PCI_CLK)	but frequency (CLKIN or PCI_CLK) 25–66.67			MHz
Security core maximum internal operating frequency	133	133	166	MHz

Table 69. Operating Frequencies for the TBGA Package

Notes:

- 1. The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
- 2. The 667 MHz core frequency is based on a 1.3 V V_{DD} supply voltage.
- 3. The 500 MHz QE frequency is based on a 1.3 V V_{DD} supply voltage.
- 4. The DDR data rate is 2x the DDR memory bus frequency.
- 5. The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWL[LBCM]).

21.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] and RCWL[SVCOD] parameters. This table shows the multiplication factor encodings for the system PLL.

RCWL[SPMF]	System PLL Multiplication Factor
0000	× 16
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11

Table 70. System PLL Multiplication Factors



21.3 QUICC Engine Block PLL Configuration

The QUICC Engine block PLL is controlled by the RCWL[CEPMF], RCWL[CEPDF], and RCWL[CEVCOD] parameters. This table shows the multiplication factor encodings for the QUICC Engine block PLL.

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF])
00000	0	× 16
00001	0	Reserved
00010	0	× 2
00011	0	× 3
00100	0	× 4
00101	0	× 5
00110	0	× 6
00111	0	× 7
01000	0	× 8
01001	0	× 9
01010	0	× 10
01011	0	× 11
01100	0	× 12
01101	0	× 13
01110	0	× 14
01111	0	× 15
10000	0	× 16
10001	0	× 17
10010	0	× 18
10011	0	× 19
10100	0	× 20
10101	0	× 21
10110	0	× 22
10111	0	× 23
11000	0	× 24
11001	0	× 25
11010	0	× 26
11011	0	× 27
11100	0	× 28

Table 74. QUICC Engine Block PLL Multiplication Factors



The QUICC Engine block VCO frequency is derived from the following equations:

 $ce_clk = (primary clock input \times CEPMF) \div (1 + CEPDF)$

QE VCO Frequency = $ce_clk \times VCO$ divider $\times (1 + CEPDF)$

21.4 Suggested PLL Configurations

To simplify the PLL configurations, the device might be separated into two clock domains. The first domain contains the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine block PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. This table shows suggested PLL configurations for 33 and 66 MHz input clocks and illustrates each of the clock domains separately. Any combination of clock domains setting with same input clock are valid. Refer to Section 21, "Clocking," for the appropriate operating frequencies for your device.

Conf No. ¹	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock Freq (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
				33 MH:	z CLKIN/PCI	SYNC_IN	Options				
s1	0100	0000100	æ	æ	33	133	266	—	8	8	8
s2	0100	0000101	æ	æ	33	133	333	_	8	∞	8
s3	0101	0000100	æ	æ	33	166	333	_	8	8	8
s4	0101	0000101	æ	æ	33	166	416			8	8
s5	0110	0000100	æ	æ	33	200	400		8	8	8
s6	0110	0000110	æ	æ	33	200	600			—	8
s7	0111	0000011	æ	æ	33	233	350		8	8	8
s8	0111	0000100	æ	æ	33	233	466			8	8
s9	0111	0000101	æ	æ	33	233	583			_	8
s10	1000	0000011	æ	æ	33	266	400		8	8	8
s11	1000	0000100	æ	æ	33	266	533			8	8
s12	1000	0000101	æ	æ	33	266	667			_	8
s13	1001	0000010	æ	æ	33	300	300		8	8	8
s14	1001	0000011	æ	æ	33	300	450	_		8	8
s15	1001	0000100	æ	æ	33	300	600	_		—	8
s16	1010	0000010	æ	æ	33	333	333	_	8	8	8
s17	1010	0000011	æ	æ	33	333	500	_		8	8
s18	1010	0000100	æ	æ	33	333	667	_		—	8
c1	æ	æ	01001	0	33			300	8	8	8
c2	æ	æ	01100	0	33	_	_	400	8	8	8
c3	æ	æ	01110	0	33	_	_	466	_	8	8
c4	æ	æ	01111	0	33			500	_	8	8

Table 76. Suggested PLL Configurations

Suggested PLL Configurations

Conf No. ¹	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock Freq (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
c5	æ	æ	10000	0	33	—	—	533	_	∞	8
c6	æ	æ	10001	0	33	—	—	566	_	_	8
	66 MHz CLKIN/PCI_SYNC_IN Options										
s1h	0011	0000110	æ	æ	66	200	400	_	8	∞	8
s2h	0011	0000101	æ	æ	66	200	500	_	—	∞	8
s3h	0011	0000110	æ	æ	66	200	600	_	—	—	8
s4h	0100	0000011	æ	æ	66	266	400	_	8	∞	8
s5h	0100	0000100	æ	æ	66	266	533	_	—	∞	8
s6h	0100	0000101	æ	æ	66	266	667	_	—	—	8
s7h	0101	0000010	æ	æ	66	333	333	_	8	∞	8
s8h	0101	0000011	æ	æ	66	333	500	_	—	∞	8
s9h	0101	0000100	æ	æ	66	333	667	_	_	—	8
c1h	æ	æ	00101	0	66	—	—	333	∞	∞	∞
c2h	æ	æ	00110	0	66	—	—	400	8	∞	8
c3h	æ	æ	00111	0	66	—	_	466	—	∞	8
c4h	æ	æ	01000	0	66	—	_	533	—	∞	8
c5h	æ	æ	01001	0	66	—	_	600	_	—	~

Table 76. Suggested PLL Configurations (continued)

Note:

1. The Conf No. consist of prefix, an index and a postfix. The prefix "s" and "c" stands for "syset" and "ce" respectively. The postfix "h" stands for "high input clock." The index is a serial number.

The following steps describe how to use above table. See Example 1.

- 2. Choose the up or down sections in the table according to input clock rate 33 MHz or 66 MHz.
- 3. Select a suitable CSB and core clock rates from Table 76. Copy the SPMF and CORE PLL configuration bits.
- 4. Select a suitable QUICC Engine block clock rate from Table 76. Copy the CEPMF and CEPDF configuration bits.
- 5. Insert the chosen SPMF, COREPLL, CEPMF and CEPDF to the RCWL fields, respectively.



Configuration Pin Muxing



Figure 57. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term} . The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD} , nominal OV_{DD} , 105° C.

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R _N	42 Target	25 Target	20 Target	Z ₀	W
R _P	42 Target	25 Target	20 Target	Z ₀	W
Differential	NA	NA	NA	Z _{DIFF}	W

Table 79. Impedance Characteristics

Note: Nominal supply voltages. See Table 1, $T_J = 105^{\circ}$ C.

23.6 Configuration Pin Muxing

The device provides the user with power-on configuration options that can be set through the use of external pull-up or pull-down resistors of 4.7 k Ω on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While HRESET is asserted however, these pins are treated as inputs. The value presented on these pins while HRESET is asserted, is latched when HRESET deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

Part Numbers Fully Addressed by this Document

Device	Package	SVR (Rev. 2.0)	SVR (Rev. 2.1)
MPC8358E	TBGA	0x804A_0020	0x804A_0021
MPC8358	TBGA	0x804B_0020	0x804B_0021

25 Document Revision History

This table provides a revision history for this document.

Table 82. Revision History

Rev. Number	Date	Substantive Change(s)
5	09/2011	 Section 2.2.1, "Power-Up Sequencing", added the current limitation "3A to 5A" for the excessive current. Section 2.1.2, "Power Supply Voltage Specification, Updated the Characteristic for TBGA (MPC8358 & MPC8360 Device) with specific frequency for Core and PLL voltages. Added table footnote 3 to Table 2. Applied table footnotes 1 and 2 to Table 10. Removed table footnotes from Table 19. Applied table footnotes 8 and 9 to Table 40. Applied table footnotes 2 and 3 to Table 41. Applied table footnotes from Table 46. Applied table footnote to last three rows of Table 65.
4	01/2011	 Updated references to the LCRR register throughout Removed references to DDR DLL mode in Section 6.2.2, "DDR and DDR2 SDRAM Output AC Timing Specifications." Changed "Junction-to-Case" to "Junction-to-Ambient" in Section 22.2.4, "Heat Sinks and Junction-to-Ambient Thermal Resistance," and Table 78, "Heat Sinks and Junction-to-Ambient Thermal Resistance of TBGA Package," titles.

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