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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

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- Programmable highest priority request
- Four groups of interrupts with programmable priority
- External and internal interrupts directed to communication processor
- Redirects interrupts to external INTA pin when in core disable mode
- Unique vector number for each interrupt source
- Dual industry-standard I²C interfaces
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
 - System initialization data is optionally loaded from I²C-1 EPROM by boot sequencer embedded hardware
- DMA controller
 - Four independent virtual channels
 - Concurrent execution across multiple channels with programmable bandwidth control
 - All channels accessible by local core and remote PCI masters
 - Misaligned transfer capability
 - Data chaining and direct mode
 - Interrupt on completed segment and chain
 - DMA external handshake signals: DMA_DREQ[0:3]/DMA_DACK[0:3]/DMA_DONE[0:3]. There is one set for each DMA channel. The pins are multiplexed to the parallel IO pins with other QE functions.
- DUART
 - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
 - Programming model compatible with the original 16450 UART and the PC16550D
- System timers
 - Periodic interrupt timer
 - Real-time clock
 - Software watchdog timer
 - Eight general-purpose timers
- IEEE Std. 1149.1[™]-compliant, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8360E/58E. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.



Table 1.	Absolute	Maximum	Ratings ¹	(continued)
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Characteristic	Symbol	Max Value	Unit	Notes
Storage temperature range	T _{STG}	-55 to 150	°C	_

Notes:

- 1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- 2. Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
- 3. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
- 4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
- 5. (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 3.
- 6. OV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 4.

2.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for the device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2.	Recommended	Operating	Conditions
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Characteristic	Symbol	Recommended Value	Unit	Notes
Core and PLL supply voltage for	V _{DD} & AV _{DD}	1.2 V ± 60 mV	V	1, 3
MPC8358 Device Part Number with Processor Frequency label of AD=266MHz and AG=400MHz & QUICC Engine Frequency label of E=300MHz & G=400MHz				
MPC8360 Device Part Number with Processor Frequency label of AG=400MHz and AJ=533MHz & QUICC Engine Frequency label of G=400MHz				
Core and PLL supply voltage for	V _{DD} & AV _{DD}	1.3 V ± 50 mV	V	1, 3
MPC8360 Device Part Number with Processor Frequency label of AL=667MHz and QUICC Engine Frequency label of H=500MHz				
DDR and DDR2 DRAM I/O supply voltage DDR DDR2	GV _{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	_
Three-speed Ethernet I/O supply voltage	LV _{DD} 0	3.3 V ± 330 mV 2.5 V ± 125 mV	V	_
Three-speed Ethernet I/O supply voltage	LV _{DD} 1	3.3 V ± 330 mV 2.5 V ± 125 mV	V	_
Three-speed Ethernet I/O supply voltage	LV _{DD} 2	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—

DC Electrical Characteristics



4.1 DC Electrical Characteristics

This table provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the device.

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Parameter	Condition	Symbol	Min	Мах	Unit
Input high voltage	—	V _{IH}	2.7	OV _{DD} + 0.3	V
Input low voltage	—	V _{IL}	-0.3	0.4	V
CLKIN input current	0 V ≤V _{IN} ≤OV _{DD}	I _{IN}	—	±10	μA
PCI_SYNC_IN input current	0 V ≤V _{IN} ≤0.5V or OV _{DD} – 0.5V ≤V _{IN} ≤OV _{DD}	I _{IN}	_	±10	μΑ
PCI_SYNC_IN input current	0.5 V ≤V _{IN} ≤OV _{DD} – 0.5 V	I _{IN}	—	±100	μA

4.2 AC Electrical Characteristics

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 8.	CLKIN	AC	Timing	Specifications
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Parameter/Condition	Symbol	Min	Typical	Мах	Unit	Notes
CLKIN/PCI_CLK frequency	f _{CLKIN}	—	—	66.67	MHz	1
CLKIN/PCI_CLK cycle time	t _{CLKIN}	15	—	_	ns	—
CLKIN/PCI_CLK rise and fall time	t _{KH} , t _{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t _{KHK} /t _{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:

- 1. **Caution:** The system, core, USB, security, and 10/100/1000 Ethernet must not exceed their respective maximum or minimum operating frequencies.
- 2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 V and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the total input jitter-short term and long term-and is guaranteed by design.
- 5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.

4.3 Gigabit Reference Clock Input Timing

This table provides the Gigabit reference clocks (GTX_CLK125) AC timing specifications.

Table 9. GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 \pm 0.125 mV/ 3.3 V \pm 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
GTX_CLK125 frequency	t _{G125}	_	125	_	MHz	_
GTX_CLK125 cycle time	t _{G125}	_	8		ns	



DDR and DDR2 SDRAM AC Electrical Characteristics

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 21 and Table 22 provide the output AC timing specifications and measurement conditions for the DDR and DDR2 SDRAM interface.

Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter ⁸	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time, (MCK[n]/MCK[n] crossing)	t _{MCK}	6	10	ns	2
Skew between any MCK to ADDR/CMD 333 MHz 266 MHz 200 MHz	t _{AOSKEW}	-1.0 -1.1 -1.2	0.2 0.3 0.4	ns	3
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz 200 MHz	^t DDKHAS	2.1 2.8 3.5	_	ns	4
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz—DDR1 266 MHz—DDR2 200 MHz	t _{ddkhax}	2.0 2.7 2.8 3.5		ns	4
MCS(n) output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t _{DDKHCS}	2.1 2.8 3.5	_	ns	4
MCS(n) output hold with respect to MCK 333 MHz 266 MHz 200 MHz	t _{DDKHCX}	2.0 2.7 3.5	_	ns	4
MCK to MDQS	t _{DDKHMH}	-0.8	0.7	ns	5, 9
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	t _{DDKHDS} , t _{DDKLDS}	0.7 1.0 1.2	_	ns	6
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	t _{DDKHDX} , t _{DDKLDX}	0.7 1.0 1.2	_	ns	6
MDQS preamble start	t _{DDKHMP}	$-0.5\timest_{MCK}-0.6$	$-0.5\timest_{\text{MCK}}\text{+}0.6$	ns	7





This section describes the DC and AC electrical specifications for the DUART interface of the MPC8360E/58E.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface of the device.

Table 23. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit	Notes
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V	—
Low-level input voltage OV _{DD}	V _{IL}	-0.3	0.8	V	—
High-level output voltage, I _{OH} = −100 μA	V _{OH}	OV _{DD} - 0.4	—	V	—
Low-level output voltage, I _{OL} = 100 μA	V _{OL}	—	0.2	V	—
Input current (0 V ≰⁄ _{IN} ≤OV _{DD})	I _{IN}	—	±10	μA	1

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface of the device.

Table 24.	DUART	AC T	iming	Speci	ifications
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Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	_
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	_	2

Notes:

- 1. Actual attainable baud rate is limited by the latency of interrupt processing.
- 2. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

8 UCC Ethernet Controller: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

8.1 Three-Speed Ethernet Controller (10/100/1000 Mbps)— GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), MII (media independent interface), RMII (reduced media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The MII, RMII, GMII, and TBI interfaces are only defined for 3.3 V, while the RGMII and RTBI interfaces are only defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet



GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

8.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

Table 34. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
PMA_RX_CLK clock period	t _{TRX}	_	16.0	_	ns	—
PMA_RX_CLK skew	t _{SKTRX}	7.5	_	8.5	ns	—
RX_CLK duty cycle	t _{TRXH} /t _{TRX}	40	_	60	%	—
RCG[9:0] setup time to rising PMA_RX_CLK	t _{TRDVKH}	2.5	—		ns	2
RCG[9:0] hold time to rising PMA_RX_CLK	t _{trdxkh}	1.0	_	_	ns	2
RX_CLK clock rise time, $V_{IL}(min)$ to $V_{IH}(max)$	t _{TRXR}	0.7	_	2.4	ns	—
RX_CLK clock fall time, $V_{IH}(max)$ to $V_{IL}(min)$	t _{TRXF}	0.7	_	2.4	ns	—

Notes:

- 1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).}
- 2. Setup and hold time of even numbered RCG are measured from riding edge of PMA_RX_CLK1. Setup and hold time of odd numbered RCG are measured from riding edge of PMA_RX_CLK0.

This figure shows the TBI receive AC timing diagram.



Figure 19. TBI Receive AC Timing Diagram



8.2.5 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 35. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
Data to clock output skew (at transmitter)	t _{SKRGTKHDX} t _{SKRGTKHDV}	-0.5 		— 0.5	ns	7
Data to clock input skew (at receiver)	t _{SKRGDXKH} t _{SKRGDVKH}	1.0		 2.6	ns	2
Clock cycle duration	t _{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	t _{RGTH} /t _{RGT}	45	50	55	%	4, 5
Duty cycle for 10BASE-T and 100BASE-TX	t _{RGTH} /t _{RGT}	40	50	60	%	3, 5
Rise time (20–80%)	t _{RGTR}	—		0.75	ns	
Fall time (20–80%)	t _{RGTF}	—	_	0.75	ns	
GTX_CLK125 reference clock period	t _{G125}	—	8.0	_	ns	6
GTX_CLK125 reference clock duty cycle	t _{G125H} /t _{G125}	47		53	%	

Notes:

- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (Rx) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- 2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns can be added to the associated clock signal.
- 3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
- 4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- 5. Duty cycle reference is LV_{DD}/2.
- 6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
- 7. In rev. 2.0 silicon, due to errata, t_{SKRGTKHDX} minimum is –2.3 ns and t_{SKRGTKHDV} maximum is 1 ns for UCC1, 1.2 ns for UCC2 option 1, and 1.8 ns for UCC2 option 2. In rev. 2.1 silicon, due to errata, t_{SKRGTKHDX} minimum is –0.65 ns for UCC2 option 1 and –0.9 for UCC2 option 2, and t_{SKRGTKHDV} maximum is 0.75 ns for UCC1 and UCC2 option 1 and 0.85 for UCC2 option 2. Refer to Errata QE_ENET10 in *Chip Errata for the MPC8360E, Rev. 1*. UCC1 does meet t_{SKRGTKHDX} minimum for rev. 2.1 silicon.



Ethernet Management Interface Electrical Characteristics

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.



Figure 20. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI, and RTBI are specified in Section 8.1, "Three-Speed Ethernet Controller (10/100/1000 Mbps)— GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage (3.3 V)	OV _{DD}	-	_	2.97	3.63	V
Output high voltage	V _{OH}	$I_{OH} = -1.0 \text{ mA}$	$OV_{DD} = Min$	2.10	OV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	$OV_{DD} = Min$	GND	0.50	V
Input high voltage	V _{IH}	-	_	2.00	—	V
Input low voltage	V _{IL}	—		—	0.80	V
Input current	I _{IN}	0 V ≤V _{IN}	₁≤OV _{DD}	—	±10	μA

Table 36. MII Management DC Electrica	I Characteristics When Powered at 3.3 V
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8.3.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 37. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC frequency	f _{MDC}	—	2.5	—	MHz	2
MDC period	t _{MDC}	—	400	—	ns	—
MDC clock pulse width high	t _{MDCH}	32	—	—	ns	_
MDC to MDIO delay	^t мрткнрх ^t мрткнрv	10 —	_	 110	ns	3
MDIO to MDC setup time	t _{MDRDVKH}	10	—	—	ns	—
MDIO to MDC hold time	t _{MDRDXKH}	0	—	—	ns	—
MDC rise time	t _{MDCR}	—	—	10	ns	—
MDC fall time	t _{MDHF}	_	_	10	ns	

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDRDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
 </sub>
- This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
- 3. This parameter is dependent on the ce_clk speed (that is, for a ce_clk of 200 MHz, the delay is 90 ns and for a ce_clk of 300 MHz, the delay is 63 ns).

This figure shows the MII management AC timing diagram.



Figure 21. MII Management Interface Timing Diagram

Local Bus AC Electrical Specifications

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to output valid	t _{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ}		4	ns	8

Table 41. Local Bus General Timing Parameters—DLL Bypass Mode⁹ (continued)

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the to the output (O) going invalid (X) or output hold time.
 </sub>
- 2. All timings are in reference to falling edge of LCLK0 (for all outputs and for LGTA and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
- 3. All signals are measured from OV_{DD}/2 of the rising/falling edge of LCLK0 to 0.4 × OV_{DD} of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. t_{LBOTOT1} should be used when RCWH[LALE] is not set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- t_{LBOTOT2} should be used when RCWH[LALE] is set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- 7. t_{LBOTOT3} should be used when RCWH[LALE] is set and when the load on LALE output pin equals to the load on LAD output pins.
- 8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 9. DLL bypass mode is not recommended for use at frequencies above 66 MHz.

This figure provides the AC test load for the local bus.



Figure 22. Local Bus C Test Load



Local Bus AC Electrical Specifications



Figure 25. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Enabled)





JTAG AC Electrical Characteristics

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.



Figure 29. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.



VM = Midpoint Voltage (OV_{DD}/2)

Figure 30. JTAG Clock Input Timing Diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.



This figure provides the boundary-scan timing diagram.



VM = Midpoint Voltage (OV_{DD}/2)





This figure shows the TDM/SI timing with external clock.



Note: The clock edge is selectable on TDM/SI



17.3 UTOPIA/POS

This section describes the DC and AC electrical specifications for the UTOPIA/POS of the MPC8360E/58E.

17.4 UTOPIA/POS DC Electrical Characteristics

This table provides the DC electrical characteristics for the device UTOPIA.

 Table 59. UTOPIA DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	_	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	$0 V \leq V_{IN} \leq OV_{DD}$	—	±10	μA

17.5 UTOPIA/POS AC Timing Specifications

This table provides the UTOPIA input and output AC timing specifications.

Table 60. UTOPIA AC Timing Specifications¹

Characteristic	Symbol ²	Min	Мах	Unit	Notes
UTOPIA outputs—Internal clock delay	t _{UIKHOV}	0	11.5	ns	
UTOPIA outputs—External clock delay	t _{UEKHOV}	1	11.6	ns	_
UTOPIA outputs—Internal clock high impedance	t _{UIKHOX}	0	8.0	ns	—
UTOPIA outputs—External clock high impedance	t _{UEKHOX}	1	10.0	ns	_
UTOPIA inputs—Internal clock input setup time	t _{UIIVKH}	6	_	ns	_
UTOPIA inputs—External clock input setup time	t _{UEIVKH}	4	—	ns	3



HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

Characteristic	Symbol ²	Min	Мах	Unit
Outputs—Internal clock high impedance	t _{нікнох}	-0.5	5.5	ns
Outputs—External clock high impedance	t _{НЕКНОХ}	1	8	ns
Inputs—Internal clock input setup time	t _{HIIVKH}	8.5	_	ns
Inputs—External clock input setup time	t _{HEIVKH}	4	-	ns
Inputs—Internal clock input hold time	t _{HIIXKH}	1.4	_	ns
Inputs—External clock input hold time	t _{HEIXKH}	1	_	ns

Table 62. HDLC, BISYNC, and Transparent AC Timing Specifications¹ (continued)

Notes:

- 1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
 </sub>

Characteristic	Symbol ²	Min	Мах	Unit
Outputs—Internal clock delay	t _{UAIKHOV}	0	11.3	ns
Outputs—External clock delay	t _{UAEKHOV}	1	14	ns
Outputs—Internal clock high impedance	t _{UAIKHOX}	0	11	ns
Outputs—External clock high impedance	t _{UAEKHOX}	1	14	ns
Inputs—Internal clock input setup time	t _{UAIIVKH}	6	—	ns
Inputs—External clock input setup time	t _{UAEIVKH}	8	—	ns
Inputs—Internal clock input hold time	t _{UAIIXKH}	1	—	ns
Inputs—External clock input hold time	t _{UAEIXKH}	1	—	ns

Notes:

- 1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
 </sub></sub>

This figure provides the AC test load.



Figure 49. AC Test Load



20 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8360E/58E is available in a tape ball grid array (TBGA), see Section 20.1, "Package Parameters for the TBGA Package," and Section 20.2, "Mechanical Dimensions of the TBGA Package," for information on the package.

20.1 Package Parameters for the TBGA Package

The package parameters for rev. 2.0 silicon are as provided in the following list. The package type is $37.5 \text{ mm} \times 37.5 \text{ mm}$, 740 tape ball grid array (TBGA).

Package outline	$37.5 \text{ mm} \times 37.5 \text{ mm}$
Interconnects	740
Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder Balls	62 Sn/36 Pb/2 Ag (ZU package)
	95.5 Sn/0.5 Cu/4Ag (VV package)
Ball diameter (typical)	0.64 mm



Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV _{DD} 0	D5, D6	Power for UCC1 Ethernet interface (2.5 V, 3.3 V)	LV _{DD} 0	
LV _{DD} 1	C17, D16	Power for UCC2 Ethernet interface option 1 (2.5 V, 3.3 V)	LV _{DD} 1	9
LV _{DD} 2	B18, E21	Power for UCC2 Ethernet interface option 2 (2.5 V, 3.3 V)	LV _{DD} 2	9
V _{DD}	C36, D29, D35, E16, F9, F12, F15, F17, F18, F20, F21, F23, F25, F26, F29, F31, F32, F33, G6, J6, K32, M32, N6, P33, R6, R32, U32, V6, Y5, Y32, AB6, AB33, AD6, AF32, AK6, AL6, AM7, AM9, AM10, AM11, AM12, AM13, AM14, AM15, AM18, AM21, AM25, AM28, AM32, AN15, AN21, AN26, AU9, AU17	Power for core (1.2 V)	V _{DD}	_
OV _{DD}	A10, B9, B15, B32, C1, C12, C22, C29, D24, E3, E10, E27, G4, H35, J1, J35, K2, M4, N3, N34, R2, R37, T36, U2, U33, V4, V34, W3, Y35, Y37, AA1, AA36, AB2, AB34	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV _{DD}	_
MVREF1	AN20	I	DDR reference voltage	—
MVREF2	AU32	I	DDR reference voltage	_
SPARE1	B11	I/O	OV _{DD}	8
SPARE3	AH32		GV _{DD}	8
SPARE4	AU18	_	GV _{DD}	7
SPARE5	AP1	_	GV _{DD}	8

Table 66. MPC8360E TBGA Pinout Listing (continued)



Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
IRQ[4:5]	G33, G32	I/O	OV _{DD}	—
IRQ[6]/LCS[6]/CKSTOP_OUT	E35	I/O	OV _{DD}	—
IRQ[7]/LCS[7]/CKSTOP_IN	H36	I/O	OV _{DD}	—
	DUART			
UART1_SOUT/M1SRCID[0]/ M2SRCID[0]/LSRCID[0]	E32	0	OV _{DD}	_
UART1_SIN/M1SRCID[1]/ M2SRCID[1]/LSRCID[1]	B34	I/O	OV _{DD}	
UART1_CTS/M1SRCID[2]/ M2SRCID[2]/LSRCID[2]	C34	I/O	OV _{DD}	
UART1_RTS/M1SRCID[3]/ M2SRCID[3]/LSRCID[3]	A35	0	OV _{DD}	_
	I ² C Interface			<u></u>
IIC1_SDA	D34	I/O	OV _{DD}	2
IIC1_SCL	B35	I/O	OV _{DD}	2
IIC2_SDA	E33	I/O	OV _{DD}	2
IIC2_SCL C35		I/O	OV _{DD}	2
	QUICC Engine			
CE_PA[0]	F8	I/O	LV _{DD0}	—
CE_PA[1:2]	AH1, AG5	I/O	OV _{DD}	—
CE_PA[3:7]	F6, D4, C3, E5, A3	I/O	LV _{DD} 0	—
CE_PA[8]	AG3	I/O	OV _{DD}	—
CE_PA[9:12]	F7, B3, E6, B4	I/O	LV _{DD} 0	—
CE_PA[13:14]	AG1, AF6	I/O	OV _{DD}	—
CE_PA[15]	B2	I/O	LV _{DD} 0	—
CE_PA[16]	AF4		OV _{DD}	—
CE_PA[17:21]	B16, A16, E17, A17, B17	I/O	LV _{DD} 1	—
CE_PA[22]	AF3	I/O	OV _{DD}	—
CE_PA[23:26]	C18, D18, E18, A18	I/O	LV _{DD} 1	—
CE_PA[27:28]	AF2, AE6	I/O	OV _{DD}	—
CE_PA[29]	B19	I/O	LV _{DD} 1	—
CE_PA[30]	AE5	I/O	OV_{DD}	—
CE_PA[31]	F16		LV _{DD} 1	—



The QUICC Engine block VCO frequency is derived from the following equations:

 $ce_clk = (primary clock input \times CEPMF) \div (1 + CEPDF)$

QE VCO Frequency = $ce_clk \times VCO$ divider $\times (1 + CEPDF)$

21.4 Suggested PLL Configurations

To simplify the PLL configurations, the device might be separated into two clock domains. The first domain contains the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine block PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. This table shows suggested PLL configurations for 33 and 66 MHz input clocks and illustrates each of the clock domains separately. Any combination of clock domains setting with same input clock are valid. Refer to Section 21, "Clocking," for the appropriate operating frequencies for your device.

Conf No. ¹	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock Freq (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
				33 MH:	z CLKIN/PCI	SYNC_IN	Options				
s1	0100	0000100	æ	æ	33	133	266	—	8	8	8
s2	0100	0000101	æ	æ	33	133	333	_	8	∞	8
s3	0101	0000100	æ	æ	33	166	333	_	8	8	8
s4	0101	0000101	æ	æ	33	166	416			8	8
s5	0110	0000100	æ	æ	33	200	400		8	8	8
s6	0110	0000110	æ	æ	33	200	600			—	8
s7	0111	0000011	æ	æ	33	233	350		8	8	8
s8	0111	0000100	æ	æ	33	233	466			8	8
s9	0111	0000101	æ	æ	33	233	583			_	8
s10	1000	0000011	æ	æ	33	266	400		8	8	8
s11	1000	0000100	æ	æ	33	266	533			8	8
s12	1000	0000101	æ	æ	33	266	667			_	8
s13	1001	0000010	æ	æ	33	300	300		8	8	8
s14	1001	0000011	æ	æ	33	300	450	_		8	8
s15	1001	0000100	æ	æ	33	300	600	_		—	8
s16	1010	0000010	æ	æ	33	333	333	_	8	8	8
s17	1010	0000011	æ	æ	33	333	500	_		8	8
s18	1010	0000100	æ	æ	33	333	667	_		—	8
c1	æ	æ	01001	0	33			300	8	8	8
c2	æ	æ	01100	0	33	_	_	400	8	8	8
c3	æ	æ	01110	0	33	_	_	466	_	8	8
c4	æ	æ	01111	0	33			500	_	8	8

Table 76. Suggested PLL Configurations



Table 77. Package Thermal Characteristics for the TBGA Package (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-package natural convection on top		1	° C/W	6

Notes

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
- 2. Per JEDEC JESD51-2 and SEMI G38-87 with the single layer board horizontal.
- 3. Per JEDEC JESD51-6 with the board horizontal. 1 m/sec is approximately equal to 200 linear feet per minute (LFM).
- 4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

22.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See Table 6 for typical power dissipations values.

22.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

 T_J = junction temperature (° C)

 T_A = ambient temperature for the package (° C)

 $R_{\theta IA}$ = junction-to-ambient thermal resistance (° C/W)

 P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

22.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. Additionally, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device. At a known board temperature, the junction temperature is estimated using the following equation:

Part Numbers Fully Addressed by this Document

Device	Package	SVR (Rev. 2.0)	SVR (Rev. 2.1)
MPC8358E	TBGA	0x804A_0020	0x804A_0021
MPC8358	TBGA	0x804B_0020	0x804B_0021

25 Document Revision History

This table provides a revision history for this document.

Table 82. Revision History

Rev. Number	Date	Substantive Change(s)
5	09/2011	 Section 2.2.1, "Power-Up Sequencing", added the current limitation "3A to 5A" for the excessive current. Section 2.1.2, "Power Supply Voltage Specification, Updated the Characteristic for TBGA (MPC8358 & MPC8360 Device) with specific frequency for Core and PLL voltages. Added table footnote 3 to Table 2. Applied table footnotes 1 and 2 to Table 10. Removed table footnotes from Table 19. Applied table footnotes 8 and 9 to Table 40. Applied table footnotes 2 and 3 to Table 41. Applied table footnotes from Table 46. Applied table footnote to last three rows of Table 65.
4	01/2011	 Updated references to the LCRR register throughout Removed references to DDR DLL mode in Section 6.2.2, "DDR and DDR2 SDRAM Output AC Timing Specifications." Changed "Junction-to-Case" to "Junction-to-Ambient" in Section 22.2.4, "Heat Sinks and Junction-to-Ambient Thermal Resistance," and Table 78, "Heat Sinks and Junction-to-Ambient Thermal Resistance of TBGA Package," titles.