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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8358vvagdg

4.1 DC Electrical Characteristics

This table provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the device.

Table 7. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	$OV_{DD} + 0.3$	V
Input low voltage	—	V_{IL}	−0.3	0.4	V
CLKIN input current	$0\text{ V} \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0\text{ V} \leq V_{IN} \leq 0.5\text{ V}$ or $OV_{DD} - 0.5\text{ V} \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	$0.5\text{ V} \leq V_{IN} \leq OV_{DD} - 0.5\text{ V}$	I_{IN}	—	±100	μA

4.2 AC Electrical Characteristics

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 8. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f_{CLKIN}	—	—	66.67	MHz	1
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	—	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:

- Caution:** The system, core, USB, security, and 10/100/1000 Ethernet must not exceed their respective maximum or minimum operating frequencies.
- Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 V and 2.7 V.
- Timing is guaranteed by design and characterization.
- This represents the total input jitter—short term and long term—and is guaranteed by design.
- The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at −20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.

4.3 Gigabit Reference Clock Input Timing

This table provides the Gigabit reference clocks (GTX_CLK125) AC timing specifications.

Table 9. GTX_CLK125 AC Timing Specifications

At recommended operating conditions with $LV_{DD} = 2.5 \pm 0.125\text{ mV}$ / $3.3\text{ V} \pm 165\text{ mV}$

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—

Table 9. GTX_CLK125 AC Timing Specifications

At recommended operating conditions with $LV_{DD} = 2.5 \pm 0.125$ mV/ $3.3 \text{ V} \pm 165$ mV (continued)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
GTX_CLK rise and fall time $LV_{DD} = 2.5 \text{ V}$ $LV_{DD} = 3.3 \text{ V}$	t_{G125R}/t_{G125F}	—	—	0.75 1.0	ns	1
GTX_CLK125 duty cycle GMII & TBI 1000Base-T for RGMII & RTBI	t_{G125H}/t_{G125}	45 47	—	55 53	%	2
GTX_CLK125 jitter	—	—	—	± 150	ps	2

Notes:

1. Rise and fall times for GTX_CLK125 are measured from 0.5 and 2.0 V for $LV_{DD} = 2.5 \text{ V}$ and from 0.6 and 2.7 V for $LV_{DD} = 3.3 \text{ V}$.
2. GTX_CLK125 is used to generate the GTX clock for the UCC Ethernet transmitter with 2% degradation. The GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by GTX_CLK. See [Section 8.2.2, “MII AC Timing Specifications,”](#) [Section 8.2.3, “RMII AC Timing Specifications,”](#) and [Section 8.2.5, “RGMII and RTBI AC Timing Specifications”](#) for the duty cycle for 10Base-T and 100Base-T reference clock.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8360E/58E.

5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins of the device.

Table 10. RESET Pins DC Electrical Characteristics ¹

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	−0.3	0.8	V
Input current	I_{IN}	—	—	± 10	μA
Output high voltage	V_{OH} ²	$I_{OH} = -8.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V

Notes:

1. This table applies for pins $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, and $\overline{\text{QUIESCE}}$.
2. $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) \pm 5%.

Parameter ⁸	Symbol ¹	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKHME}	-0.6	0.9	ns	7

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/ \overline{MCK} referenced measurements are made from the crossing of the two signals ± 0.1 V.
- In the source synchronous mode, MCK/ \overline{MCK} can be shifted in $\frac{1}{4}$ applied cycle increments through the clock control register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
- ADDR/CMD includes all DDR SDRAM output signals except $\overline{MCK}/\overline{MCK}$, \overline{MCS} , and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by $\frac{1}{2}$ applied cycle.
- Note that t_{DDKMHM} follows the symbol conventions described in note 1. For example, t_{DDKMHM} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKMHM} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. Refer *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the device.
- All outputs are referenced to the rising edge of MCK(n) at the pins of the device. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
- AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.
- In rev. 2.0 silicon, t_{DDKMHM} maximum meets the specification of 0.6 ns. In rev. 2.0 silicon, due to errata, t_{DDKMHM} minimum is -0.9 ns. Refer to Errata DDR18 in *Chip Errata for the MPC8360E, Rev. 1*.

This figure shows the DDR SDRAM output timing for address skew with respect to any MCK.

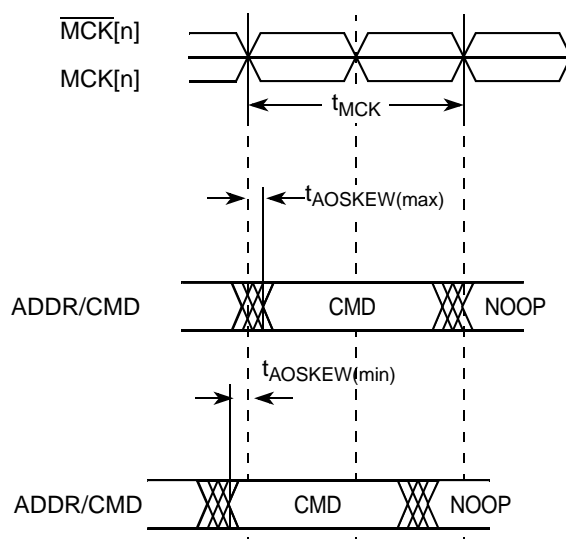


Figure 7. Timing Diagram for t_{AOSKEW} Measurement

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8360E/58E.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface of the device.

Table 23. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V	—
Low-level input voltage OV_{DD}	V_{IL}	-0.3	0.8	V	—
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.4$	—	V	—
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V	—
Input current ($0 V \leq V_{IN} \leq OV_{DD}$)	I_{IN}	—	± 10	μA	1

Note:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface of the device.

Table 24. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	—
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	—	2

Notes:

- Actual attainable baud rate is limited by the latency of interrupt processing.
- The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

8 UCC Ethernet Controller: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

8.1 Three-Speed Ethernet Controller (10/100/1000 Mbps)—GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), MII (media independent interface), RMII (reduced media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The MII, RMII, GMII, and TBI interfaces are only defined for 3.3 V, while the RGMII and RTBI interfaces are only defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet

8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.2.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 29. MII Transmit AC Timing Specifications

At recommended operating conditions with V_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX} t_{MTKHDV}	1 —	5	— 15	ns
TX_CLK data clock rise time, (20% to 80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall time, (80% to 20%)	t_{MTXF}	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the MII transmit AC timing diagram.

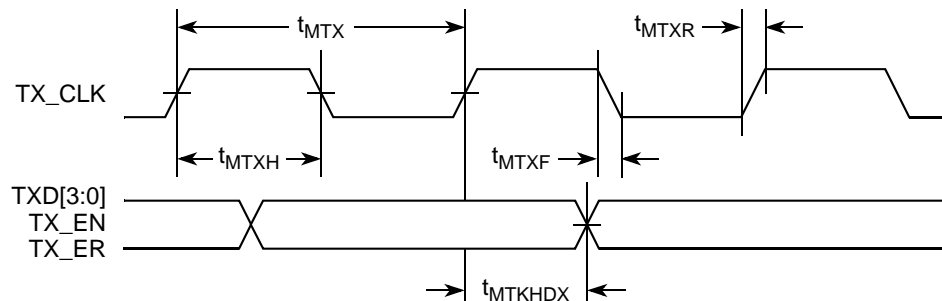


Figure 12. MII Transmit AC Timing Diagram

8.2.3 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.3.1 RMII Transmit AC Timing Specifications

This table provides the RMII transmit AC timing specifications.

Table 31. RMII Transmit AC Timing Specifications

At recommended operating conditions with V_{DD}/OV_{DD} of 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$ $t_{RMTKHDXV}$	2 —	—	— 10	ns
REF_CLK data clock rise time	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall time	t_{RMXF}	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications follow the pattern of $t_{(first\ three\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

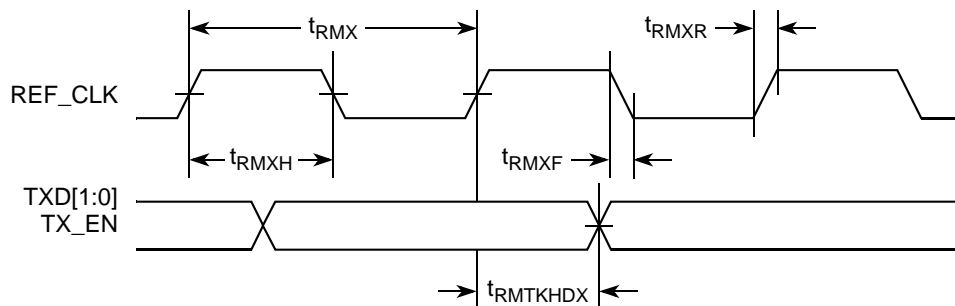


Figure 15. RMII Transmit AC Timing Diagram

8.2.3.2 RMII Receive AC Timing Specifications

This table provides the RMII receive AC timing specifications.

Table 32. RMII Receive AC Timing Specifications

At recommended operating conditions with V_{DD}/OV_{DD} of 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%

8.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

Table 34. TBI Receive AC Timing Specifications

At recommended operating conditions with V_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
PMA_RX_CLK clock period	t_{TRX}	—	16.0	—	ns	—
PMA_RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns	—
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%	—
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns	2
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.0	—	—	ns	2
RX_CLK clock rise time, $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$	t_{TRXR}	0.7	—	2.4	ns	—
RX_CLK clock fall time, $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$	t_{TRXF}	0.7	—	2.4	ns	—

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
- Setup and hold time of even numbered RCG are measured from rising edge of PMA_RX_CLK1. Setup and hold time of odd numbered RCG are measured from rising edge of PMA_RX_CLK0.

This figure shows the TBI receive AC timing diagram.

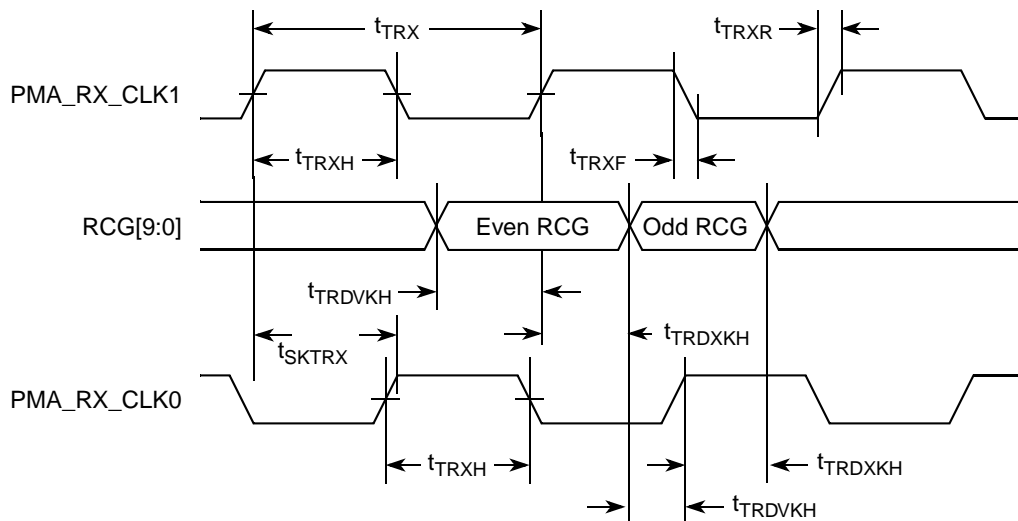


Figure 19. TBI Receive AC Timing Diagram

8.3.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 37. MII Management AC Timing Specifications

At recommended operating conditions with V_{DD} is 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	$t_{MDTKHDX}$ $t_{MDTKHDV}$	10 —	—	— 110	ns	3
MDIO to MDC setup time	$t_{MDRDVKH}$	10	—	—	ns	—
MDIO to MDC hold time	$t_{MDRDXXKH}$	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDRDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
3. This parameter is dependent on the ce_clk speed (that is, for a ce_clk of 200 MHz, the delay is 90 ns and for a ce_clk of 300 MHz, the delay is 63 ns).

This figure shows the MII management AC timing diagram.

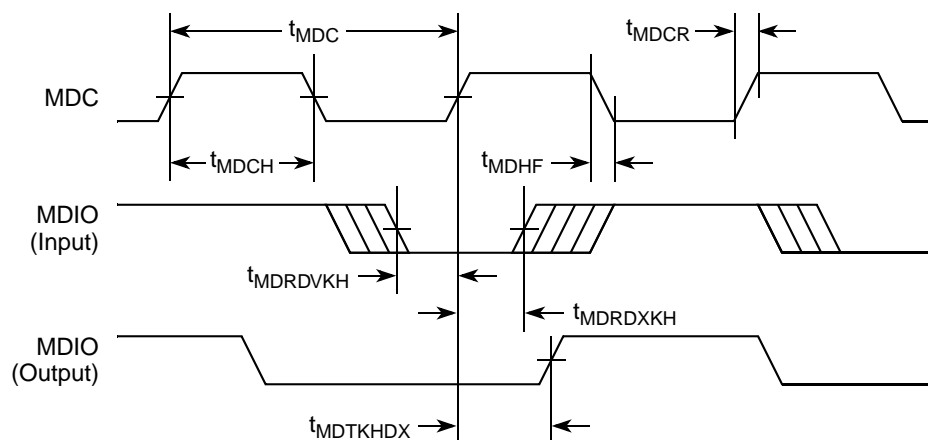


Figure 21. MII Management Interface Timing Diagram

This figure provides the test access port timing diagram.

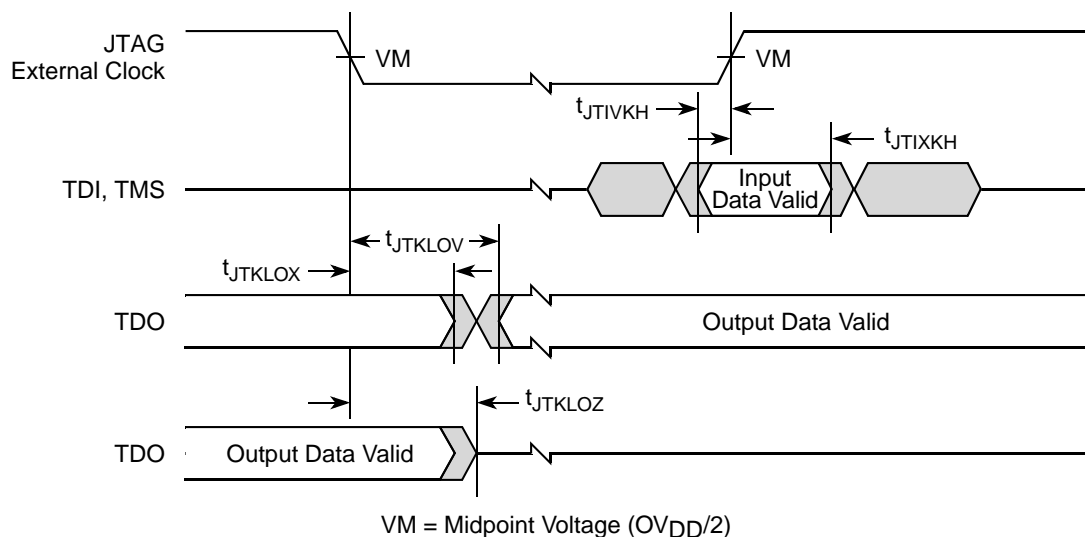


Figure 33. Test Access Port Timing Diagram

11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8360E/58E.

11.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I²C interface of the device.

Table 44. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	-0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	0.4	V	1
Output fall time from $V_{IH}(\text{min})$ to $V_{IL}(\text{max})$ with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current ($0\text{ V} \leq V_{IN} \leq OV_{DD}$)	I_{IN}	—	± 10	μA	4

Notes:

- Output voltage (open drain or open collector) condition = 3 mA sink current.
- C_B = capacitance of one bus line in pF.
- Refer to the *MPC8360E Integrated Communications Processor Reference Manual* for information on the digital filter used.
- I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

20.2 Mechanical Dimensions of the TBGA Package

This figure depicts the mechanical dimensions and bottom surface nomenclature of the device, 740-TBGA package.

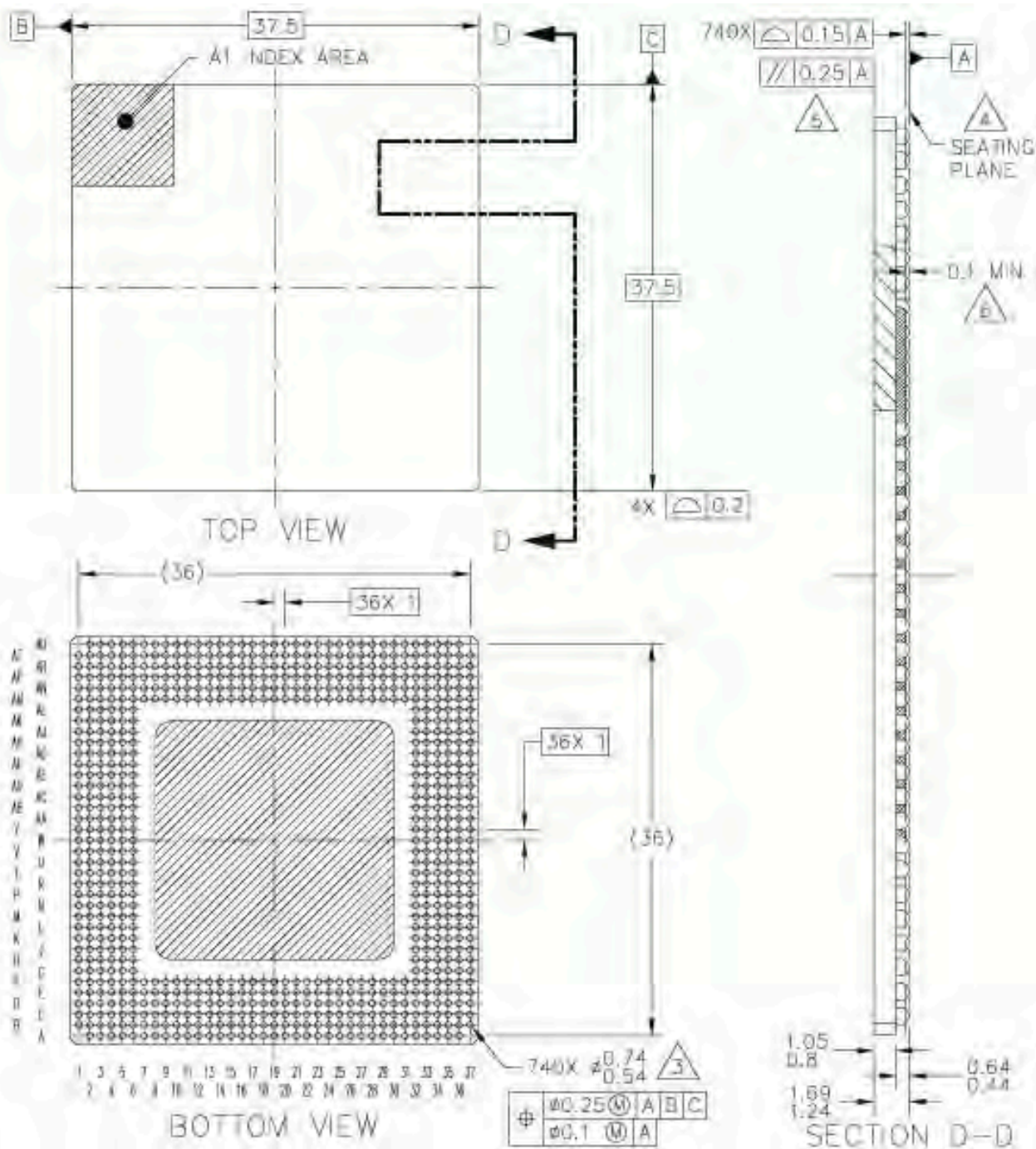


Figure 53. Mechanical Dimensions and Bottom Surface Nomenclature of the TBGA Package

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC1_MCKE[0:1]	AL32, AU33	O	GV _{DD}	3
MEMC1_MCK[0:1]	AK37, AT37	O	GV _{DD}	—
MEMC1_MCK[2:3]/ MEMC2_MCK[0:1]	AN1, AR2	O	GV _{DD}	—
MEMC1_MCK[4:5]/ MEMC2_MCKE[0:1]	AN25, AK1	O	GV _{DD}	—
MEMC1_MCK[0:1]	AL37, AT36	O	GV _{DD}	—
MEMC1_MCK[2:3]/ MEMC2_MCK[0:1]	AP2, AT2	O	GV _{DD}	—
MEMC1_MCK[4]/ MEMC2_MDM[8]	AN24	O	GV _{DD}	—
MEMC1_MCK[5]/ MEMC2_MDQS[8]	AL1	O	GV _{DD}	—
MDIC[0:1]	AH6, AP30	I/O	GV _{DD}	10
Secondary DDR SDRAM Memory Controller Interface				
MEMC2_MECC[0:7]	AN16, AP18, AM16, AM17, AN17, AP13, AP15, AN13	I/O	GV _{DD}	—
MEMC2_MBA[0:2]	AU12, AU15, AU13	O	GV _{DD}	—
MEMC2_MA[0:14]	AT12, AP11, AT13, AT14, AR13, AR15, AR16, AT16, AT18, AT17, AP10, AR20, AR17, AR14, AR11	O	GV _{DD}	—
MEMC2_MWE	AU10	O	GV _{DD}	—
MEMC2_MRAS	AT11	O	GV _{DD}	—
MEMC2_MCAS	AU11	O	GV _{DD}	—
PCI				
PCI_INTA/IRQ_OUT/CE_PF[5]	A20	I/O	LV _{DD2}	2
PCI_RESET_OUT/CE_PF[6]	E19	I/O	LV _{DD2}	—
PCI_AD[31:30]/CE_PG[31:30]	D20, D21	I/O	LV _{DD2}	—
PCI_AD[29:25]/CE_PG[29:25]	A24, B23, C23, E23, A26	I/O	OV _{DD}	—
PCI_AD[24]/CE_PG[24]	B21	I/O	LV _{DD2}	—
PCI_AD[23:0]/CE_PG[23:0]	C24, C25, D25, B25, E24, F24, A27, A28, F27, A30, C30, D30, E29, B31, C31, D31, D32, A32, C33, B33, F30, E31, A34, D33	I/O	OV _{DD}	—
PCI_C/BE[3:0]/CE_PF[10:7]	E22, B26, E28, F28	I/O	OV _{DD}	—
PCI_PAR/CE_PF[11]	D28	I/O	OV _{DD}	—
PCI_FRAME/CE_PF[12]	D26	I/O	OV _{DD}	5
PCI_TRDY/CE_PF[13]	C27	I/O	OV _{DD}	5
PCI_IRDY/CE_PF[14]	C28	I/O	OV _{DD}	5
PCI_STOP/CE_PF[15]	B28	I/O	OV _{DD}	5

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
CE_PA[22]	AF3	I/O	OV _{DD}	—
CE_PA[23:26]	C18, D18, E18, A18	I/O	LV _{DD1}	—
CE_PA[27:28]	AF2, AE6	I/O	OV _{DD}	—
CE_PA[29]	B19	I/O	LV _{DD1}	—
CE_PA[30]	AE5	I/O	OV _{DD}	—
CE_PA[31]	F16	I/O	LV _{DD1}	—
CE_PB[0:27]	AE2, AE1, AD5, AD3, AD2, AC6, AC5, AC4, AC2, AC1, AB5, AB4, AB3, AB1, AA6, AA4, AA2, Y6, Y4, Y3, Y2, Y1, W6, W5, W2, V5, V3, V2	I/O	OV _{DD}	—
CE_PC[0:1]	V1, U6	I/O	OV _{DD}	—
CE_PC[2:3]	C16, A15	I/O	LV _{DD1}	—
CE_PC[4:6]	U4, U3, T6	I/O	OV _{DD}	—
CE_PC[7]	C19	I/O	LV _{DD2}	—
CE_PC[8:9]	A4, C5	I/O	LV _{DD0}	—
CE_PC[10:30]	T5, T4, T2, T1, R5, R3, R1, C11, D12, F13, B10, C10, E12, A9, B8, D10, A14, E15, B14, D15, AH2	I/O	OV _{DD}	—
CE_PD[0:27]	E11, D9, C8, F11, A7, E9, C7, A6, F10, B6, D7, E8, B5, A5, C2, E4, F5, B1, D2, G5, D1, E2, H6, F3, E1, F2, G3, H4	I/O	OV _{DD}	—
CE_PE[0:31]	K3, J2, F1, G2, J5, H3, G1, H2, K6, J3, K5, K4, L6, P6, P4, P3, P1, N4, N5, N2, N1, M2, M3, M5, M6, L1, L2, L4, E14, C13, C14, B13	I/O	OV _{DD}	—
CE_PF[0:3]	F14, D13, A12, A11	I/O	OV _{DD}	—
Clocks				
PCI_CLK_OUT[0]/CE_PF[26]	B22	I/O	LV _{DD2}	—
PCI_CLK_OUT[1:2]/CE_PF[27:28]	D22, A23	I/O	OV _{DD}	—
CLKIN	E37	I	OV _{DD}	—
PCI_CLOCK/PCI_SYNC_IN	M36	I	OV _{DD}	—
PCI_SYNC_OUT/CE_PF[29]	D37	I/O	OV _{DD}	3
JTAG				
TCK	K33	I	OV _{DD}	—
TDI	K34	I	OV _{DD}	4
TDO	H37	O	OV _{DD}	3
TMS	J36	I	OV _{DD}	4
TRST	L32	I	OV _{DD}	4
Test				
TEST	L35	I	OV _{DD}	7
TEST_SEL	AU34	I	GV _{DD}	7

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PMC				
$\overline{\text{QUIESCE}}$	B36	O	OV_{DD}	—
System Control				
$\overline{\text{PORESET}}$	L37	I	OV_{DD}	—
$\overline{\text{HRESET}}$	L36	I/O	OV_{DD}	1
$\overline{\text{SRESET}}$	M33	I/O	OV_{DD}	2
Thermal Management				
THERM0	AP19	I	GV_{DD}	—
THERM1	AT31	I	GV_{DD}	—
Power and Ground Signals				
AV_{DD1}	K35	Power for LBIU DLL (1.2 V)	AV_{DD1}	—
AV_{DD2}	K36	Power for CE PLL (1.2 V)	AV_{DD2}	—
AV_{DD5}	AM29	Power for e300 PLL (1.2 V)	AV_{DD5}	—
AV_{DD6}	K37	Power for system PLL (1.2 V)	AV_{DD6}	—
GND	A2, A8, A13, A19, A22, A25, A31, A33, A36, B7, B12, B24, B27, B30, C4, C6, C9, C15, C26, C32, D3, D8, D11, D14, D17, D19, D23, D27, E7, E13, E25, E30, E36, F4, F37, G34, H1, H5, H32, H33, J4, J32, J37, K1, L3, L5, L33, L34, M1, M34, M35, N37, P2, P5, P35, P36, R4, T3, U1, U5, U35, V37, W1, W4, W33, W36, Y34, AA3, AA5, AC3, AC32, AC35, AD1, AD37, AE4, AE34, AE36, AF33, AG4, AG6, AG32, AH35, AJ1, AJ4, AJ32, AJ35, AJ37, AK36, AL3, AL34, AM4, AN6, AN23, AN30, AP8, AP12, AP14, AP16, AP17, AP20, AP25, AR6, AR8, AR9, AR19, AR24, AR31, AR35, AR37, AT4, AT10, AT19, AT20, AT25, AU14, AU22, AU28, AU35	—	—	—
GV_{DD}	AD4, AE3, AF1, AF5, AF35, AF37, AG2, AG36, AH33, AH34, AK5, AM1, AM35, AM37, AN2, AN10, AN11, AN12, AN14, AN32, AN36, AP5, AP23, AP28, AR1, AR7, AR10, AR12, AR21, AR25, AR27, AR33, AT15, AT22, AT28, AT33, AU2, AU5, AU16, AU31, AU36	Power for DDR DRAM I/O voltage (2.5 or 1.8 V)	GV_{DD}	—

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV _{DD0}	D5, D6	Power for UCC1 Ethernet interface (2.5 V, 3.3 V)	LV _{DD0}	—
LV _{DD1}	C17, D16	Power for UCC2 Ethernet interface option 1 (2.5 V, 3.3 V)	LV _{DD1}	9
LV _{DD2}	B18, E21	Power for UCC2 Ethernet interface option 2 (2.5 V, 3.3 V)	LV _{DD2}	9
V _{DD}	C36, D29, D35, E16, F9, F12, F15, F17, F18, F20, F21, F23, F25, F26, F29, F31, F32, F33, G6, J6, K32, M32, N6, P33, R6, R32, U32, V6, Y5, Y32, AB6, AB33, AD6, AF32, AK6, AL6, AM7, AM9, AM10, AM11, AM12, AM13, AM14, AM15, AM18, AM21, AM25, AM28, AM32, AN15, AN21, AN26, AU9, AU17	Power for core (1.2 V)	V _{DD}	—
OV _{DD}	A10, B9, B15, B32, C1, C12, C22, C29, D24, E3, E10, E27, G4, H35, J1, J35, K2, M4, N3, N34, R2, R37, T36, U2, U33, V4, V34, W3, Y35, Y37, AA1, AA36, AB2, AB34	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV _{DD}	—
MVREF1	AN20	I	DDR reference voltage	—
MVREF2	AU32	I	DDR reference voltage	—
SPARE1	B11	I/O	OV _{DD}	8
SPARE3	AH32	—	GV _{DD}	8
SPARE4	AU18	—	GV _{DD}	7
SPARE5	AP1	—	GV _{DD}	8

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
No Connect				
NC	AM20, AU19	—	—	—

Notes:

1. This pin is an open drain signal. A weak pull-up resistor (1 k Ω) should be placed on this pin to OV_{DD}.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 k Ω) should be placed on this pin to OV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. These are On Die Termination pins, used to control DDR2 memories internal termination resistance.
7. This pin must always be tied to GND.
8. This pin must always be left not connected.
9. Refer to *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* section on “RGMII Pins,” for information about the two UCC2 Ethernet interface options.
10. It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor for DDR2.

This table shows the pin list of the MPC8358E TBGA package.

Table 67. MPC8358E TBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Controller Interface				
MEMC1_MDQ[0:63]	AJ34, AK33, AL33, AL35, AJ33, AK34, AK32, AM36, AN37, AN35, AR34, AT34, AP37, AP36, AR36, AT35, AP34, AR32, AP32, AM31, AN33, AM34, AM33, AM30, AP31, AM27, AR30, AT32, AN29, AP29, AN27, AR29, AN8, AN7, AM8, AM6, AP9, AN9, AT7, AP7, AU6, AP6, AR4, AR3, AT6, AT5, AR5, AT3, AP4, AM5, AP3, AN3, AN5, AL5, AN4, AM2, AL2, AH5, AK3, AJ2, AJ3, AH4, AK4, AH3	I/O	GV _{DD}	—
MEMC_MECC[0:4]/MSRCID[0:4]	AP24, AN22, AM19, AN19, AM24	I/O	GV _{DD}	—
MEMC_MECC[5]/MDVAL	AM23	I/O	GV _{DD}	—
MEMC_MECC[6:7]	AM22, AN18	I/O	GV _{DD}	—
MEMC_MDM[0:8]	AL36, AN34, AP33, AN28, AT9, AU4, AM3, AJ6, AP27	O	GV _{DD}	—
MEMC_MDQS[0:8]	AK35, AP35, AN31, AM26, AT8, AU3, AL4, AJ5, AP26	I/O	GV _{DD}	—
MEMC_MBA[0:1]	AU29, AU30	O	GV _{DD}	—
MEMC_MBA[2]	AT30	O	GV _{DD}	—
MEMC_MA[0:14]	AU21, AP22, AP21, AT21, AU25, AU26, AT23, AR26, AU24, AR23, AR28, AU23, AR22, AU20, AR18	O	GV _{DD}	—
MEMC_MODT[0:3]	AG33, AJ36, AT1, AK2	O	GV _{DD}	6

ordered, see [Section 24.1, “Part Numbers Fully Addressed by this Document,”](#) for part ordering details and contact your Freescale sales representative or authorized distributor for more information.

Table 69. Operating Frequencies for the TBGA Package

Characteristic ¹	400 MHz	533 MHz	667 MHz ²	Unit
e300 core frequency (<i>core_clk</i>)	266–400	266–533	266–667	MHz
Coherent system bus frequency (<i>csb_clk</i>)	133–333			MHz
QUICC Engine frequency ³ (<i>ce_clk</i>)	266–500			MHz
DDR and DDR2 memory bus frequency (MCLK) ⁴	100–166.67			MHz
Local bus frequency (LCLK _n) ⁵	16.67–133			MHz
PCI input frequency (CLKIN or PCI_CLK)	25–66.67			MHz
Security core maximum internal operating frequency	133	133	166	MHz

Notes:

1. The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
2. The 667 MHz core frequency is based on a 1.3 V V_{DD} supply voltage.
3. The 500 MHz QE frequency is based on a 1.3 V V_{DD} supply voltage.
4. The DDR data rate is 2x the DDR memory bus frequency.
5. The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

21.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] and RCWL[SVCOD] parameters. This table shows the multiplication factor encodings for the system PLL.

Table 70. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	× 16
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11

Table 72. CSB Frequency Options (continued)

CFG_CLKIN_DIV at Reset ¹	SPMF	csb_clk: Input Clock Ratio ²	Input Clock Frequency (MHz) ²			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0110	6:1	100	150	200	
Low	0111	7:1	116	175	233	
Low	1000	8:1	133	200	266	
Low	1001	9:1	150	225	300	
Low	1010	10:1	166	250	333	
Low	1011	11:1	183	275		
Low	1100	12:1	200	300		
Low	1101	13:1	216	325		
Low	1110	14:1	233			
Low	1111	15:1	250			
Low	0000	16:1	266			
High	0010	2:1				133
High	0011	3:1				100
High	0100	4:1				133
High	0101	5:1				166
High	0110	6:1				200
High	0111	7:1				233
High	1000	8:1				
High	1001	9:1				
High	1010	10:1				
High	1011	11:1				
High	1100	12:1				
High	1101	13:1				
High	1110	14:1				
High	1111	15:1				
High	0000	16:1				

¹ CFG_CLKIN_DIV is only used for host mode; CLKIN must be tied low and CFG_CLKIN_DIV must be pulled down (low) in agent mode.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

Example 1. Sample Table Use

Index	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
A	1000	0000011	01001	0	33	266	400	300	∞	∞	∞
B	0100	0000100	00110	0	66	266	533	400	∞	∞	∞

- **Example A.** To configure the device with CSB clock rate of 266 MHz, core rate of 400 MHz, and QUICC Engine clock rate 300 MHz while the input clock rate is 33 MHz. Conf No. 's10' and 'c1' are selected from [Table 76](#). SPMF is 1000, CORPLL is 0000011, CEPMPF is 01001, and CEPDF is 0.
- **Example B.** To configure the device with CSBCSB clock rate of 266 MHz, core rate of 533 MHz and QUICC Engine clock rate 400 MHz while the input clock rate is 66 MHz. Conf No. 's5h' and 'c2h' are selected from [Table 76](#). SPMF is 0100, CORPLL is 0000100, CEPMPF is 00110, and CEPDF is 0.

22 Thermal

This section describes the thermal specifications of the MPC8360E/58E.

22.1 Thermal Characteristics

This table provides the package thermal characteristics for the 37.5 mm × 37.5 mm 740-TBGA package.

Table 77. Package Thermal Characteristics for the TBGA Package

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection on single-layer board (1s)	$R_{\theta JA}$	15	°C/W	1, 2
Junction-to-ambient natural convection on four-layer board (2s2p)	$R_{\theta JA}$	11	°C/W	1, 3
Junction-to-ambient (@ 1 m/s) on single-layer board (1s)	$R_{\theta JMA}$	10	°C/W	1, 3
Junction-to-ambient (@ 1 m/s) on four-layer board (2s2p)	$R_{\theta JMA}$	8	°C/W	1, 3
Junction-to-ambient (@ 2 m/s) on single-layer board (1s)	$R_{\theta JMA}$	9	°C/W	1, 3
Junction-to-ambient (@ 2 m/s) on four-layer board (2s2p)	$R_{\theta JMA}$	7	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	4.5	°C/W	4
Junction-to-case thermal	$R_{\theta JC}$	1.1	°C/W	5

Table 82. Revision History (continued)

Rev. Number	Date	Substantive Change(s)
3	03/2010	<ul style="list-style-type: none"> • Changed references to RCWH[PCICKEN] to RCWH[PCICKDRV]. • In Table 2, added extended temperature characteristics. • Added Figure 6, “DDR Input Timing Diagram.” • In Figure 53, “Mechanical Dimensions and Bottom Surface Nomenclature of the TBGA Package,” removed watermark. • Updated the title of Table 19, “DDR SDRAM Input AC Timing Specifications.” • In Table 20, “DDR and DDR2 SDRAM Input AC Timing Specifications Mode,” changed table subtitle. • In Table 27–Table 30, and Table 33–Table 34, changed the rise and fall time specifications to reference 20–80% and 80–20% of the voltage supply, respectively. • In Table 38, “IEEE 1588 Timer AC Specifications,” changed first parameter to “Timer clock frequency.” • In Table 45, “I2C AC Electrical Specifications,” changed units to “ns” for t_{12DVKH}. • In Table 66, “MPC8360E TBGA Pinout Listing,” and Table 67 “MPC8358E TBGA Pinout Listing,” added note 7: “This pin must always be tied to GND” to the TEST pin and added a note to SPARE1 stating: “This pin must always be left not connected.” • In Section 4, “Clock Input Timing,” added note regarding rise/fall time on QUICC Engine block input pins. • Added Section 4.3, “Gigabit Reference Clock Input Timing.” • Updated Section 8.1.1, “10/100/1000 Ethernet DC Electrical Characteristics.” • In Section 20.3, “Pinout Listings,” added sentence stating “Refer to AN3097, ‘MPC8360/MPC8358E PowerQUICC Design Checklist,’ for proper pin termination and usage.” • In Section 21, “Clocking,” removed statement: “The OCCR[PCICDn] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUTn signals.” • In Section 21.1, “System PLL Configuration,” updated the system VCO frequency conditions. • In Table 80, added extended temperature characteristics.
2	12/2007	Initial release.

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