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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8358zuagdg

- Programmable highest priority request
- Four groups of interrupts with programmable priority
- External and internal interrupts directed to communication processor
- Redirects interrupts to external $\overline{\text{INTA}}$ pin when in core disable mode
- Unique vector number for each interrupt source
- Dual industry-standard I²C interfaces
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
 - System initialization data is optionally loaded from I²C-1 EPROM by boot sequencer embedded hardware
- DMA controller
 - Four independent virtual channels
 - Concurrent execution across multiple channels with programmable bandwidth control
 - All channels accessible by local core and remote PCI masters
 - Misaligned transfer capability
 - Data chaining and direct mode
 - Interrupt on completed segment and chain
 - DMA external handshake signals: $\overline{\text{DMA_DREQ}}[0:3]/\overline{\text{DMA_DACK}}[0:3]/\overline{\text{DMA_DONE}}[0:3]$. There is one set for each DMA channel. The pins are multiplexed to the parallel IO pins with other QE functions.
- DUART
 - Two 4-wire interfaces (Rx/D, Tx/D, RTS, CTS)
 - Programming model compatible with the original 16450 UART and the PC16550D
- System timers
 - Periodic interrupt timer
 - Real-time clock
 - Software watchdog timer
 - Eight general-purpose timers
- IEEE Std. 1149.1TM-compliant, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8360E/58E. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value	Unit	Notes
PCI, local bus, DUART, system control and power management, I ² C, SPI, and JTAG I/O voltage	OV _{DD}	3.3 V ± 330 mV	V	—
Junction temperature	T _J	0 to 105 –40 to 105	°C	2

Notes:

1. GV_{DD}, LV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. The operating conditions for junction temperature, T_J, on the 600/333/400 MHz and 500/333/500 MHz on rev. 2.0 silicon is 0° to 70 °C. Refer to Errata General9 in *Chip Errata for the MPC8360E, Rev. 1*.
3. For more information on Part Numbering, refer to [Table 80](#).

This figure shows the undershoot and overshoot voltages at the interfaces of the device.

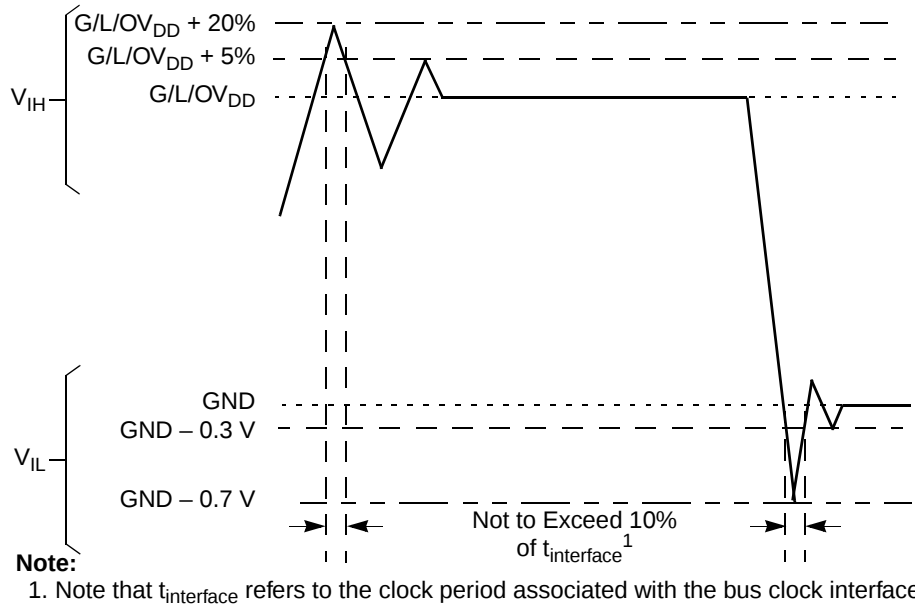


Figure 3. Overshoot/Undershoot Voltage for GV_{DD}/OV_{DD}/LV_{DD}

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 21 and Table 22 provide the output AC timing specifications and measurement conditions for the DDR and DDR2 SDRAM interface.

Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) $\pm$ 5%.

Parameter ⁸	Symbol ¹	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/ $\overline{MCK[n]}$ crossing)	t_{MCK}	6	10	ns	2
Skew between any MCK to ADDR/CMD 333 MHz 266 MHz 200 MHz	t_{AOSKEW}	-1.0 -1.1 -1.2	0.2 0.3 0.4	ns	3
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHAS}	2.1 2.8 3.5	—	ns	4
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz—DDR1 266 MHz—DDR2 200 MHz	t_{DDKHAX}	2.0 2.7 2.8 3.5	—	ns	4
$\overline{MCS}(n)$ output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHCS}	2.1 2.8 3.5	—	ns	4
$\overline{MCS}(n)$ output hold with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHCS}	2.0 2.7 3.5	—	ns	4
MCK to MDQS	t_{DDKMH}	-0.8	0.7	ns	5, 9
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDS} , t_{DDKLDS}	0.7 1.0 1.2	—	ns	6
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDX} , t_{DDKLDX}	0.7 1.0 1.2	—	ns	6
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	7

Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) $\pm$ 5%.

Parameter ⁸	Symbol ¹	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKHME}	-0.6	0.9	ns	7

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/MCK referenced measurements are made from the crossing of the two signals ± 0.1 V.
- In the source synchronous mode, MCK/MCK can be shifted in $\frac{1}{4}$ applied cycle increments through the clock control register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
- ADDR/CMD includes all DDR SDRAM output signals except $\overline{MCK}/\overline{MCK}$, $\overline{MCS}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by $\frac{1}{2}$ applied cycle.
- Note that t_{DDKMHM} follows the symbol conventions described in note 1. For example, t_{DDKMHM} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKMHM} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. Refer *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the device.
- All outputs are referenced to the rising edge of MCK(n) at the pins of the device. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
- AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.
- In rev. 2.0 silicon, t_{DDKMHM} maximum meets the specification of 0.6 ns. In rev. 2.0 silicon, due to errata, t_{DDKMHM} minimum is -0.9 ns. Refer to Errata DDR18 in *Chip Errata for the MPC8360E, Rev. 1*.

This figure shows the DDR SDRAM output timing for address skew with respect to any MCK.

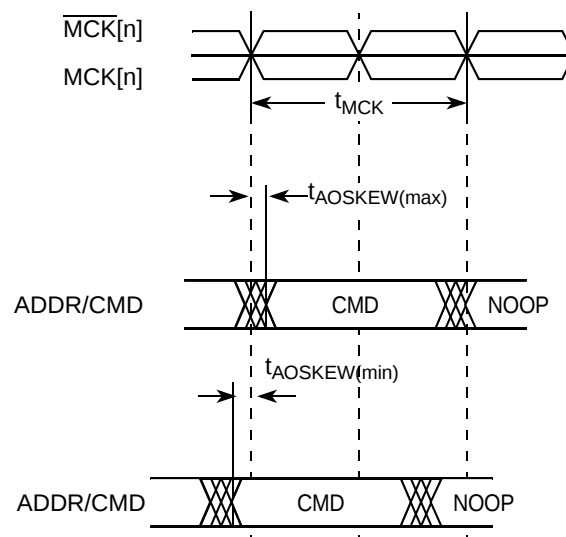


Figure 7. Timing Diagram for t_{AOSKEW} Measurement

This figure provides the AC test load for the DDR bus.

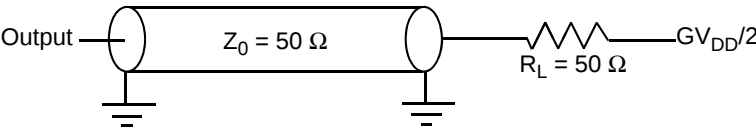


Figure 8. DDR AC Test Load

Table 22. DDR and DDR2 SDRAM Measurement Conditions

Symbol	DDR	DDR2	Unit	Notes
V_{TH}	$MV_{REF} \pm 0.31\text{ V}$	$MV_{REF} \pm 0.25\text{ V}$	V	1
V_{OUT}	$0.5 \times GV_{DD}$	$0.5 \times GV_{DD}$	V	2

Notes:

1. Data input threshold measurement point.
2. Data output measurement point.

This figure shows the DDR SDRAM output timing diagram for source synchronous mode.

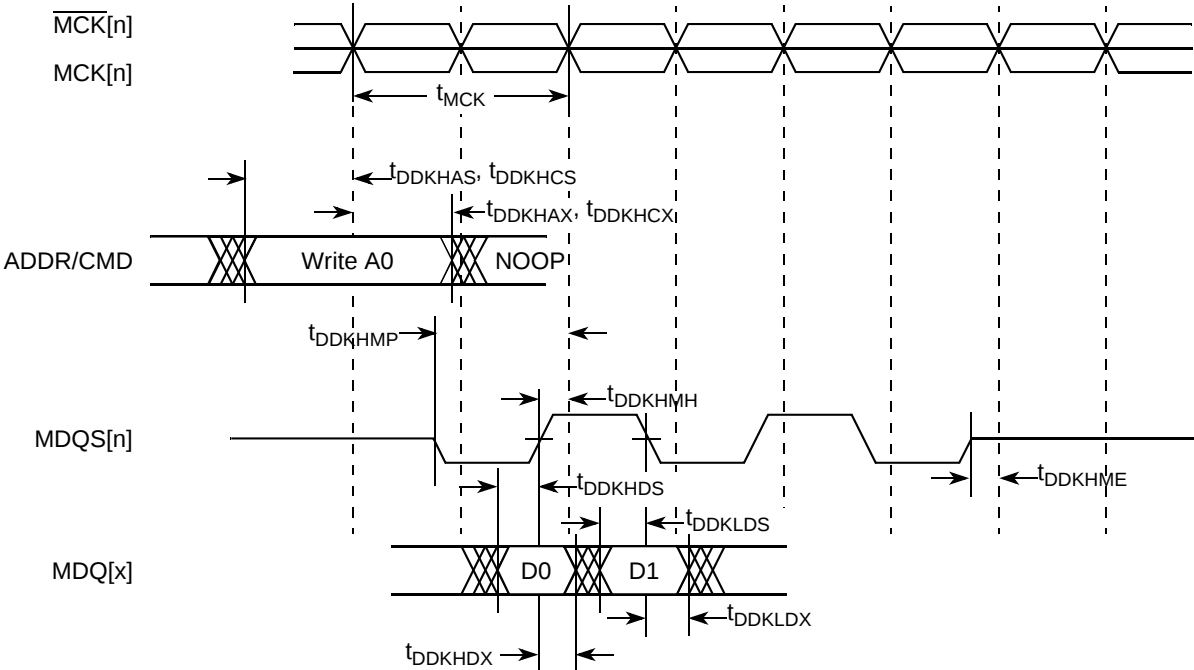


Figure 9. DDR SDRAM Output Timing Diagram for Source Synchronous Mode

8.2.1.1 GMII Transmit AC Timing Specifications

This table provides the GMII transmit AC timing specifications.

Table 27. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns	—
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	40	—	60	%	—
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX} t_{GTKHDV}	0.5 —	—	— 5.0	ns	3
GTX_CLK clock rise time, (20% to 80%)	t_{GTXR}	—	—	1.0	ns	—
GTX_CLK clock fall time, (80% to 20%)	t_{GTXF}	—	—	1.0	ns	—
GTX_CLK125 clock period	t_{G125}	—	8.0	—	ns	2
GTX_CLK125 reference clock duty cycle measured at $LV_{DD}/2$	t_{G125H}/t_{G125}	45	—	55	%	2

Notes:

1. The symbols used for timing specifications follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This symbol is used to represent the external GTX_CLK125 signal and does not follow the original symbol naming convention.
3. In rev. 2.0 silicon, due to errata, t_{GTKHDX} minimum and t_{GTKHDV} maximum are not supported when the GTX_CLK is selected. Refer to Errata *QE_ENET18* in *Chip Errata for the MPC8360E, Rev. 1*.

This figure shows the GMII transmit AC timing diagram.

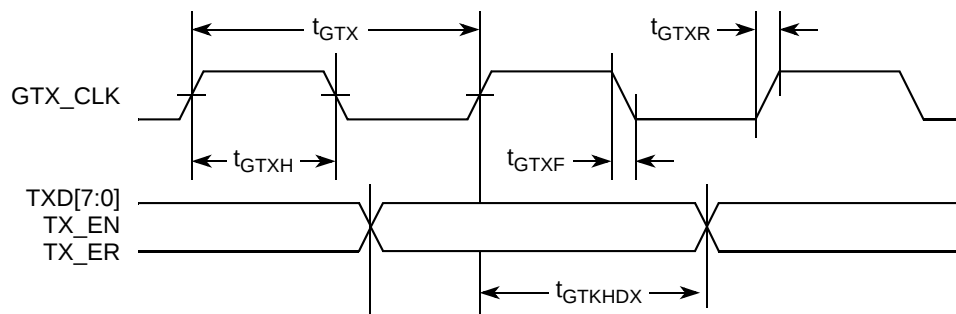


Figure 10. GMII Transmit AC Timing Diagram

8.2.3 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.3.1 RMII Transmit AC Timing Specifications

This table provides the RMII transmit AC timing specifications.

Table 31. RMII Transmit AC Timing Specifications

At recommended operating conditions with V_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$ $t_{RMTKHDX}$	2 —	—	— 10	ns
REF_CLK data clock rise time	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall time	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first three letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

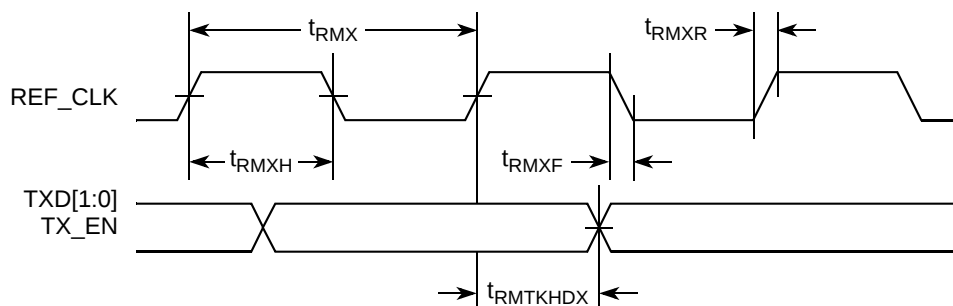


Figure 15. RMII Transmit AC Timing Diagram

8.2.3.2 RMII Receive AC Timing Specifications

This table provides the RMII receive AC timing specifications.

Table 32. RMII Receive AC Timing Specifications

At recommended operating conditions with V_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%

8.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

Table 34. TBI Receive AC Timing Specifications

At recommended operating conditions with V_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
PMA_RX_CLK clock period	t_{TRX}	—	16.0	—	ns	—
PMA_RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns	—
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%	—
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns	2
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.0	—	—	ns	2
RX_CLK clock rise time, $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$	t_{TRXR}	0.7	—	2.4	ns	—
RX_CLK clock fall time, $V_{IH}(\text{max})$ to $V_{IL}(\text{min})$	t_{TRXF}	0.7	—	2.4	ns	—

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
- Setup and hold time of even numbered RCG are measured from rising edge of PMA_RX_CLK1. Setup and hold time of odd numbered RCG are measured from rising edge of PMA_RX_CLK0.

This figure shows the TBI receive AC timing diagram.

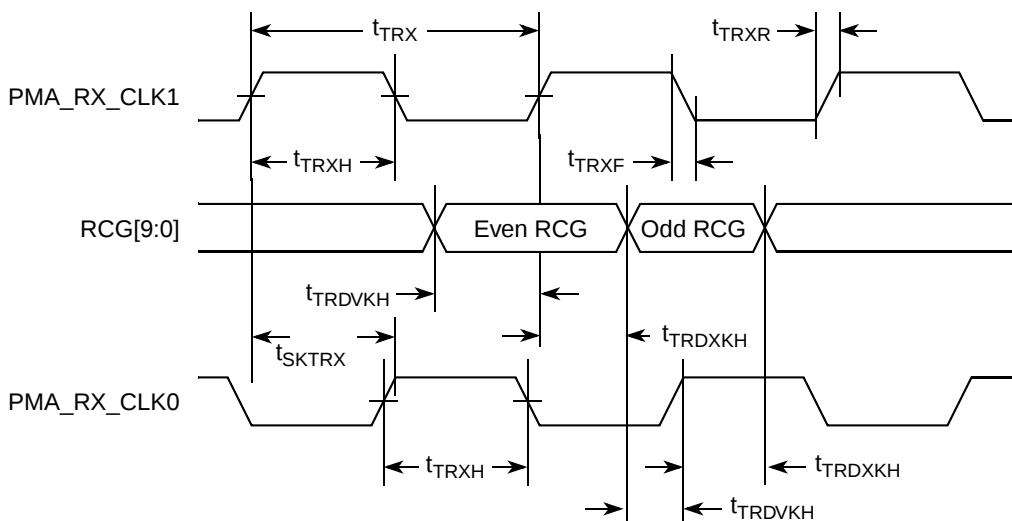


Figure 19. TBI Receive AC Timing Diagram

11.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interface of the device.

Table 45. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 44).

Parameter	Symbol ¹	Min	Max	Unit	Note
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	3
Data hold time: CBUS compatible masters I ² C bus devices	t_{I2DXKL}	— 0 ²	— 0.9 ³	μs	—
Rise time of both SDA and SCL signals	t_{I2CR}	$20 + 0.1 C_B^4$	300	ns	—
Fall time of both SDA and SCL signals	t_{I2CF}	$20 + 0.1 C_B^4$	300	ns	—
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- C_B = capacitance of one bus line in pF.

This figure provides the AC test load for the I²C.

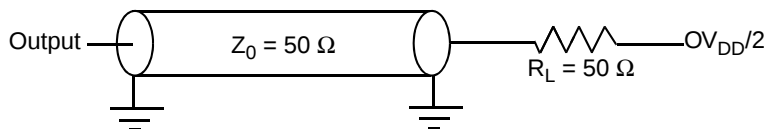


Figure 34. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

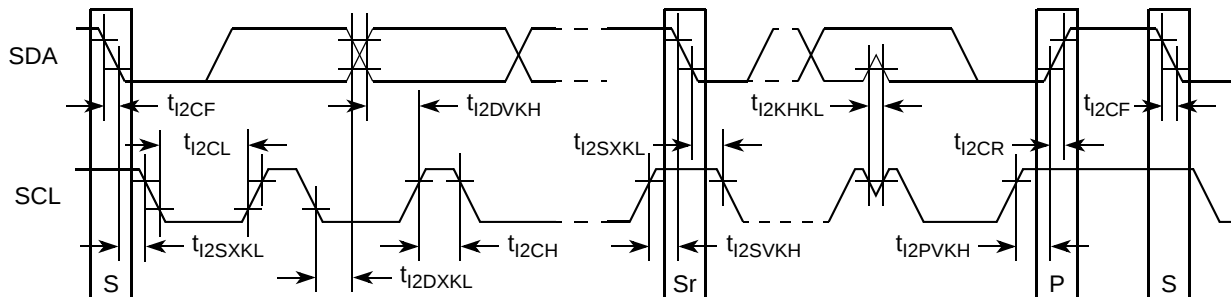


Figure 35. I²C Bus AC Timing Diagram

12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8360E/58E.

12.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface of the device.

Table 46. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH} \text{ (min) or}$	$0.5 \times OV_{DD}$	$OV_{DD} + 0.5$	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL} \text{ (max)}$	-0.5	$0.3 \times OV_{DD}$	V
High-level output voltage	V_{OH}	$I_{OH} = -500 \mu A$	$0.9 \times OV_{DD}$	—	V
Low-level output voltage	V_{OL}	$I_{OL} = 1500 \mu A$	—	$0.1 \times OV_{DD}$	V
Input current	I_{IN}	$0 V \leq V_{IN}^1 \leq OV_{DD}$	—	± 10	μA

12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the device. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. This table provides the PCI AC timing specifications at 66 MHz.

Table 47. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2, 5
Output hold from clock	t_{PCKHOX}	1	—	ns	2

This figure shows the UTOPIA timing with internal clock.

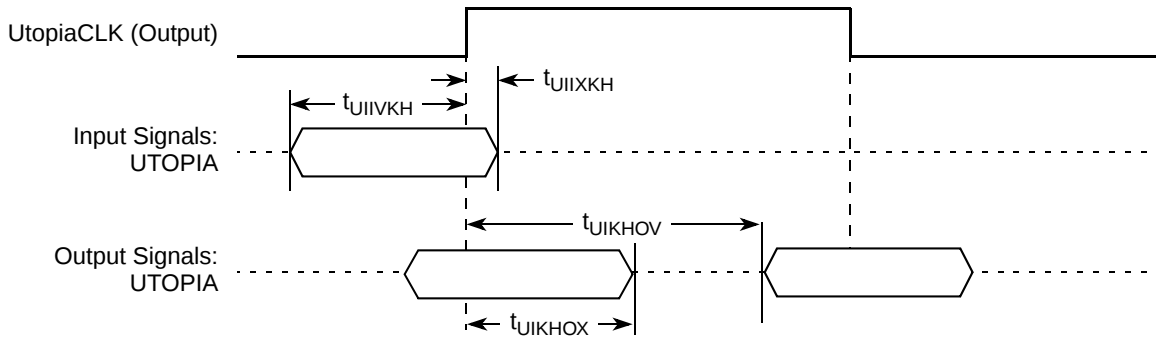


Figure 48. UTOPIA AC Timing (Internal Clock) Diagram

18 HDLC, BISYNC, Transparent, and Synchronous UART

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent, and synchronous UART protocols of the MPC8360E/58E.

18.1 HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

This table provides the DC electrical characteristics for the device HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 61. HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	$I_{OH} = -2.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.5	V
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 10	μA

18.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

These tables provide the input and output AC timing specifications for HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 62. HDLC, BISYNC, and Transparent AC Timing Specifications¹

Characteristic	Symbol ²	Min	Max	Unit
Outputs—Internal clock delay	t_{HIKHOV}	0	11.2	ns
Outputs—External clock delay	t_{HEKHOV}	1	10.8	ns

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PMC				
$\overline{\text{QUIESCE}}$	B36	O	OV_{DD}	—
System Control				
$\overline{\text{PORESET}}$	L37	I	OV_{DD}	—
$\overline{\text{HRESET}}$	L36	I/O	OV_{DD}	1
$\overline{\text{SRESET}}$	M33	I/O	OV_{DD}	2
Thermal Management				
THERM0	AP19	I	GV_{DD}	—
THERM1	AT31	I	GV_{DD}	—
Power and Ground Signals				
$\text{AV}_{\text{DD}1}$	K35	Power for LBIU DLL (1.2 V)	$\text{AV}_{\text{DD}1}$	—
$\text{AV}_{\text{DD}2}$	K36	Power for CE PLL (1.2 V)	$\text{AV}_{\text{DD}2}$	—
$\text{AV}_{\text{DD}5}$	AM29	Power for e300 PLL (1.2 V)	$\text{AV}_{\text{DD}5}$	—
$\text{AV}_{\text{DD}6}$	K37	Power for system PLL (1.2 V)	$\text{AV}_{\text{DD}6}$	—
GND	A2, A8, A13, A19, A22, A25, A31, A33, A36, B7, B12, B24, B27, B30, C4, C6, C9, C15, C26, C32, D3, D8, D11, D14, D17, D19, D23, D27, E7, E13, E25, E30, E36, F4, F37, G34, H1, H5, H32, H33, J4, J32, J37, K1, L3, L5, L33, L34, M1, M34, M35, N37, P2, P5, P35, P36, R4, T3, U1, U5, U35, V37, W1, W4, W33, W36, Y34, AA3, AA5, AC3, AC32, AC35, AD1, AD37, AE4, AE34, AE36, AF33, AG4, AG6, AG32, AH35, AJ1, AJ4, AJ32, AJ35, AJ37, AK36, AL3, AL34, AM4, AN6, AN23, AN30, AP8, AP12, AP14, AP16, AP17, AP20, AP25, AR6, AR8, AR9, AR19, AR24, AR31, AR35, AR37, AT4, AT10, AT19, AT20, AT25, AU14, AU22, AU28, AU35	—	—	—
GV_{DD}	AD4, AE3, AF1, AF5, AF35, AF37, AG2, AG36, AH33, AH34, AK5, AM1, AM35, AM37, AN2, AN10, AN11, AN12, AN14, AN32, AN36, AP5, AP23, AP28, AR1, AR7, AR10, AR12, AR21, AR25, AR27, AR33, AT15, AT22, AT28, AT33, AU2, AU5, AU16, AU31, AU36	Power for DDR DRAM I/O voltage (2.5 or 1.8 V)	GV_{DD}	—

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MWE	AT26	O	GV _{DD}	—
MEMC_MRAS	AT29	O	GV _{DD}	—
MEMC_MCAS	AT24	O	GV _{DD}	—
MEMC_MCS[0:3]	AU27, AT27, AU8, AU7	O	GV _{DD}	—
MEMC_MCKE[0:1]	AL32, AU33	O	GV _{DD}	3
MEMC_MCK[0:5]	AK37, AT37, AN1, AR2, AN25, AK1	O	GV _{DD}	—
MEMC_MCK[0:5]	AL37, AT36, AP2, AT2, AN24, AL1	O	GV _{DD}	—
MDIC[0:1]	AH6, AP30	I/O	GV _{DD}	11
PCI				
PCI_INTA/IRQ_OUT/CE_PF[5]	A20	I/O	LV _{DD2}	2
PCI_RESET_OUT/CE_PF[6]	E19	I/O	LV _{DD2}	—
PCI_AD[31:30]/CE_PG[31:30]	D20, D21	I/O	LV _{DD2}	—
PCI_AD[29:25]/CE_PG[29:25]	A24, B23, C23, E23, A26	I/O	OV _{DD}	—
PCI_AD[24]/CE_PG[24]	B21	I/O	LV _{DD2}	—
PCI_AD[23:0]/CE_PG[23:0]	C24, C25, D25, B25, E24, F24, A27, A28, F27, A30, C30, D30, E29, B31, C31, D31, D32, A32, C33, B33, F30, E31, A34, D33	I/O	OV _{DD}	—
PCI_C/BE[3:0]/CE_PF[10:7]	E22, B26, E28, F28	I/O	OV _{DD}	—
PCI_PAR/CE_PF[11]	D28	I/O	OV _{DD}	—
PCI_FRAME/CE_PF[12]	D26	I/O	OV _{DD}	5
PCI_TRDY/CE_PF[13]	C27	I/O	OV _{DD}	5
PCI_IRDY/CE_PF[14]	C28	I/O	OV _{DD}	5
PCI_STOP/CE_PF[15]	B28	I/O	OV _{DD}	5
PCI_DEVSEL/CE_PF[16]	E26	I/O	OV _{DD}	5
PCI_IDSEL/CE_PF[17]	F22	I/O	OV _{DD}	—
PCI_SERR/CE_PF[18]	B29	I/O	OV _{DD}	5
PCI_PERR/CE_PF[19]	A29	I/O	OV _{DD}	5
PCI_REQ[0]/CE_PF[20]	F19	I/O	LV _{DD2}	—
PCI_REQ[1]/CPCI_HS_ES/ CE_PF[21]	A21	I/O	LV _{DD2}	—
PCI_REQ[2]/CE_PF[22]	C21	I/O	LV _{DD2}	—
PCI_GNT[0]/CE_PF[23]	E20	I/O	LV _{DD2}	—
PCI_GNT[1]/CPCI1_HS_LED/ CE_PF[24]	B20	I/O	LV _{DD2}	—
PCI_GNT[2]/CPCI1_HS_ENUM/ CE_PF[25]	C20	I/O	LV _{DD2}	—

Table 72. CSB Frequency Options (continued)

CFG_CLKIN_DIV at Reset ¹	SPMF	csb_clk: Input Clock Ratio ²	Input Clock Frequency (MHz) ²			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0110	6:1	100	150	200	
Low	0111	7:1	116	175	233	
Low	1000	8:1	133	200	266	
Low	1001	9:1	150	225	300	
Low	1010	10:1	166	250	333	
Low	1011	11:1	183	275		
Low	1100	12:1	200	300		
Low	1101	13:1	216	325		
Low	1110	14:1	233			
Low	1111	15:1	250			
Low	0000	16:1	266			
High	0010	2:1				133
High	0011	3:1				100
High	0100	4:1				133
High	0101	5:1				166
High	0110	6:1				200
High	0111	7:1				233
High	1000	8:1				
High	1001	9:1				
High	1010	10:1				
High	1011	11:1				
High	1100	12:1				
High	1101	13:1				
High	1110	14:1				
High	1111	15:1				
High	0000	16:1				

¹ CFG_CLKIN_DIV is only used for host mode; CLKIN must be tied low and CFG_CLKIN_DIV must be pulled down (low) in agent mode.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

Table 77. Package Thermal Characteristics for the TBGA Package (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-package natural convection on top	Ψ_{JT}	1	°C/W	6

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and SEMI G38-87 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal. 1 m/sec is approximately equal to 200 linear feet per minute (LFM).
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

22.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See Table 6 for typical power dissipations values.

22.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J , can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

22.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. Additionally, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device. At a known board temperature, the junction temperature is estimated using the following equation:

This table shows heat sinks and junction-to-ambient thermal resistance for TBGA package.

Table 78. Heat Sinks and Junction-to-Ambient Thermal Resistance of TBGA Package

Heat Sink Assuming Thermal Grease	Airflow	35 × 35 mm TBGA
		Junction-to-Ambient Thermal Resistance
AAVID 30 × 30 × 9.4 mm pin fin	Natural convection	10.7
AAVID 30 × 30 × 9.4 mm pin fin	1 m/s	6.2
AAVID 30 × 30 × 9.4 mm pin fin	2 m/s	5.3
AAVID 31 × 35 × 23 mm pin fin	Natural convection	8.1
AAVID 31 × 35 × 23 mm pin fin	1 m/s	4.4
AAVID 31 × 35 × 23 mm pin fin	2 m/s	3.7
Wakefield, 53 × 53 × 25 mm pin fin	Natural convection	5.4
Wakefield, 53 × 53 × 25 mm pin fin	1 m/s	3.2
Wakefield, 53 × 53 × 25 mm pin fin	2 m/s	2.4
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural convection	6.4
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	3.8
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	2.5
MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass	1 m/s	2.8

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following:

Aavid Thermalloy 603-224-9988
 80 Commercial St.
 Concord, NH 03301
 Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
 473 Sapena Ct. #15
 Santa Clara, CA 95054
 Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
 413 North Moss St.
 Burbank, CA 91502
 Internet: www.ctscorp.com

Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-millennium.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Interface material vendors include the following:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

22.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb force (4.5 kg force). If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

This figure shows the PLL power supply filter circuit.

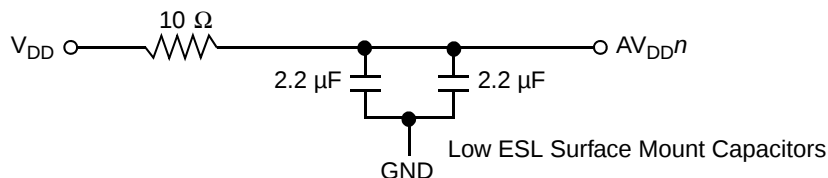


Figure 56. PLL Power Supply Filter Circuit

23.3 Decoupling Recommendations

Due to large address and data buses as well as high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the device system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pins of the device. These decoupling capacitors should receive their power from separate V_{DD} , OV_{DD} , GV_{DD} , LV_{DD} , and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μF . Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

Additionally, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μF (AVX TPS tantalum or Sanyo OSCON).

23.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD} , GV_{DD} , or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , GV_{DD} , LV_{DD} , OV_{DD} , and GND pins of the device.

23.5 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 57). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

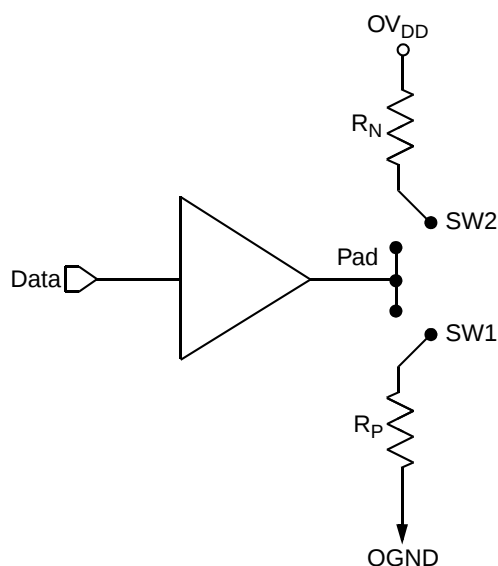


Figure 57. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{\text{source}} \times I_{\text{source}}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term} . The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2) \times I_{\text{source}}$. Solving for the output impedance gives $R_{\text{source}} = R_{\text{term}} \times (V_1/V_2 - 1)$. The drive current is then $I_{\text{source}} = V_1/R_{\text{source}}$.

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD} , nominal OV_{DD} , 105° C.

Table 79. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	20 Target	Z_0	W
R_P	42 Target	25 Target	20 Target	Z_0	W
Differential	NA	NA	NA	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, $T_J = 105^\circ \text{C}$.

23.6 Configuration Pin Muxing

The device provides the user with power-on configuration options that can be set through the use of external pull-up or pull-down resistors of 4.7 k Ω on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

Table 81. SVR Settings (continued)

Device	Package	SVR (Rev. 2.0)	SVR (Rev. 2.1)
MPC8358E	TBGA	0x804A_0020	0x804A_0021
MPC8358	TBGA	0x804B_0020	0x804B_0021

25 Document Revision History

This table provides a revision history for this document.

Table 82. Revision History

Rev. Number	Date	Substantive Change(s)
5	09/2011	• Section 2.2.1, "Power-Up Sequencing", added the current limitation "3A to 5A" for the excessive current. • Section 2.1.2, "Power Supply Voltage Specification", Updated the Characteristic for TBGA (MPC8358 & MPC8360 Device) with specific frequency for Core and PLL voltages. • Added table footnote 3 to Table 2. • Applied table footnotes 1 and 2 to Table 10. • Removed table footnotes from Table 19. • Applied table footnote 8 to the last row of Table 40. • Applied table footnotes 8 and 9 to Table 41. • Applied table footnotes 2 and 3 to Table 45. • Removed table footnotes from Table 46. • Applied table footnote to last three rows of Table 65.
4	01/2011	• Updated references to the LCRR register throughout • Removed references to DDR DLL mode in Section 6.2.2, "DDR and DDR2 SDRAM Output AC Timing Specifications". • Changed "Junction-to-Case" to "Junction-to-Ambient" in Section 22.2.4, "Heat Sinks and Junction-to-Ambient Thermal Resistance", and Table 78, "Heat Sinks and Junction-to-Ambient Thermal Resistance of TBGA Package", titles.