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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8360ecvvajdg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



wide range of protocols including ATM, Ethernet, HDLC, and POS. The QUICC Engine module's enhanced interworking eases the transition and reduces investment costs from ATM to IP based systems. The other major features include a dual DDR SDRAM memory controller for the MPC8360E, which allows equipment providers to partition system parameters and data in an extremely efficient way, such as using one 32-bit DDR memory controller for control plane processing and the other for data plane processing. The MPC8358E has a single DDR SDRAM memory controller. The MPC8360E/58E also offers a 32-bit PCI controller, a flexible local bus, and a dedicated security engine.

This figure shows the MPC8360Eblock diagram.



Figure 1. MPC8360E Block Diagram





Table 4. MPC8360E TBGA Core Power Dissipation ¹	(continued)
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Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
667	333	500	6.1	6.8	W	2, 3, 5, 9

Notes:

- 1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 6.
- 2. Typical power is based on a voltage of V_{DD} = 1.2 V or 1.3 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.
- 3. Thermal solutions need to design to a value higher than typical power on the end application, T_A target, and I/O power.
- 4. Maximum power is based on a voltage of V_{DD} = 1.2 V, WC process, a junction T_J = 105°C, and an artificial smoke test.
- Maximum power is based on a voltage of V_{DD} = 1.3 V for applications that use 667 MHz (CPU)/500 (QE) with WC process, a junction T₁ = 105° C, and an artificial smoke test.
- 6. Typical power is based on a voltage of V_{DD} = 1.3 V, a junction temperature of T_J = 70° C, and a Dhrystone benchmark application.
- Maximum power is based on a voltage of V_{DD} = 1.3 V for applications that use 667 MHz (CPU) or 500 (QE) with WC process, a junction T_J = 70° C, and an artificial smoke test.
- 8. This frequency combination is only available for rev. 2.0 silicon.
- 9. This frequency combination is not available for rev. 2.0 silicon.

Table 5. MPC8358E TBGA Core Power Dissipation¹

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	300	4.1	4.5	W	2, 3, 4
400	266	400	4.5	5.0	W	2, 3, 4

Notes:

- 1. The values do not include I/O supply power (OV_{DD}, LV_{DD} , GV_{DD}) or AV_{DD} . For I/O power values, see Table 6.
- Typical power is based on a voltage of V_{DD} = 1.2 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.
- 3. Thermal solutions need to design to a value higher than typical power on the end application, T_A target, and I/O power.
- 4. Maximum power is based on a voltage of V_{DD} = 1.2 V, WC process, a junction T_J = 105°C, and an artificial smoke test.



DDR and DDR2 SDRAM AC Electrical Characteristics

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 21 and Table 22 provide the output AC timing specifications and measurement conditions for the DDR and DDR2 SDRAM interface.

Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter ⁸	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time, (MCK[n]/MCK[n] crossing)	t _{MCK}	6	10	ns	2
Skew between any MCK to ADDR/CMD 333 MHz 266 MHz 200 MHz	t _{AOSKEW}	-1.0 -1.1 -1.2	0.2 0.3 0.4	ns	3
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz 200 MHz	^t DDKHAS	2.1 2.8 3.5	_	ns	4
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz—DDR1 266 MHz—DDR2 200 MHz	t _{DDKHAX}	2.0 2.7 2.8 3.5		ns	4
MCS(n) output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t _{DDKHCS}	2.1 2.8 3.5	_	ns	4
MCS(n) output hold with respect to MCK 333 MHz 266 MHz 200 MHz	t _{DDKHCX}	2.0 2.7 3.5	_	ns	4
MCK to MDQS	t _{DDKHMH}	-0.8	0.7	ns	5, 9
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	t _{DDKHDS} , t _{DDKLDS}	0.7 1.0 1.2	_	ns	6
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	t _{DDKHDX} , t _{DDKLDX}	0.7 1.0 1.2	_	ns	6
MDQS preamble start	t _{DDKHMP}	$-0.5\timest_{MCK}-0.6$	$-0.5\timest_{\text{MCK}}\text{+}0.6$	ns	7





This section describes the DC and AC electrical specifications for the DUART interface of the MPC8360E/58E.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface of the device.

Table 23. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit	Notes
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V	—
Low-level input voltage OV _{DD}	V _{IL}	-0.3	0.8	V	—
High-level output voltage, I _{OH} = −100 μA	V _{OH}	OV _{DD} - 0.4	—	V	—
Low-level output voltage, I _{OL} = 100 μA	V _{OL}	—	0.2	V	—
Input current (0 V ≰⁄ _{IN} ≤OV _{DD})	I _{IN}	—	±10	μA	1

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface of the device.

Table 24.	DUART	AC T	iming	Speci	ifications
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Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	_
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	_	2

Notes:

- 1. Actual attainable baud rate is limited by the latency of interrupt processing.
- 2. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

8 UCC Ethernet Controller: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

8.1 Three-Speed Ethernet Controller (10/100/1000 Mbps)— GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), MII (media independent interface), RMII (reduced media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The MII, RMII, GMII, and TBI interfaces are only defined for 3.3 V, while the RGMII and RTBI interfaces are only defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet



GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

8.2.1.2 GMII Receive AC Timing Specifications

This table provides the GMII receive AC timing specifications.

Table 28. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
RX_CLK clock period	t _{GRX}	_	8.0	—	ns	_
RX_CLK duty cycle	t _{GRXH} /t _{GRX}	40		60	%	—
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{GRDVKH}	2.0		—	ns	—
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t _{GRDXKH}	0.2		—	ns	2
RX_CLK clock rise time, (20% to 80%)	t _{GRXR}	_		1.0	ns	—
RX_CLK clock fall time, (80% to 20%)	t _{GRXF}	_	_	1.0	ns	—

Notes:

- 1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- In rev. 2.0 silicon, due to errata, t_{GRDXKH} minimum is 0.5 which is not compliant with the standard. Refer to Errata QE_ENET18 in Chip Errata for the MPC8360E, Rev. 1.

This figure shows the GMII receive AC timing diagram.



Figure 11. GMII Receive AC Timing Diagram



GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

8.2.2.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 30. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
RX_CLK clock period 10 Mbps	t _{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t _{MRX}	—	40	—	ns
RX_CLK duty cycle	t _{MRXH} /t _{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t _{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t _{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise time, (20% to 80%)	t _{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time, (80% to 20%)	t _{MRXF}	1.0	—	4.0	ns

Note:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

This figure provides the AC test load.





This figure shows the MII receive AC timing diagram.



Figure 14. MII Receive AC Timing Diagram



GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

Table 32. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with $\text{LV}_{\text{DD}}/\text{OV}_{\text{DD}}$ of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	t _{RMRDVKH}	4.0	_	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	t _{RMRDXKH}	2.0	_	—	ns
REF_CLK clock rise time	t _{RMXR}	1.0	_	4.0	ns
REF_CLK clock fall time	t _{RMXF}	1.0	_	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first three letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{RMRDVKH} symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, t_{RMRDXKL} symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}

This figure provides the AC test load.



Figure 16. AC Test Load

This figure shows the RMII receive AC timing diagram.



Figure 17. RMII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.



8.2.4.1 TBI Transmit AC Timing Specifications

This table provides the TBI transmit AC timing specifications.

Table 33. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
GTX_CLK clock period	t _{TTX}	_	8.0	_	ns	—
GTX_CLK duty cycle	t _{TTXH} /t _{TTX}	40	—	60	%	—
GTX_CLK to TBI data TCG[9:0] delay	t _{TTKHDX} t _{TTKHDV}	1.0	—	 5.0	ns	3
GTX_CLK clock rise time, (20% to 80%)	t _{TTXR}	_	—	1.0	ns	—
GTX_CLK clock fall time, (80% to 20%)	t _{TTXF}	_	_	1.0	ns	—
GTX_CLK125 reference clock period	t _{G125}	_	8.0	_	ns	2
GTX_CLK125 reference clock duty cycle	t _{G125H} /t _{G125}	45	—	55	ns	—

Notes:

- The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 2. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
- 3. In rev. 2.0 silicon, due to errata, t_{TTKHDX} minimum is 0.7 ns for UCC1. Refer to Errata QE_ENET19 in Chip Errata for the MPC8360E, Rev. 1.

This figure shows the TBI transmit AC timing diagram.



Figure 18. TBI Transmit AC Timing Diagram



8.3.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 37. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC frequency	f _{MDC}	—	2.5	—	MHz	2
MDC period	t _{MDC}	—	400	—	ns	—
MDC clock pulse width high	t _{MDCH}	32	—	—	ns	_
MDC to MDIO delay	^t мрткнрх ^t мрткнрv	10 —	_	 110	ns	3
MDIO to MDC setup time	t _{MDRDVKH}	10	—	—	ns	—
MDIO to MDC hold time	t _{MDRDXKH}	0	—	—	ns	—
MDC rise time	t _{MDCR}	—	—	10	ns	—
MDC fall time	t _{MDHF}	_	_	10	ns	

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDRDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
 </sub>
- This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
- 3. This parameter is dependent on the ce_clk speed (that is, for a ce_clk of 200 MHz, the delay is 90 ns and for a ce_clk of 300 MHz, the delay is 63 ns).

This figure shows the MII management AC timing diagram.



Figure 21. MII Management Interface Timing Diagram



Local Bus AC Electrical Specifications



Figure 25. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Enabled)





JTAG DC Electrical Characteristics



Figure 28. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (DLL Enabled)

10 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8360E/58E.

10.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface of the device.

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	—	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V
Input high voltage	V _{IH}	—	2.5	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	$0 V \leq V_{IN} \leq OV_{DD}$	_	±10	μA



10.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device.

This table provides the JTAG AC timing specifications as defined in Figure 30 through Figure 33.

Table 43. JTAG AC Timing Specifications (Independent of CLKIN)¹

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Мах	Unit	Notes
JTAG external clock frequency of operation	f _{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t _{JTG}	30	—	ns	—
JTAG external clock duty cycle	t _{JTKHKL} /t _{JTG}	45	55	%	—
JTAG external clock rise and fall times	t _{JTGR} & t _{JTGF}	0	2	ns	—
TRST assert time	t _{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	t _{JTDVKH} t _{JTIVKH}	4 4		ns	4
Input hold times: Boundary-scan data TMS, TDI	t _{JTDXKH} t _{JTIXKH}	10 10		ns	4
Valid times: Boundary-scan data TDO	t _{JTKLDV} t _{JTKLOV}	2 2	11 11	ns	5
Output hold times: Boundary-scan data TDO	t _{jtkldx} t _{jtklox}	2 2		ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	t _{JTKLDZ} t _{JTKLOZ}	2 2	19 9	ns	5, 6

Notes:

- 2. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
- 4. Non-JTAG signal input timing with respect to t_{TCLK}.
- 5. Non-JTAG signal output timing with respect to t_{TCLK}.
- 6. Guaranteed by design and characterization.

All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 22). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.



Timers AC Timing Specifications

13.2 Timers AC Timing Specifications

This table provides the timer input and output AC timing specifications.

Table 50. Timers Input AC Timing Specifications¹

Characteristic	Symbol ²	Тур	Unit
Timers inputs—minimum pulse width	t _{TIWID}	20	ns

Notes:

- 1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
- 2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

This figure provides the AC test load for the timers.



Figure 39. Timers AC Test Load

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8360E/58E.

14.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the device GPIO.

Table 51. GPIO DC Electrical Charac

Characteristic	Symbol	Condition	Min	Мах	Unit	Notes
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	—	V	1
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V	1
Input low voltage	V _{IL}	—	-0.3	0.8	V	—
Input current	I _{IN}	$0 \ V \leq V_{IN} \leq OV_{DD}$	—	±10	μA	—

Note:

1. This specification applies when operating from 3.3-V supply.



USB DC Electrical Characteristics

19 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8360E/58E.

19.1 USB DC Electrical Characteristics

This table provides the DC electrical characteristics for the USB interface.

Table 64. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
High-level output voltage, $I_{OH} = -100 \ \mu A$	V _{OH}	OV _{DD} - 0.4	—	V
Low-level output voltage, I _{OL} = 100 μA	V _{OL}	—	0.2	V
Input current	I _{IN}	—	±10	μA

19.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface of the device.

Table 65. USB General Timing Parameters

Parameter	Symbol ¹	Min	Max	Unit	Notes	Note
USB clock cycle time	t _{USCK}	20.83		ns	Full speed 48 MHz	_
USB clock cycle time	t _{USCK}	166.67		ns	Low speed 6 MHz	_
Skew between TXP and TXN	t _{USTSPN}	_	5	ns	—	2
Skew among RXP, RXN, and RXD	t _{USRSPND}	_	10	ns	Full speed transitions	2
Skew among RXP, RXN, and RXD	t _{USRPND}		100	ns	Low speed transitions	2

Notes:

The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(state)(signal)} for receive signals and t_{(first two letters of functional block)(state)(signal)} for transmit signals. For example, t_{USRSPND} symbolizes USB timing (US) for the USB receive signals skew (RS) among RXP, RXN, and RXD (PND). Also, t_{USTSPN} symbolizes USB timing (US) for the USB transmit signals skew (TS) between TXP and TXN (PN).

2. Skew measurements are done at $OV_{DD}/2$ of the rising or falling edge of the signals.

This figure provide the AC test load for the USB.



Figure 52. USB AC Test Load



NP

20.3 Pinout Listings

Refer to AN3097, "MPC8360/MPC8358E PowerQUICC Design Checklist," for proper pin termination and usage.

This table shows the pin list of the MPC8360E TBGA package.

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Pri	mary DDR SDRAM Memory Controller Interface			
MEMC1_MDQ[0:31]	AJ34, AK33, AL33, AL35, AJ33, AK34, AK32, AM36, AN37, AN35, AR34, AT34, AP37, AP36, AR36, AT35, AP34, AR32, AP32, AM31, AN33, AM34, AM33, AM30, AP31, AM27, AR30, AT32, AN29, AP29, AN27, AR29	I/O	GV _{DD}	_
MEMC1_MDQ[32:63]/ MEMC2_MDQ[0:31]	AN8, AN7, AM8, AM6, AP9, AN9, AT7, AP7, AU6, AP6, AR4, AR3, AT6, AT5, AR5, AT3, AP4, AM5, AP3, AN3, AN5, AL5, AN4, AM2, AL2, AH5, AK3, AJ2, AJ3, AH4, AK4, AH3	I/O	GV _{DD}	_
MEMC1_MECC[0:4]/ MSRCID[0:4]	AP24, AN22, AM19, AN19, AM24	I/O	GV _{DD}	_
MEMC1_MECC[5]/ MDVAL	AM23	I/O	GV _{DD}	—
MEMC1_MECC[6:7]	AM22, AN18	I/O	GV _{DD}	—
MEMC1_MDM[0:3]	AL36, AN34, AP33, AN28	0	GV _{DD}	—
MEMC1_MDM[4:7]/ MEMC2_MDM[0:3]	AT9, AU4, AM3, AJ6	0	GV _{DD}	—
MEMC1_MDM[8]	AP27	0	GV _{DD}	—
MEMC1_MDQS[0:3]	AK35, AP35, AN31, AM26	I/O	GV _{DD}	—
MEMC1_MDQS[4:7]/ MEMC2_MDQS[0:3]	AT8, AU3, AL4, AJ5	I/O	GV _{DD}	—
MEMC1_MDQS[8]	AP26	I/O	GV _{DD}	—
MEMC1_MBA[0:1]	AU29, AU30	0	GV _{DD}	—
MEMC1_MBA[2]	AT30	0	GV _{DD}	—
MEMC1_MA[0:14]	AU21, AP22, AP21, AT21, AU25, AU26, AT23, AR26, AU24, AR23, AR28, AU23, AR22, AU20, AR18	0	GV _{DD}	-
MEMC1_MODT[0:1]	AG33, AJ36	0	GV _{DD}	6
MEMC1_MODT[2:3]/ MEMC2_MODT[0:1]	AT1, AK2	0	GV _{DD}	6
MEMC1_MWE	AT26	0	GV _{DD}	—
MEMC1_MRAS	AT29	0	GV _{DD}	—
MEMC1_MCAS	AT24	0	GV _{DD}	_
MEMC1_MCS[0:1]	AU27, AT27	0	GV _{DD}	_
MEMC1_MCS[2:3]/ MEMC2_MCS[0:1]	AU8, AU7	0	GV _{DD}	

Table 66. MPC8360E TBGA Pinout Listing



Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes					
IRQ[4:5]	G33, G32	I/O	OV _{DD}	—					
IRQ[6]/LCS[6]/CKSTOP_OUT	E35	I/O	OV _{DD}	—					
IRQ[7]/LCS[7]/CKSTOP_IN	H36	I/O	OV _{DD}	—					
	DUART								
UART1_SOUT/M1SRCID[0]/ M2SRCID[0]/LSRCID[0]	E32	0	OV _{DD}	_					
UART1_SIN/M1SRCID[1]/ M2SRCID[1]/LSRCID[1]	B34	I/O	OV _{DD}						
UART1_CTS/M1SRCID[2]/ M2SRCID[2]/LSRCID[2]	C34	I/O	OV _{DD}						
UART1_RTS/M1SRCID[3]/ M2SRCID[3]/LSRCID[3]	A35	0	OV _{DD}	_					
	I ² C Interface								
IIC1_SDA	D34	I/O	OV _{DD}	2					
IIC1_SCL	B35	I/O	OV _{DD}	2					
IIC2_SDA	E33	I/O	OV _{DD}	2					
IIC2_SCL	C35	I/O	OV _{DD}	2					
	QUICC Engine								
CE_PA[0]	F8	I/O	LV _{DD0}	—					
CE_PA[1:2]	AH1, AG5	I/O	OV _{DD}	—					
CE_PA[3:7]	F6, D4, C3, E5, A3	I/O	LV _{DD} 0	—					
CE_PA[8]	AG3	I/O	OV _{DD}	—					
CE_PA[9:12]	F7, B3, E6, B4	I/O	LV _{DD} 0	—					
CE_PA[13:14]	AG1, AF6	I/O	OV _{DD}	—					
CE_PA[15]	B2	I/O	LV _{DD} 0	—					
CE_PA[16]	AF4	I/O	OV _{DD}	—					
CE_PA[17:21]	B16, A16, E17, A17, B17	I/O	LV _{DD} 1	—					
CE_PA[22]	AF3	I/O	OV _{DD}	—					
CE_PA[23:26]	C18, D18, E18, A18	I/O	LV _{DD} 1	—					
CE_PA[27:28]	AF2, AE6	I/O	OV _{DD}	—					
CE_PA[29]	B19	I/O	LV _{DD} 1	—					
CE_PA[30]	AE5	I/O	OV_{DD}	—					
CE_PA[31]	F16	I/O	LV _{DD} 1	—					



Pinout Listings

21 Clocking

This figure shows the internal distribution of clocks within the MPC8360E.



Figure 54. MPC8360E Clock Subsystem



where:

 T_I = junction temperature (° C)

 $T_I = T_B + (R_{\theta IB} \times P_D)$

 T_B = board temperature at the package perimeter (° C)

 $R_{\theta JA}$ = junction to board thermal resistance (° C/W) per JESD51-8

 P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

22.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

 T_J = junction temperature (° C)

 T_T = thermocouple temperature on top of package (° C)

 Ψ_{IT} = junction-to-ambient thermal resistance (° C/W)

 P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

22.2.4 Heat Sinks and Junction-to-Ambient Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

 $R_{\theta JA}$ = junction-to-ambient thermal resistance (° C/W)

 $R_{\theta JC}$ = junction-to-case thermal resistance (° C/W)

 $R_{\theta CA}$ = case-to-ambient thermal resistance (° C/W)

 $R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.



23.7 Pull-Up Resistor Requirements

The device requires high resistance pull-up resistors (10 k Ω is recommended) on open drain type pins including I²C pins, Ethernet Management MDIO pin, and EPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, see *MPC8360E/MPC8358E PowerQUICC Design Checklist* (AN3097).

24 Ordering Information

24.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the MPC8360E/58E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. Additionally to the processor frequency, the part numbering scheme also includes an application modifier, which may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number.

MPC	nnnn	е	t	рр	aa	а	а	Α
Product Code	Part Identifier	Encryption Acceleration	Temperature Range	Package ²	Processor Frequency ³	Platform Frequency	QUICC Engine Frequency	Die Revision
MPC	8358	Blank = not included E = included	Blank = 0° C T _A to 105° C T _J	ZU = TBGA VV = TBGA (no lead)	e300 core speed AD = 266 MHz AG = 400 MHz	D = 266 MHz	E = 300 MHz G = 400 MHz	A = rev. 2.1 silicon
	8360		to 105° C T _J	C T _A C T _J	e300 core speed AG = 400 MHz AJ = 533 MHz AL = 667 MHz	D = 266 MHz F = 333 MHz	G = 400 MHz H = 500 MHz	A = rev. 2.1 silicon
MPC (rev. 2.0 silicon only)	8360	Blank = not included E = included	0° C T _A to 70° C T _J	ZU = TBGA VV = TBGA (no lead)	e300 core speed AH = 500 MHz AL = 667 MHz	F = 333 MHz	G = 400 MHz H = 500 MHz	_

Table 80. Part Numbering Nomenclature¹

Notes:

1. Not all processor, platform, and QUICC Engine block frequency combinations are supported. For available frequency combinations, contact your local Freescale sales office or authorized distributor.

2. See Section 20, "Package and Pin Listings," for more information on available package types.

Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this
specification support all core frequencies. Additionally, parts addressed by part number specifications may support other
maximum core frequencies.

This table shows the SVR settings by device and package type.

Table 81.	SVR	Settings
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Device	Package	SVR (Rev. 2.0)	SVR (Rev. 2.1)
MPC8360E	TBGA	0x8048_0020	0x8048_0021
MPC8360	TBGA	0x8049_0020	0x8049_0021



Table 82.	Revision	History	(continued)
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Rev. Number	Date	Substantive Change(s)	
3	03/2010	Substantive Change(s) Changed references to RCWH[PCICKEN] to RCWH[PCICKDRV]. In Table 2, added extended temperature characteristics. Added Figure 6, "DDR Input Timing Diagram." In Figure 53, "Mechanical Dimensions and Bottom Surface Nomenclature of the TBGA Package," removed watermark. Updated the title of Table 19,"DDR SDRAM Input AC Timing Specifications." In Table 20, "DDR and DDR2 SDRAM Input AC Timing Specifications Mode," changed table subtitle. In Table 27-Table 30, and Table 33—Table 34, changed the rise and fall time specifications to reference 20–80% and 80–20% of the voltage supply, respectively. In Table 35, "IEEE 1588 Timer AC Specifications," changed first parameter to "Timer clock frequency." In Table 36, "MPC8360E TBGA Pinout Listing," and Table 67 "MPC8358E TBGA Pinout Listing, added note 7: "This pin must always be tied to GND" to the TEST pin and added a note to SPARE1 stating: "This pin must always be left not connected." In Section 4.3, "Gigabit Reference Clock Input Timing." Updated Section 8.1.1, "10/100/1000 Ethernet DC Electrical Characteristics." In Section 20.3, "Pinout Listings," added sentence stating "Refer to AN3097, 'MPC8360/MPC8358E PowerQUICC Design Checklist,' for proper pin termination and usage." In Section 21.1, "Clocking," removed statement: "The OCCR[PCICDn] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_	
2	12/2007	Initial release.	