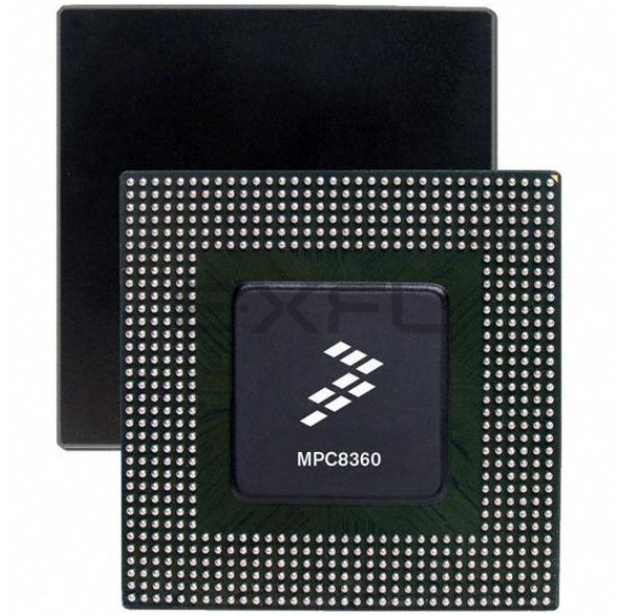


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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e300 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 533MHz |
| Co-Processors/DSP | Communications; QUICC Engine, Security; SEC |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (1) |
| SATA | - |
| USB | USB 1.x (1) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 740-LBGA |
| Supplier Device Package | 740-TBGA (37.5x37.5) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8360eczuajdg |

wide range of protocols including ATM, Ethernet, HDLC, and POS. The QUICC Engine module's enhanced interworking eases the transition and reduces investment costs from ATM to IP based systems. The other major features include a dual DDR SDRAM memory controller for the MPC8360E, which allows equipment providers to partition system parameters and data in an extremely efficient way, such as using one 32-bit DDR memory controller for control plane processing and the other for data plane processing. The MPC8358E has a single DDR SDRAM memory controller. The MPC8360E/58E also offers a 32-bit PCI controller, a flexible local bus, and a dedicated security engine.

This figure shows the MPC8360Eblock diagram.

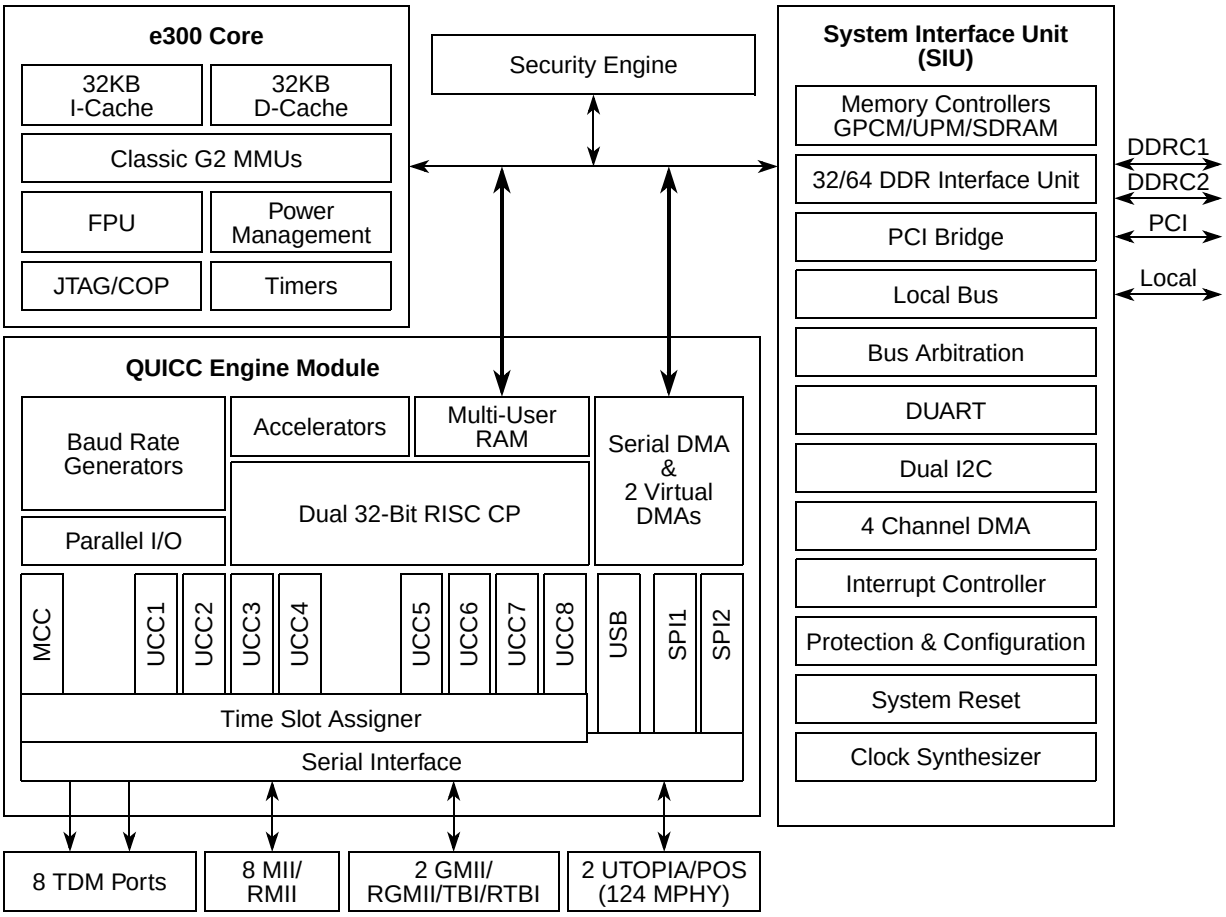


**Figure 1. MPC8360E Block Diagram**

  - Programmable highest priority request
  - Four groups of interrupts with programmable priority
  - External and internal interrupts directed to communication processor
  - Redirects interrupts to external $\overline{\text{INTA}}$ pin when in core disable mode
  - Unique vector number for each interrupt source
- Dual industry-standard $I^2C$ interfaces
  - Two-wire interface
  - Multiple master support
  - Master or slave $I^2C$ mode support
  - On-chip digital filtering rejects spikes on the bus
  - System initialization data is optionally loaded from $I^2C$-1 EPROM by boot sequencer embedded hardware
- DMA controller
  - Four independent virtual channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - All channels accessible by local core and remote PCI masters
  - Misaligned transfer capability
  - Data chaining and direct mode
  - Interrupt on completed segment and chain
  - DMA external handshake signals: $\overline{\text{DMA\_DREQ}}$[0:3]/$\overline{\text{DMA\_DACK}}$[0:3]/$\overline{\text{DMA\_DONE}}$[0:3]. There is one set for each DMA channel. The pins are multiplexed to the parallel IO pins with other QE functions.
- DUART
  - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- System timers
  - Periodic interrupt timer
  - Real-time clock
  - Software watchdog timer
  - Eight general-purpose timers
- IEEE Std. 1149.1™-compliant, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

# 2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8360E/58E. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

**Table 4. MPC8360E TBGA Core Power Dissipation[1] (continued)**

| Core Frequency (MHz) | CSB Frequency (MHz) | QUICC Engine Frequency (MHz) | Typical | Maximum | Unit | Notes |
|---|---|---|---|---|---|---|
| 667 | 333 | 500 | 6.1 | 6.8 | W | 2, 3, 5, 9 |

**Notes:**
1. The values do not include I/O supply power ($OV_{DD}$, $LV_{DD}$, $GV_{DD}$) or $AV_{DD}$. For I/O power values, see Table 6.
2. Typical power is based on a voltage of $V_{DD}$ = 1.2 V or 1.3 V, a junction temperature of $T_J$ = 105° C, and a Dhrystone benchmark application.
3. Thermal solutions need to design to a value higher than typical power on the end application, $T_A$ target, and I/O power.
4. Maximum power is based on a voltage of $V_{DD}$ = 1.2 V, WC process, a junction $T_J$ = 105° C, and an artificial smoke test.
5. Maximum power is based on a voltage of $V_{DD}$ = 1.3 V for applications that use 667 MHz (CPU)/500 (QE) with WC process, a junction $T_J$ = 105° C, and an artificial smoke test.
6. Typical power is based on a voltage of $V_{DD}$ = 1.3 V, a junction temperature of $T_J$ = 70° C, and a Dhrystone benchmark application.
7. Maximum power is based on a voltage of $V_{DD}$ = 1.3 V for applications that use 667 MHz (CPU) or 500 (QE) with WC process, a junction $T_J$ = 70° C, and an artificial smoke test.
8. This frequency combination is only available for rev. 2.0 silicon.
9. This frequency combination is not available for rev. 2.0 silicon.

**Table 5. MPC8358E TBGA Core Power Dissipation[1]**

| Core Frequency (MHz) | CSB Frequency (MHz) | QUICC Engine Frequency (MHz) | Typical | Maximum | Unit | Notes |
|---|---|---|---|---|---|---|
| 266 | 266 | 300 | 4.1 | 4.5 | W | 2, 3, 4 |
| 400 | 266 | 400 | 4.5 | 5.0 | W | 2, 3, 4 |

**Notes:**
1. The values do not include I/O supply power ($OV_{DD}$, $LV_{DD}$, $GV_{DD}$) or $AV_{DD}$. For I/O power values, see Table 6.
2. Typical power is based on a voltage of $V_{DD}$ = 1.2 V, a junction temperature of $T_J$ = 105° C, and a Dhrystone benchmark application.
3. Thermal solutions need to design to a value higher than typical power on the end application, $T_A$ target, and I/O power.
4. Maximum power is based on a voltage of $V_{DD}$ = 1.2 V, WC process, a junction $T_J$ = 105° C, and an artificial smoke test.

## 4.1 DC Electrical Characteristics

This table provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the device.

**Table 7. CLKIN DC Electrical Characteristics**

| Parameter | Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | — | $V_{IH}$ | 2.7 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | — | $V_{IL}$ | –0.3 | 0.4 | V |
| CLKIN input current | 0 V ≤$V_{IN}$ ≤$OV_{DD}$ | $I_{IN}$ | — | ±10 | μA |
| PCI_SYNC_IN input current | 0 V ≤$V_{IN}$ ≤0.5V or $OV_{DD}$ – 0.5V ≤$V_{IN}$ ≤$OV_{DD}$ | $I_{IN}$ | — | ±10 | μA |
| PCI_SYNC_IN input current | 0.5 V ≤$V_{IN}$ ≤$OV_{DD}$ – 0.5 V | $I_{IN}$ | — | ±100 | μA |

## 4.2 AC Electrical Characteristics

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

**Table 8. CLKIN AC Timing Specifications**

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| CLKIN/PCI_CLK frequency | $f_{CLKIN}$ | — | — | 66.67 | MHz | 1 |
| CLKIN/PCI_CLK cycle time | $t_{CLKIN}$ | 15 | — | — | ns | — |
| CLKIN/PCI_CLK rise and fall time | $t_{KH}$, $t_{KL}$ | 0.6 | 1.0 | 2.3 | ns | 2 |
| CLKIN/PCI_CLK duty cycle | $t_{KHK}/t_{CLKIN}$ | 40 | — | 60 | % | 3 |
| CLKIN/PCI_CLK jitter | — | — | — | ±150 | ps | 4, 5 |

**Notes:**

1. **Caution:** The system, core, USB, security, and 10/100/1000 Ethernet must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.

## 4.3 Gigabit Reference Clock Input Timing

This table provides the Gigabit reference clocks (GTX_CLK125) AC timing specifications.

**Table 9. GTX_CLK125 AC Timing Specifications**

**At recommended operating conditions with $LV_{DD}$ = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV**

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| GTX_CLK125 frequency | $t_{G125}$ | — | 125 | — | MHz | — |
| GTX_CLK125 cycle time | $t_{G125}$ | — | 8 | — | ns | — |

**Table 9. GTX_CLK125 AC Timing Specifications**

**At recommended operating conditions with $LV_{DD}$ = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV (continued)**

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| GTX_CLK rise and fall time<br>$LV_{DD}$ = 2.5 V<br>$LV_{DD}$ = 3.3 V | $t_{G125R}/t_{G125F}$ | — | — | <br>0.75<br>1.0 | ns | 1 |
| GTX_CLK125 duty cycle<br>GMII & TBI<br>1000Base-T for RGMII & RTBI | $t_{G125H}/t_{G125}$ | <br>45<br>47 | — | <br>55<br>53 | % | 2 |
| GTX_CLK125 jitter | — | — | — | ±150 | ps | 2 |

**Notes:**

1. Rise and fall times for GTX_CLK125 are measured from 0.5 and 2.0 V for $LV_{DD}$ = 2.5 V and from 0.6 and 2.7 V for $LV_{DD}$ = 3.3 V.
2. GTX_CLK125 is used to generate the GTX clock for the UCC Ethernet transmitter with 2% degradation. The GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by GTX_CLK. See Section 8.2.2, “MII AC Timing Specifications,” Section 8.2.3, “RMII AC Timing Specifications,” and Section 8.2.5, “RGMII and RTBI AC Timing Specifications” for the duty cycle for 10Base-T and 100Base-T reference clock.

# 5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8360E/58E.

## 5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins of the device.

**Table 10. RESET Pins DC Electrical Characteristics [1]**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | 2.0 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | — | — | ±10 | μA |
| Output high voltage | $V_{OH}$[2] | $I_{OH}$ = –8.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |

**Notes:**

1. This table applies for pins $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, and $\overline{\text{QUIESCE}}$.
2. $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are open drain pins, thus $V_{OH}$ is not relevant for those pins.

## 5.2 RESET AC Electrical Characteristics

This section describes the AC electrical specifications for the reset initialization timing requirements of the device. This table provides the reset initialization AC timing specifications for the DDR SDRAM component(s).

**Table 11. RESET Initialization Timing Specifications**

| Parameter/Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow | 32 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the device is in PCI host mode | 32 | — | $t_{CLKIN}$ | 2 |
| Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the device is in PCI agent mode | 32 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| $\overline{\text{HRESET}}$/$\overline{\text{SRESET}}$ assertion (output) | 512 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| $\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output) | 16 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode | 4 | — | $t_{CLKIN}$ | 2 |
| Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode | 4 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$ | 0 | — | ns | — |
| Time for the device to turn off POR config signals with respect to the assertion of $\overline{\text{HRESET}}$ | — | 4 | ns | 3 |
| Time for the device to turn on POR config signals with respect to the negation of $\overline{\text{HRESET}}$ | 1 | — | $t_{PCI\_SYNC\_IN}$ | 1, 3 |

**Notes:**

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. Refer *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
2. $t_{CLKIN}$ is the clock period of the input clock applied to CLKIN. It is only valid when the device is in PCI host mode. Refer *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
3. POR config signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

This table provides the PLL and DLL lock times.

**Table 12. PLL and DLL Lock Times**

| Parameter/Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|
| PLL lock times | — | 100 | µs | — |
| DLL lock times | 7680 | 122,880 | csb_clk cycles | 1, 2 |

**Notes:**

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 21, “Clocking,” for more information.

## 6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 21 and Table 22 provide the output AC timing specifications and measurement conditions for the DDR and DDR2 SDRAM interface.

**Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode**

At recommended operating conditions with $GV_{DD}$ of (1.8 V or 2.5 V) ± 5%.

| Parameter[8] | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| MCK[n] cycle time, (MCK[n]/$\overline{\text{MCK}}$[n] crossing) | $t_{MCK}$ | 6 | 10 | ns | 2 |
| Skew between any MCK to ADDR/CMD<br>333 MHz<br>266 MHz<br>200 MHz | $t_{AOSKEW}$ | <br>–1.0<br>–1.1<br>–1.2 | <br>0.2<br>0.3<br>0.4 | ns | 3 |
| ADDR/CMD output setup with respect to MCK<br>333 MHz<br>266 MHz<br>200 MHz | $t_{DDKHAS}$ | <br>2.1<br>2.8<br>3.5 | — | ns | 4 |
| ADDR/CMD output hold with respect to MCK<br>333 MHz<br>266 MHz—DDR1<br>266 MHz—DDR2<br>200 MHz | $t_{DDKHAX}$ | <br>2.0<br>2.7<br>2.8<br>3.5 | — | ns | 4 |
| $\overline{\text{MCS}}$(n) output setup with respect to MCK<br>333 MHz<br>266 MHz<br>200 MHz | $t_{DDKHCS}$ | <br>2.1<br>2.8<br>3.5 | — | ns | 4 |
| $\overline{\text{MCS}}$(n) output hold with respect to MCK<br>333 MHz<br>266 MHz<br>200 MHz | $t_{DDKHCX}$ | <br>2.0<br>2.7<br>3.5 | — | ns | 4 |
| MCK to MDQS | $t_{DDKHMH}$ | –0.8 | 0.7 | ns | 5, 9 |
| MDQ/MECC/MDM output setup with respect to MDQS<br>333 MHz<br>266 MHz<br>200 MHz | $t_{DDKHDS}$, $t_{DDKLDS}$ | <br>0.7<br>1.0<br>1.2 | — | ns | 6 |
| MDQ/MECC/MDM output hold with respect to MDQS<br>333 MHz<br>266 MHz<br>200 MHz | $t_{DDKHDX}$, $t_{DDKLDX}$ | <br>0.7<br>1.0<br>1.2 | — | ns | 6 |
| MDQS preamble start | $t_{DDKHMP}$ | $-0.5 \times t_{MCK} - 0.6$ | $-0.5 \times t_{MCK} + 0.6$ | ns | 7 |

**Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)**

At recommended operating conditions with $GV_{DD}$ of (1.8 V or 2.5 V) ± 5%.

| Parameter[8] | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| MDQS epilogue end | $t_{DDKHME}$ | –0.6 | 0.9 | ns | 7 |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, $t_{DDKHAS}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, $t_{DDKLDX}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. In the source synchronous mode, MCK/$\overline{\text{MCK}}$ can be shifted in ¼ applied cycle increments through the clock control register. For the skew measurements referenced for $t_{AOSKEW}$ it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
4. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.
5. Note that $t_{DDKHMH}$ follows the symbol conventions described in note 1. For example, $t_{DDKHMH}$ describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). $t_{DDKHMH}$ can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. Refer *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the device.
7. All outputs are referenced to the rising edge of MCK(n) at the pins of the device. Note that $t_{DDKHMP}$ follows the symbol conventions described in note 1.
8. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.
9. In rev. 2.0 silicon, $t_{DDKHMH}$ maximum meets the specification of 0.6 ns. In rev. 2.0 silicon, due to errata, $t_{DDKHMH}$ minimum is –0.9 ns. Refer to Errata DDR18 in *Chip Errata for the MPC8360E, Rev. 1*.

This figure shows the DDR SDRAM output timing for address skew with respect to any MCK.

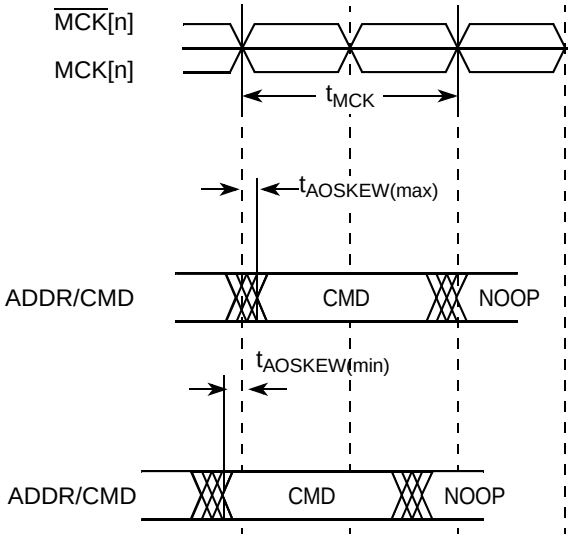


**Figure 7. Timing Diagram for $t_{AOSKEW}$ Measurement**

Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for the MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

### 8.1.1 10/100/1000 Ethernet DC Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), reduced media independent interface (RMII) signals, management data input/output (MDIO) and management data clock (MDC).

The MII and RMII interfaces are defined for 3.3 V, while the RGMII and RTBI interfaces can be operated at 2.5 V. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3.* The RMII interface follows the *RMII Consortium RMII Specification Version 1.2.*

**Table 25. RGMII/RTBI, GMII, TBI, MII, and RMII DC Electrical Characteristics (when operating at 3.3 V)**

| Parameter | Symbol | Conditions | | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Supply voltage 3.3 V | $LV_{DD}$ | — | | 2.97 | 3.63 | V | 1 |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –4.0 mA | $LV_{DD}$ = Min | 2.40 | $LV_{DD}$ + 0.3 | V | — |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 4.0 mA | $LV_{DD}$ = Min | GND | 0.50 | V | — |
| Input high voltage | $V_{IH}$ | — | — | 2.0 | $LV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | — | — | –0.3 | 0.90 | V | — |
| Input current | $I_{IN}$ | 0 V ≤$V_{IN}$ ≤$LV_{DD}$ | | — | ±10 | μA | — |

**Note:**
1. GMII/MII pins that are not needed for RGMII, RMII, or RTBI operation are powered by the $OV_{DD}$ supply.

**Table 26. RGMII/RTBI DC Electrical Characteristics (when operating at 2.5 V)**

| Parameters | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage 2.5 V | $LV_{DD}$ | — | | 2.37 | 2.63 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –1.0 mA | $LV_{DD}$ = Min | 2.00 | $LV_{DD}$ + 0.3 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 1.0 mA | $LV_{DD}$ = Min | GND – 0.3 | 0.40 | V |
| Input high voltage | $V_{IH}$ | — | $LV_{DD}$ = Min | 1.7 | $LV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | $LV_{DD}$ = Min | –0.3 | 0.70 | V |
| Input current | $I_{IN}$ | 0 V ≤$V_{IN}$ ≤$LV_{DD}$ | | — | ±10 | μA |

## 8.2 GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

### 8.2.1 GMII Timing Specifications

This sections describe the GMII transmit and receive AC timing specifications.

### 8.2.1.2 GMII Receive AC Timing Specifications

This table provides the GMII receive AC timing specifications.

**Table 28. GMII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/OV_{DD}$ of 3.3 V ± 10%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| RX_CLK clock period | $t_{GRX}$ | — | 8.0 | — | ns | — |
| RX_CLK duty cycle | $t_{GRXH}/t_{GRX}$ | 40 | — | 60 | % | — |
| RXD[7:0], RX_DV, RX_ER setup time to RX_CLK | $t_{GRDVKH}$ | 2.0 | — | — | ns | — |
| RXD[7:0], RX_DV, RX_ER hold time to RX_CLK | $t_{GRDXKH}$ | 0.2 | — | — | ns | 2 |
| RX_CLK clock rise time, (20% to 80%) | $t_{GRXR}$ | — | — | 1.0 | ns | — |
| RX_CLK clock fall time, (80% to 20%) | $t_{GRXF}$ | — | — | 1.0 | ns | — |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{GRDVKH}$ symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{RX}$ clock reference (K) going to the high state (H) or setup time. Also, $t_{GRDXKL}$ symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{GRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{GRX}$ represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In rev. 2.0 silicon, due to errata, $t_{GRDXKH}$ minimum is 0.5 which is not compliant with the standard. Refer to Errata *QE_ENET18* in *Chip Errata for the MPC8360E, Rev. 1*.

This figure shows the GMII receive AC timing diagram.

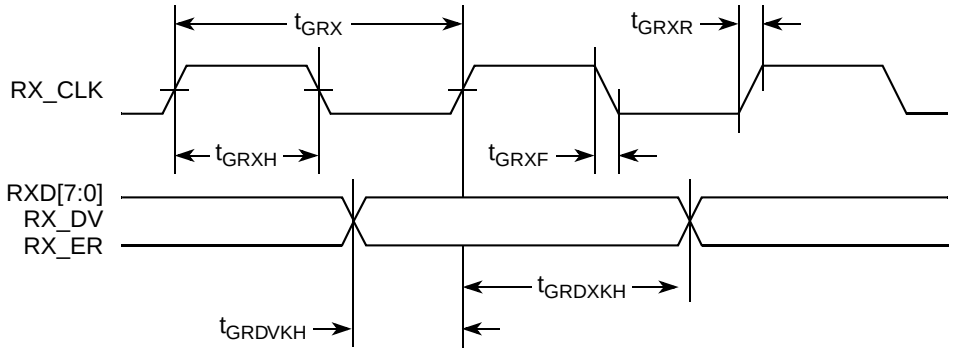


**Figure 11. GMII Receive AC Timing Diagram**

### 8.2.2.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

**Table 30. MII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}/OV_{DD}$ of 3.3 V ± 10%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period 10 Mbps | $t_{MRX}$ | — | 400 | — | ns |
| RX_CLK clock period 100 Mbps | $t_{MRX}$ | — | 40 | — | ns |
| RX_CLK duty cycle | $t_{MRXH}/t_{MRX}$ | 35 | — | 65 | % |
| RXD[3:0], RX_DV, RX_ER setup time to RX_CLK | $t_{MRDVKH}$ | 10.0 | — | — | ns |
| RXD[3:0], RX_DV, RX_ER hold time to RX_CLK | $t_{MRDXKH}$ | 10.0 | — | — | ns |
| RX_CLK clock rise time, (20% to 80%) | $t_{MRXR}$ | 1.0 | — | 4.0 | ns |
| RX_CLK clock fall time, (80% to 20%) | $t_{MRXF}$ | 1.0 | — | 4.0 | ns |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MRDVKH}$ symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{MRDXKL}$ symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{MRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{MRX}$ represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load.

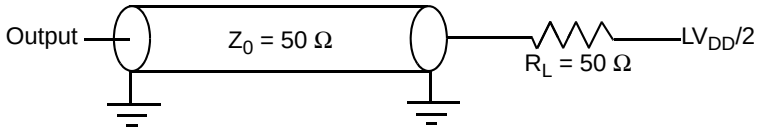


**Figure 13. AC Test Load**

This figure shows the MII receive AC timing diagram.

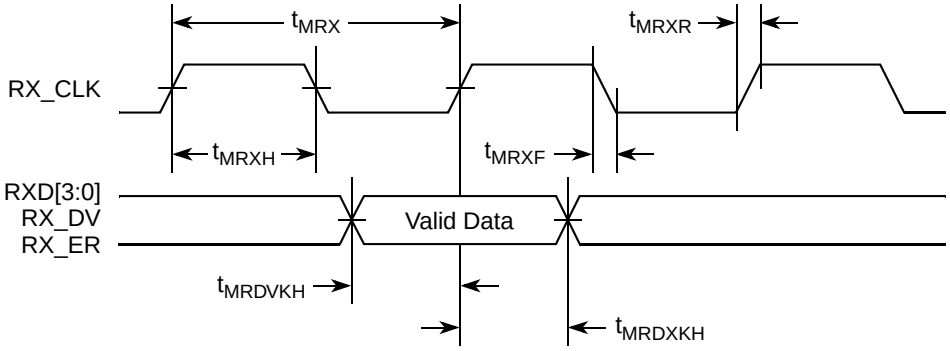


**Figure 14. MII Receive AC Timing Diagram**

**Table 40. Local Bus General Timing Parameters—DLL Enabled (continued)**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| LUPWAIT input hold from local bus clock | $t_{LBIXKH2}$ | 1.0 | — | ns | 3, 4 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT1}$ | 1.5 | — | ns | 5 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT2}$ | 3.0 | — | ns | 6 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT3}$ | 2.5 | — | ns | 7 |
| Local bus clock to LALE rise | $t_{LBKHLR}$ | — | 4.5 | ns | — |
| Local bus clock to output valid (except LAD/LDP and LALE) | $t_{LBKHOV1}$ | — | 4.5 | ns | — |
| Local bus clock to data valid for LAD/LDP | $t_{LBKHOV2}$ | — | 4.5 | ns | 3 |
| Local bus clock to address valid for LAD | $t_{LBKHOV3}$ | — | 4.5 | ns | 3 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKHOX1}$ | 1.0 | — | ns | 3 |
| Output hold from local bus clock for LAD/LDP | $t_{LBKHOX2}$ | 1.0 | — | ns | 3 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKHOZ}$ | — | 3.8 | ns | 8 |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one (1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to rising edge of LSYNC_IN.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This table describes the general timing parameters of the local bus interface of the device.

**Table 41. Local Bus General Timing Parameters—DLL Bypass Mode[9]**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus cycle time | $t_{LBK}$ | 15 | — | ns | 2 |
| Input setup to local bus clock | $t_{LBIVKH}$ | 7 | — | ns | 3, 4 |
| Input hold from local bus clock | $t_{LBIXKH}$ | 1.0 | — | ns | 3, 4 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT1}$ | 1.5 | — | ns | 5 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT2}$ | 3 | — | ns | 6 |
| LALE output fall to LAD output transition (LATCH hold time) | $t_{LBOTOT3}$ | 2.5 | — | ns | 7 |

## 10.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device.

This table provides the JTAG AC timing specifications as defined in Figure 30 through Figure 33.

**Table 43. JTAG AC Timing Specifications (Independent of CLKIN)[1]**

At recommended operating conditions (see Table 2).

| Parameter | Symbol [2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| JTAG external clock frequency of operation | $f_{JTG}$ | 0 | 33.3 | MHz | — |
| JTAG external clock cycle time | $t_{JTG}$ | 30 | — | ns | — |
| JTAG external clock duty cycle | $t_{JTKHKL}/t_{JTG}$ | 45 | 55 | % | — |
| JTAG external clock rise and fall times | $t_{JTGR}$ & $t_{JTGF}$ | 0 | 2 | ns | — |
| $\overline{\text{TRST}}$ assert time | $t_{TRST}$ | 25 | — | ns | 3 |
| Input setup times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDVKH}$<br>$t_{JTIVKH}$ | <br>4<br>4 | <br>—<br>— | ns | 4 |
| Input hold times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDXKH}$<br>$t_{JTIXKH}$ | <br>10<br>10 | <br>—<br>— | ns | 4 |
| Valid times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDV}$<br>$t_{JTKLOV}$ | <br>2<br>2 | <br>11<br>11 | ns | 5 |
| Output hold times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDX}$<br>$t_{JTKLOX}$ | <br>2<br>2 | <br>—<br>— | ns | 5 |
| JTAG external clock to output high impedance:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDZ}$<br>$t_{JTKLOZ}$ | <br>2<br>2 | <br>19<br>9 | ns | 5, 6 |

**Notes:**

1. All outputs are measured from the midpoint voltage of the falling/rising edge of $t_{TCLK}$ to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 22). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{JTDVKH}$ symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{JTDXKH}$ symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the $t_{JTG}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to $t_{TCLK}$.
5. Non-JTAG signal output timing with respect to $t_{TCLK}$.
6. Guaranteed by design and characterization.

## 15.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

**Table 54. IPIC Input AC Timing Specifications[1]**

| Characteristic | Symbol[2] | Min | Unit |
|---|---|---|---|
| IPIC inputs—minimum pulse width | $t_{PIWID}$ | 20 | ns |

**Notes:**
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least $t_{PIWID}$ ns to ensure proper operation when working in edge triggered mode.

# 16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8360E/58E.

## 16.1 SPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the device SPI.

**Table 55. SPI DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –6.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 6.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |
| Input high voltage | $V_{IH}$ | — | 2.0 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | 0 V ≤$V_{IN}$ ≤$OV_{DD}$ | — | ±10 | μA |

## 16.2 SPI AC Timing Specifications

This table and provide the SPI input and output AC timing specifications.

**Table 56. SPI AC Timing Specifications[1]**

| Characteristic | Symbol[2] | Min | Max | Unit |
|---|---|---|---|---|
| SPI outputs—Master mode (internal clock) delay | $t_{NIKHOX}$<br>$t_{NIKHOV}$ | 0.3<br>— | —<br>8 | ns |
| SPI outputs—Slave mode (external clock) delay | $t_{NEKHOX}$<br>$t_{NEKHOV}$ | 2<br>— | —<br>8 | ns |
| SPI inputs—Master mode (internal clock) input setup time | $t_{NIIVKH}$ | 8 | — | ns |
| SPI inputs—Master mode (internal clock) input hold time | $t_{NIIXKH}$ | 0 | — | ns |
| SPI inputs—Slave mode (external clock) input setup time | $t_{NEIVKH}$ | 4 | — | ns |

The QUICC Engine block VCO frequency is derived from the following equations:

*ce_clk* = (primary clock input × CEPMF) ÷ (1 + CEPDF)

QE VCO Frequency = *ce_clk* × VCO divider × (1 + CEPDF)

## 21.4 Suggested PLL Configurations

To simplify the PLL configurations, the device might be separated into two clock domains. The first domain contains the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine block PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. This table shows suggested PLL configurations for 33 and 66 MHz input clocks and illustrates each of the clock domains separately. Any combination of clock domains setting with same input clock are valid. Refer to Section 21, "Clocking," for the appropriate operating frequencies for your device.

**Table 76. Suggested PLL Configurations**

| Conf No.[1] | SPMF | CORE PLL | CEPMF | CEPDF | Input Clock Freq (MHz) | CSB Freq (MHz) | Core Freq (MHz) | QUICC Engine Freq (MHz) | 400 (MHz) | 533 (MHz) | 667 (MHz) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **33 MHz CLKIN/PCI_SYNC_IN Options** | | | | | | | | | | | |
| **s1** | **0100** | **0000100** | æ | æ | 33 | 133 | 266 | — | ∞ | ∞ | ∞ |
| **s2** | **0100** | **0000101** | æ | æ | 33 | 133 | 333 | — | ∞ | ∞ | ∞ |
| **s3** | **0101** | **0000100** | æ | æ | 33 | 166 | 333 | — | ∞ | ∞ | ∞ |
| **s4** | **0101** | **0000101** | æ | æ | 33 | 166 | 416 | — | — | ∞ | ∞ |
| **s5** | **0110** | **0000100** | æ | æ | 33 | 200 | 400 | — | ∞ | ∞ | ∞ |
| **s6** | **0110** | **0000110** | æ | æ | 33 | 200 | 600 | — | — | — | ∞ |
| **s7** | **0111** | **0000011** | æ | æ | 33 | 233 | 350 | — | ∞ | ∞ | ∞ |
| **s8** | **0111** | **0000100** | æ | æ | 33 | 233 | 466 | — | — | ∞ | ∞ |
| **s9** | **0111** | **0000101** | æ | æ | 33 | 233 | 583 | — | — | — | ∞ |
| **s10** | **1000** | **0000011** | æ | æ | 33 | 266 | 400 | — | ∞ | ∞ | ∞ |
| **s11** | **1000** | **0000100** | æ | æ | 33 | 266 | 533 | — | — | ∞ | ∞ |
| **s12** | **1000** | **0000101** | æ | æ | 33 | 266 | 667 | — | — | — | ∞ |
| **s13** | **1001** | **0000010** | æ | æ | 33 | 300 | 300 | — | ∞ | ∞ | ∞ |
| **s14** | **1001** | **0000011** | æ | æ | 33 | 300 | 450 | — | — | ∞ | ∞ |
| **s15** | **1001** | **0000100** | æ | æ | 33 | 300 | 600 | — | — | — | ∞ |
| **s16** | **1010** | **0000010** | æ | æ | 33 | 333 | 333 | — | ∞ | ∞ | ∞ |
| **s17** | **1010** | **0000011** | æ | æ | 33 | 333 | 500 | — | — | ∞ | ∞ |
| **s18** | **1010** | **0000100** | æ | æ | 33 | 333 | 667 | — | — | — | ∞ |
| **c1** | æ | æ | **01001** | **0** | 33 | — | — | 300 | ∞ | ∞ | ∞ |
| **c2** | æ | æ | **01100** | **0** | 33 | — | — | 400 | ∞ | ∞ | ∞ |
| **c3** | æ | æ | **01110** | **0** | 33 | — | — | 466 | — | ∞ | ∞ |
| **c4** | æ | æ | **01111** | **0** | 33 | — | — | 500 | — | ∞ | ∞ |

**Table 76. Suggested PLL Configurations (continued)**

| Conf No.[1] | SPMF | CORE PLL | CEPMF | CEPDF | Input Clock Freq (MHz) | CSB Freq (MHz) | Core Freq (MHz) | QUICC Engine Freq (MHz) | 400 (MHz) | 533 (MHz) | 667 (MHz) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **c5** | æ | æ | **10000** | **0** | 33 | — | — | 533 | — | ∞ | ∞ |
| **c6** | æ | æ | **10001** | **0** | 33 | — | — | 566 | — | — | ∞ |
| **66 MHz CLKIN/PCI_SYNC_IN Options** | | | | | | | | | | | |
| **s1h** | **0011** | **0000110** | æ | æ | 66 | 200 | 400 | — | ∞ | ∞ | ∞ |
| **s2h** | **0011** | **0000101** | æ | æ | 66 | 200 | 500 | — | — | ∞ | ∞ |
| **s3h** | **0011** | **0000110** | æ | æ | 66 | 200 | 600 | — | — | — | ∞ |
| **s4h** | **0100** | **0000011** | æ | æ | 66 | 266 | 400 | — | ∞ | ∞ | ∞ |
| **s5h** | **0100** | **0000100** | æ | æ | 66 | 266 | 533 | — | — | ∞ | ∞ |
| **s6h** | **0100** | **0000101** | æ | æ | 66 | 266 | 667 | — | — | — | ∞ |
| **s7h** | **0101** | **0000010** | æ | æ | 66 | 333 | 333 | — | ∞ | ∞ | ∞ |
| **s8h** | **0101** | **0000011** | æ | æ | 66 | 333 | 500 | — | — | ∞ | ∞ |
| **s9h** | **0101** | **0000100** | æ | æ | 66 | 333 | 667 | — | — | — | ∞ |
| **c1h** | æ | æ | **00101** | **0** | 66 | — | — | 333 | ∞ | ∞ | ∞ |
| **c2h** | æ | æ | **00110** | **0** | 66 | — | — | 400 | ∞ | ∞ | ∞ |
| **c3h** | æ | æ | **00111** | **0** | 66 | — | — | 466 | — | ∞ | ∞ |
| **c4h** | æ | æ | **01000** | **0** | 66 | — | — | 533 | — | ∞ | ∞ |
| **c5h** | æ | æ | **01001** | **0** | 66 | — | — | 600 | — | — | ∞ |

**Note:**

1. The Conf No. consist of prefix, an index and a postfix. The prefix “s” and “c” stands for “syset” and “ce” respectively. The postfix “h” stands for “high input clock.”"The index is a serial number.

The following steps describe how to use above table. See Example 1.

2. Choose the up or down sections in the table according to input clock rate 33 MHz or 66 MHz.
3. Select a suitable CSB and core clock rates from Table 76. Copy the SPMF and CORE PLL configuration bits.
4. Select a suitable QUICC Engine block clock rate from Table 76. Copy the CEPMF and CEPDF configuration bits.
5. Insert the chosen SPMF, COREPLL, CEPMF and CEPDF to the RCWL fields, respectively.

**Example 1. Sample Table Use**

| Index | SPMF | CORE PLL | CEPMF | CEPDF | Input Clock (MHz) | CSB Freq (MHz) | Core Freq (MHz) | QUICC Engine Freq (MHz) | 400 (MHz) | 533 (MHz) | 667 (MHz) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | **1000** | **0000011** | **01001** | **0** | 33 | 266 | 400 | 300 | ∞ | ∞ | ∞ |
| **B** | **0100** | **0000100** | **00110** | **0** | 66 | 266 | 533 | 400 | ∞ | ∞ | ∞ |

- **Example A.** To configure the device with CSB clock rate of 266 MHz, core rate of 400 MHz, and QUICC Engine clock rate 300 MHz while the input clock rate is 33 MHz. Conf No. ‘s10’ and ‘c1’ are selected from Table 76. SPMF is 1000, CORPLL is 0000011, CEPMF is 01001, and CEPDF is 0.
- **Example B.** To configure the device with CSBCSB clock rate of 266 MHz, core rate of 533 MHz and QUICC Engine clock rate 400 MHz while the input clock rate is 66 MHz. Conf No. ‘s5h’ and ‘c2h’ are selected from Table 76. SPMF is 0100, CORPLL is 0000100, CEPMF is 00110, and CEPDF is 0.

# 22 Thermal

This section describes the thermal specifications of the MPC8360E/58E.

## 22.1 Thermal Characteristics

This table provides the package thermal characteristics for the 37.5 mm × 37.5 mm 740-TBGA package.

**Table 77. Package Thermal Characteristics for the TBGA Package**

| Characteristic | Symbol | Value | Unit | Notes |
|---|---|---|---|---|
| Junction-to-ambient natural convection on single-layer board (1s) | $R_{\theta JA}$ | 15 | °C/W | 1, 2 |
| Junction-to-ambient natural convection on four-layer board (2s2p) | $R_{\theta JA}$ | 11 | °C/W | 1, 3 |
| Junction-to-ambient (@1 m/s) on single-layer board (1s) | $R_{\theta JMA}$ | 10 | °C/W | 1, 3 |
| Junction-to-ambient (@ 1 m/s) on four-layer board (2s2p) | $R_{\theta JMA}$ | 8 | °C/W | 1, 3 |
| Junction-to-ambient (@ 2 m/s) on single-layer board (1s) | $R_{\theta JMA}$ | 9 | °C/W | 1, 3 |
| Junction-to-ambient (@ 2 m/s) on four-layer board (2s2p) | $R_{\theta JMA}$ | 7 | °C/W | 1, 3 |
| Junction-to-board thermal | $R_{\theta JB}$ | 4.5 | °C/W | 4 |
| Junction-to-case thermal | $R_{\theta JC}$ | 1.1 | °C/W | 5 |

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$T_J$ = junction temperature (° C)
$T_B$ = board temperature at the package perimeter (° C)
$R_{\theta JA}$ = junction to board thermal resistance (° C/W) per JESD51-8
$P_D$ = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

### 22.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter ($\Psi_{JT}$) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$T_J$ = junction temperature (° C)
$T_T$ = thermocouple temperature on top of package (° C)
$\Psi_{JT}$ = junction-to-ambient thermal resistance (° C/W)
$P_D$ = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

### 22.2.4 Heat Sinks and Junction-to-Ambient Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (° C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (° C/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (° C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

This table shows heat sinks and junction-to-ambient thermal resistance for TBGA package.

**Table 78. Heat Sinks and Junction-to-Ambient Thermal Resistance of TBGA Package**

| Heat Sink Assuming Thermal Grease | Airflow | 35 × 35 mm TBGA |
|---|---|---|
| | | Junction-to-Ambient Thermal Resistance |
| AAVID 30 × 30 × 9.4 mm pin fin | Natural convention | 10.7 |
| AAVID 30 × 30 × 9.4 mm pin fin | 1 m/s | 6.2 |
| AAVID 30 × 30 × 9.4 mm pin fin | 2 m/s | 5.3 |
| AAVID 31 × 35 × 23 mm pin fin | Natural convention | 8.1 |
| AAVID 31 × 35 × 23 mm pin fin | 1 m/s | 4.4 |
| AAVID 31 × 35 × 23 mm pin fin | 2 m/s | 3.7 |
| Wakefield, 53 × 53 × 25 mm pin fin | Natural convention | 5.4 |
| Wakefield, 53 × 53 × 25 mm pin fin | 1 m/s | 3.2 |
| Wakefield, 53 × 53 × 25 mm pin fin | 2 m/s | 2.4 |
| MEI, 75 × 85 × 12 no adjacent board, extrusion | Natural convention | 6.4 |
| MEI, 75 × 85 × 12 no adjacent board, extrusion | 1 m/s | 3.8 |
| MEI, 75 × 85 × 12 no adjacent board, extrusion | 2 m/s | 2.5 |
| MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass | 1 m/s | 2.8 |

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

**Table 81. SVR Settings (continued)**

| Device | Package | SVR (Rev. 2.0) | SVR (Rev. 2.1) |
|---|---|---|---|
| MPC8358E | TBGA | 0x804A_0020 | 0x804A_0021 |
| MPC8358 | TBGA | 0x804B_0020 | 0x804B_0021 |

# 25 Document Revision History

This table provides a revision history for this document.

**Table 82. Revision History**

| Rev. Number | Date | Substantive Change(s) |
|---|---|---|
| 5 | 09/2011 | • Section 2.2.1, “Power-Up Sequencing”, added the current limitation “3A to 5A” for the excessive current.<br>• Section 2.1.2, “Power Supply Voltage Specification, Updated the Characteristic for TBGA (MPC8358 & MPC8360 Device) with specific frequency for Core and PLL voltages.<br>• Added table footnote 3 to Table 2.<br>• Applied table footnotes 1 and 2 to Table 10.<br>• Removed table footnotes from Table 19.<br>• Applied table footnote 8 to the last row of Table 40.<br>• Applied table footnotes 8 and 9 to Table 41.<br>• Applied table footnotes 2and 3 to Table 45.<br>• Removed table footnotes from Table 46.<br>• Applied table footnote to last three rows of Table 65. |
| 4 | 01/2011 | • Updated references to the LCRR register throughout<br>• Removed references to DDR DLL mode in Section 6.2.2, “DDR and DDR2 SDRAM Output AC Timing Specifications.”<br>• Changed “Junction-to-Case” to “Junction-to-Ambient” in Section 22.2.4, “Heat Sinks and Junction-to-Ambient Thermal Resistance,” and Table 78, “Heat Sinks and Junction-to-Ambient Thermal Resistance of TBGA Package,” titles. |