NXP USA Inc. - KMPC8360EVVAHFH Datasheet





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Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8360evvahfh

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Power Sequencing

This figure shows the undershoot and overshoot voltage of the PCI interface of the device for the 3.3-V signals, respectively.



Figure 4. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	OV _{DD} = 3.3 V
PCI signals	25	
PCI output clocks (including PCI_SYNC_OUT)	42	
DDR signal	20 36 (half-strength mode) ¹	GV _{DD} = 2.5 V
DDR2 signal	18 36 (half-strength mode) ¹	GV _{DD} = 1.8 V
10/100/1000 Ethernet signals	42	LV _{DD} = 2.5/3.3 V
DUART, system control, I ² C, SPI, JTAG	42	OV _{DD} = 3.3 V
GPIO signals	42	OV _{DD} = 3.3 V LV _{DD} = 2.5/3.3 V

Note:

1. DDR output impedance values for half strength mode are verified by design and not tested.

2.2 Power Sequencing

This section details the power sequencing considerations for the MPC8360E/58E.



Power Sequencing

2.2.1 Power-Up Sequencing

MPC8360E/58E does not require the core supply voltage (V_{DD} and AV_{DD}) and I/O supply voltages (GV_{DD} , LV_{DD} , and OV_{DD}) to be applied in any particular order. During the power ramp up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there may be a period of time that all input and output pins are actively be driven and cause contention and excessive current from 3A to 5A. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD} , LV_{DD} , and OV_{DD}) and assert PORESET before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V, see this figure.



Figure 5. Power Sequencing Example

I/O voltage supplies (GV_{DD}, LV_{DD}, and OV_{DD}) do not have any ordering requirements with respect to one another.

2.2.2 Power-Down Sequencing

The MPC8360E/58E does not require the core supply voltage and I/O supply voltages to be powered down in any particular order.

3 Power Characteristics

The estimated typical power dissipation values are shown in these tables.

Table 4. MPC8360E TBGA	Core Power	Dissipation ¹
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Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	500	5.0	5.6	W	2, 3, 5
400	266	400	4.5	5.0	W	2, 3, 4
533	266	400	4.8	5.3	W	2, 3, 4
667	333	400	5.8	6.3	W	3, 6, 7, 8
500	333	500	5.9	6.4	W	3, 6, 7, 8



6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the device when $GV_{DD}(typ) = 1.8 \text{ V}.$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV _{DD}	1.71	1.89	V	1
I/O reference voltage	MV _{REF}	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.125	GV _{DD} + 0.3	V	_
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.125	V	_
Output leakage current	I _{OZ}	_	±10	μA	4
Output high current (V _{OUT} = 1.420 V)	I _{OH}	-13.4	—	mA	
Output low current (V _{OUT} = 0.280 V)	I _{OL}	13.4	—	mA	
MV _{REF} input leakage current	I _{VREF}	_	±10	μA	
Input current (0 V ≰⁄ _{IN} ≤OV _{DD})	I _{IN}	—	±10	μA	_

Table 14. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.

 MV_{REF} is expected to equal 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} cannot exceed ±2% of the DC value.

 V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to equal MV_{REF}. This rail should track variations in the DC level of MV_{REF}.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

This table provides the DDR2 capacitance when $GV_{DD}(typ) = 1.8$ V.

Table 15. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) of the device when $GV_{DD}(typ) = 2.5 \text{ V}.$

Table 16. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	GV _{DD}	2.375	2.625	V	1
I/O reference voltage	MV _{REF}	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} - 0.04	MV _{REF} + 0.04	V	3



DDR and DDR2 SDRAM AC Electrical Characteristics

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 21 and Table 22 provide the output AC timing specifications and measurement conditions for the DDR and DDR2 SDRAM interface.

Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter ⁸	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time, (MCK[n]/MCK[n] crossing)	t _{MCK}	6	10	ns	2
Skew between any MCK to ADDR/CMD 333 MHz 266 MHz 200 MHz	t _{AOSKEW}	-1.0 -1.1 -1.2	0.2 0.3 0.4	ns	3
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz 200 MHz	^t DDKHAS	2.1 2.8 3.5	_	ns	4
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz—DDR1 266 MHz—DDR2 200 MHz	t _{DDKHAX}	2.0 2.7 2.8 3.5		ns	4
MCS(n) output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t _{DDKHCS}	2.1 2.8 3.5	_	ns	4
MCS(n) output hold with respect to MCK 333 MHz 266 MHz 200 MHz	t _{DDKHCX}	2.0 2.7 3.5	_	ns	4
MCK to MDQS	t _{DDKHMH}	-0.8	0.7	ns	5, 9
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	t _{DDKHDS} , t _{DDKLDS}	0.7 1.0 1.2	_	ns	6
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	t _{DDKHDX} , t _{DDKLDX}	0.7 1.0 1.2	_	ns	6
MDQS preamble start	t _{DDKHMP}	$-0.5\timest_{MCK}-0.6$	$-0.5\timest_{\text{MCK}}\text{+}0.6$	ns	7



DDR and DDR2 SDRAM AC Electrical Characteristics

This figure provides the AC test load for the DDR bus.



Figure 8. DDR AC Test Load

Table 22. DDR and DDR2 SDRAM Measurement Conditions

Symbol	DDR	DDR2	Unit	Notes
V _{TH}	MV _{REF} ± 0.31 V	MV _{REF} ± 0.25 V	V	1
V _{OUT}	$0.5 \times \text{ GV}_{\text{DD}}$	$0.5 \times \text{ GV}_{\text{DD}}$	V	2

Notes:

1. Data input threshold measurement point.

2. Data output measurement point.

This figure shows the DDR SDRAM output timing diagram for source synchronous mode.



Figure 9. DDR SDRAM Output Timing Diagram for Source Synchronous Mode



8.2.4.1 TBI Transmit AC Timing Specifications

This table provides the TBI transmit AC timing specifications.

Table 33. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
GTX_CLK clock period	t _{TTX}	_	8.0	_	ns	—
GTX_CLK duty cycle	t _{TTXH} /t _{TTX}	40	—	60	%	—
GTX_CLK to TBI data TCG[9:0] delay	t _{TTKHDX} t _{TTKHDV}	1.0	—	 5.0	ns	3
GTX_CLK clock rise time, (20% to 80%)	t _{TTXR}	_	—	1.0	ns	—
GTX_CLK clock fall time, (80% to 20%)	t _{TTXF}	_	_	1.0	ns	—
GTX_CLK125 reference clock period	t _{G125}	_	8.0	_	ns	2
GTX_CLK125 reference clock duty cycle	t _{G125H} /t _{G125}	45	—	55	ns	—

Notes:

- The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 2. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
- 3. In rev. 2.0 silicon, due to errata, t_{TTKHDX} minimum is 0.7 ns for UCC1. Refer to Errata QE_ENET19 in Chip Errata for the MPC8360E, Rev. 1.

This figure shows the TBI transmit AC timing diagram.



Figure 18. TBI Transmit AC Timing Diagram



GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

8.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

Table 34. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
PMA_RX_CLK clock period	t _{TRX}	_	16.0	_	ns	—
PMA_RX_CLK skew	t _{SKTRX}	7.5	_	8.5	ns	—
RX_CLK duty cycle	t _{TRXH} /t _{TRX}	40	_	60	%	—
RCG[9:0] setup time to rising PMA_RX_CLK	t _{TRDVKH}	2.5	—		ns	2
RCG[9:0] hold time to rising PMA_RX_CLK	t _{trdxkh}	1.0	_	_	ns	2
RX_CLK clock rise time, $V_{IL}(min)$ to $V_{IH}(max)$	t _{TRXR}	0.7	_	2.4	ns	—
RX_CLK clock fall time, $V_{IH}(max)$ to $V_{IL}(min)$	t _{TRXF}	0.7	_	2.4	ns	—

Notes:

- 1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).}
- 2. Setup and hold time of even numbered RCG are measured from riding edge of PMA_RX_CLK1. Setup and hold time of odd numbered RCG are measured from riding edge of PMA_RX_CLK0.

This figure shows the TBI receive AC timing diagram.



Figure 19. TBI Receive AC Timing Diagram



8.2.5 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 35. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
Data to clock output skew (at transmitter)	t _{SKRGTKHDX} t _{SKRGTKHDV}	-0.5 		— 0.5	ns	7
Data to clock input skew (at receiver)	t _{SKRGDXKH} t _{SKRGDVKH}	1.0		 2.6	ns	2
Clock cycle duration	t _{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	t _{RGTH} /t _{RGT}	45	50	55	%	4, 5
Duty cycle for 10BASE-T and 100BASE-TX	t _{RGTH} /t _{RGT}	40	50	60	%	3, 5
Rise time (20–80%)	t _{RGTR}	—		0.75	ns	
Fall time (20–80%)	t _{RGTF}	—	_	0.75	ns	
GTX_CLK125 reference clock period	t _{G125}	—	8.0	_	ns	6
GTX_CLK125 reference clock duty cycle	t _{G125H} /t _{G125}	47		53	%	

Notes:

- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (Rx) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- 2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns can be added to the associated clock signal.
- 3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
- 4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- 5. Duty cycle reference is LV_{DD}/2.
- 6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
- 7. In rev. 2.0 silicon, due to errata, t_{SKRGTKHDX} minimum is –2.3 ns and t_{SKRGTKHDV} maximum is 1 ns for UCC1, 1.2 ns for UCC2 option 1, and 1.8 ns for UCC2 option 2. In rev. 2.1 silicon, due to errata, t_{SKRGTKHDX} minimum is –0.65 ns for UCC2 option 1 and –0.9 for UCC2 option 2, and t_{SKRGTKHDV} maximum is 0.75 ns for UCC1 and UCC2 option 1 and 0.85 for UCC2 option 2. Refer to Errata QE_ENET10 in *Chip Errata for the MPC8360E, Rev. 1*. UCC1 does meet t_{SKRGTKHDX} minimum for rev. 2.1 silicon.



Parameter	Symbol ¹	Min	Max	Unit	Notes
LUPWAIT input hold from local bus clock	t _{LBIXKH2}	1.0	_	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT1}	1.5	_	ns	5
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT2}	3.0	_	ns	6
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT3}	2.5	_	ns	7
Local bus clock to LALE rise	t _{LBKHLR}	_	4.5	ns	
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}	_	4.5	ns	
Local bus clock to data valid for LAD/LDP	t _{LBKHOV2}	_	4.5	ns	3
Local bus clock to address valid for LAD	t _{LBKHOV3}	_	4.5	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	1.0	_	ns	3
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	1.0	_	ns	3
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ}		3.8	ns	8

Table 40. Local Bus General Timing Parameters—DLL Enabled (continued)

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the output (O) going invalid (X) or output hold time.
 </sub>
- 2. All timings are in reference to rising edge of LSYNC_IN.
- 3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. t_{LBOTOT1} should be used when RCWH[LALE] is not set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- t_{LBOTOT2} should be used when RCWH[LALE] is set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- 7. t_{LBOTOT3} should be used when RCWH[LALE] is set and when the load on LALE output pin equals to the load on LAD output pins.
- 8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This table describes the general timing parameters of the local bus interface of the device.

Table 41. Local Bus General Timing Parameters—DLL Bypass Mode⁹

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	15	—	ns	2
Input setup to local bus clock	t _{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock	t _{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT1}	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT2}	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT3}	2.5	—	ns	7



Local Bus AC Electrical Specifications



Figure 25. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Enabled)





JTAG DC Electrical Characteristics



Figure 28. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (DLL Enabled)

10 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8360E/58E.

10.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface of the device.

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	—	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V
Input high voltage	V _{IH}	—	2.5	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	$0 V \leq V_{IN} \leq OV_{DD}$	_	±10	μA



I2C AC Electrical Specifications

11.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interface of the device.

Table 45. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 44).

Parameter	Symbol ¹	Min	Max	Unit	Note
SCL clock frequency	f _{I2C}	0	400	kHz	2
Low period of the SCL clock	t _{I2CL}	1.3	_	μs	—
High period of the SCL clock	t _{I2CH}	0.6	_	μs	—
Setup time for a repeated START condition	t _{I2SVKH}	0.6	_	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL}	0.6	_	μs	_
Data setup time	t _{I2DVKH}	100	_	ns	3
Data hold time: CBUS compatible masters I ² C bus devices	t _{I2DXKL}	$\frac{1}{0^2}$	 0.9 ³	μs	—
Rise time of both SDA and SCL signals	t _{I2CR}	20 + 0.1 C _b ⁴	300	ns	—
Fall time of both SDA and SCL signals	t _{I2CF}	20 + 0.1 C _b ⁴	300	ns	—
Set-up time for STOP condition	t _{l2PVKH}	0.6	_	μs	—
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	_	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times \text{OV}_{\text{DD}}$	_	V	_
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times \text{OV}_{\text{DD}}$	_	V	_

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional}

block)(signal)(state)(reference)(state) for inputs and t_{(first} two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

 The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of the falling edge of SCL.

3. The maximum t_{12DVKH} has only to be met if the device does not stretch the LOW period (t_{12CL}) of the SCL signal.

4. C_B = capacitance of one bus line in pF.



This figure shows the PCI input AC timing conditions.



Figure 37. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.



13 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8360E/58E.

13.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the device timer pins, including TIN, TOUT, TGATE, and RTC_CLK.

Table 49. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	_	V
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	$0 V \leq V_{IN} \leq OV_{DD}$	_	±10	μA



Timers AC Timing Specifications

13.2 Timers AC Timing Specifications

This table provides the timer input and output AC timing specifications.

Table 50. Timers Input AC Timing Specifications¹

Characteristic	Symbol ²	Тур	Unit
Timers inputs—minimum pulse width	t _{TIWID}	20	ns

Notes:

- 1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
- 2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

This figure provides the AC test load for the timers.



Figure 39. Timers AC Test Load

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8360E/58E.

14.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the device GPIO.

Table 51. GPIO DC Electrical Charac

Characteristic	Symbol	Condition	Min	Мах	Unit	Notes
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	—	V	1
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V	1
Input low voltage	V _{IL}	—	-0.3	0.8	V	—
Input current	I _{IN}	$0 \ V \leq V_{IN} \leq OV_{DD}$	—	±10	μA	—

Note:

1. This specification applies when operating from 3.3-V supply.

Table 60. UTOPIA AC Timing Specifications¹ (continued)

Characteristic	Symbol ²	Min	Мах	Unit	Notes
UTOPIA inputs—Internal clock input hold time	t _{UIIXKH}	2.4	—	ns	
UTOPIA inputs—External clock input hold time	t _{UEIXKH}	1	—	ns	3

Notes:

- 1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{UIKHOX} symbolizes the UTOPIA outputs internal timing (UI) for the time t_{UTOPIA} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
 </sub>
- In rev. 2.0 silicon, due to errata, t_{UEIVKH} minimum is 4.3 ns and t_{UEIXKH} minimum is 1.4 ns under specific conditions. Refer to Errata QE_UPC3 in *Chip Errata for the MPC8360E, Rev. 1.*

This figure provides the AC test load for the UTOPIA.



Figure 46. UTOPIA AC Test Load

These figures represent the AC timing from Table 56. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the UTOPIA timing with external clock.



Figure 47. UTOPIA AC Timing (External Clock) Diagram



USB DC Electrical Characteristics

19 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8360E/58E.

19.1 USB DC Electrical Characteristics

This table provides the DC electrical characteristics for the USB interface.

Table 64. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
High-level output voltage, $I_{OH} = -100 \ \mu A$	V _{OH}	OV _{DD} - 0.4	—	V
Low-level output voltage, I _{OL} = 100 μA	V _{OL}	—	0.2	V
Input current	I _{IN}	—	±10	μA

19.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface of the device.

Table 65. USB General Timing Parameters

Parameter	Symbol ¹	Min	Max	Unit	Notes	Note
USB clock cycle time	t _{USCK}	20.83		ns	Full speed 48 MHz	_
USB clock cycle time	t _{USCK}	166.67		ns	Low speed 6 MHz	_
Skew between TXP and TXN	t _{USTSPN}	_	5	ns	—	2
Skew among RXP, RXN, and RXD	t _{USRSPND}	_	10	ns	Full speed transitions	2
Skew among RXP, RXN, and RXD	t _{USRPND}	_	100	ns	Low speed transitions	2

Notes:

The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(state)(signal)} for receive signals and t_{(first two letters of functional block)(state)(signal)} for transmit signals. For example, t_{USRSPND} symbolizes USB timing (US) for the USB receive signals skew (RS) among RXP, RXN, and RXD (PND). Also, t_{USTSPN} symbolizes USB timing (US) for the USB transmit signals skew (TS) between TXP and TXN (PN).

2. Skew measurements are done at $OV_{DD}/2$ of the rising or falling edge of the signals.

This figure provide the AC test load for the USB.



Figure 52. USB AC Test Load



20 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8360E/58E is available in a tape ball grid array (TBGA), see Section 20.1, "Package Parameters for the TBGA Package," and Section 20.2, "Mechanical Dimensions of the TBGA Package," for information on the package.

20.1 Package Parameters for the TBGA Package

The package parameters for rev. 2.0 silicon are as provided in the following list. The package type is $37.5 \text{ mm} \times 37.5 \text{ mm}$, 740 tape ball grid array (TBGA).

Package outline	$37.5 \text{ mm} \times 37.5 \text{ mm}$
Interconnects	740
Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder Balls	62 Sn/36 Pb/2 Ag (ZU package)
	95.5 Sn/0.5 Cu/4Ag (VV package)
Ball diameter (typical)	0.64 mm

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PORESET	L37	I	OV _{DD}	—
HRESET	L36	I/O	OV _{DD}	1
SRESET	M33	I/O	OV _{DD}	2
	Thermal Management			
THERM0	AP19	I	GV _{DD}	—
THERM1	AT31	I	GV _{DD}	—
	Power and Ground Signals			
AV _{DD} 1	K35	Power for LBIU DLL (1.2 V)	AV _{DD} 1	_
AV _{DD} 2	К36	Power for CE PLL (1.2 V)	AV _{DD} 2	_
AV _{DD} 5	AM29	Power for e300 PLL (1.2 V)	AV _{DD} 5	—
AV _{DD} 6	К37	Power for system PLL (1.2 V)	AV _{DD} 6	_
GND	A2, A8, A13, A19, A22, A25, A31, A33, A36, B7, B12, B24, B27, B30, C4, C6, C9, C15, C26, C32, D3, D8, D11, D14, D17, D19, D23, D27, E7, E13, E25, E30, E36, F4, F37, G34, H1, H5, H32, H33, J4, J32, J37, K1, L3, L5, L33, L34, M1, M34, M35, N37, P2, P5, P35, P36, R4, T3, U1, U5, U35, V37, W1, W4, W33, W36, Y34, AA3, AA5, AC3, AC32, AC35, AD1, AD37, AE4, AE34, AE36, AF33, AG4, AG6, AG32, AH35, AJ1, AJ4, AJ32, AJ35, AJ37, AK36, AL3, AL34, AM4, AN6, AN23, AN30, AP8, AP12, AP14, AP16, AP17, AP20, AP25, AR6, AR8, AR9, AR19, AR24, AR31, AR35, AR37, AT4, AT10, AT19, AT20, AT25, AU14, AU22, AU28, AU35	_	_	_
GV _{DD}	AD4, AE3, AF1, AF5, AF35, AF37, AG2, AG36, AH33, AH34, AK5, AM1, AM35, AM37, AN2, AN10, AN11, AN12, AN14, AN32, AN36, AP5, AP23, AP28, AR1, AR7, AR10, AR12, AR21, AR25, AR27, AR33, AT15, AT22, AT28, AT33, AU2, AU5, AU16, AU31, AU36	Power for DDR DRAM I/O voltage (2.5 or 1.8 V)	GV _{DD}	
LV _{DD} 0	D5, D6	Power for UCC1 Ethernet interface (2.5 V, 3.3 V)	LV _{DD} 0	



where:

 T_I = junction temperature (° C)

 $T_I = T_B + (R_{\theta IB} \times P_D)$

 T_B = board temperature at the package perimeter (° C)

 $R_{\theta JA}$ = junction to board thermal resistance (° C/W) per JESD51-8

 P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

22.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

 T_J = junction temperature (° C)

 T_T = thermocouple temperature on top of package (° C)

 Ψ_{IT} = junction-to-ambient thermal resistance (° C/W)

 P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

22.2.4 Heat Sinks and Junction-to-Ambient Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

 $R_{\theta JA}$ = junction-to-ambient thermal resistance (° C/W)

 $R_{\theta JC}$ = junction-to-case thermal resistance (° C/W)

 $R_{\theta CA}$ = case-to-ambient thermal resistance (° C/W)

 $R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.



Thermal Management Information

This table shows heat sinks and junction-to-ambient thermal resistance for TBGA package.

Table 78. Heat Sinks and Junction-to-Ambien	t Thermal Resistance of TBGA Package
---	--------------------------------------

		35 imes 35 mm TBGA	
Heat Sink Assuming Thermal Grease	Airflow	Junction-to-Ambient Thermal Resistance	
AAVID 30 × 30 × 9.4 mm pin fin	Natural convention	10.7	
AAVID 30 × 30 × 9.4 mm pin fin	1 m/s	6.2	
AAVID 30 × 30 × 9.4 mm pin fin	2 m/s	5.3	
AAVID 31 × 35 × 23 mm pin fin	Natural convention	8.1	
AAVID 31 × 35 × 23 mm pin fin	1 m/s	4.4	
AAVID 31 × 35 × 23 mm pin fin	2 m/s	3.7	
Wakefield, 53 × 53 × 25 mm pin fin	Natural convention	5.4	
Wakefield, 53 × 53 × 25 mm pin fin	1 m/s	3.2	
Wakefield, 53 × 53 × 25 mm pin fin	2 m/s	2.4	
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural convention	6.4	
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	3.8	
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	2.5	
MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass	1 m/s	2.8	

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following:

Aavid Thermalloy 80 Commercial St.	603-224-9988
Concord, NH 03301	
Internet: www.aavidthermalloy.com	
Alpha Novatech	408-749-7601
473 Sapena Ct. #15	
Santa Clara, CA 95054	
Internet: www.alphanovatech.com	
International Electronic Research Corporation (IERC)	818-842-7277
413 North Moss St.	
Burbank, CA 91502	
Internet: www.ctscorp.com	