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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8360ezuajdga

4.1 DC Electrical Characteristics

This table provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the device.

Table 7. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
CLKIN input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	0 V ≤ V_{IN} ≤ 0.5V or OV_{DD} – 0.5V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	0.5 V ≤ V_{IN} ≤ OV_{DD} – 0.5 V	I_{IN}	—	±100	μA

4.2 AC Electrical Characteristics

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 8. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f_{CLKIN}	—	—	66.67	MHz	1
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	—	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:
1. **Caution:** The system, core, USB, security, and 10/100/1000 Ethernet must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.

4.3 Gigabit Reference Clock Input Timing

This table provides the Gigabit reference clocks (GTX_CLK125) AC timing specifications.

Table 9. GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—

5.3 QUICC Engine Block Operating Frequency Limitations

This section specify the limits of the AC electrical characteristics for the operation of the QUICC Engine block's communication interfaces.

NOTE

The settings listed below are required for correct hardware interface operation. Each protocol by itself requires a minimal QUICC Engine block operating frequency setting for meeting the performance target. Because the performance is a complex function of all the QUICC Engine block settings, the user should make use of the QUICC Engine block performance utility tool provided by Freescale to validate their system.

This table lists the maximal QUICC Engine block I/O frequencies and the minimal QUICC Engine block core frequency for each interface.

Table 13. QUICC Engine Block Operating Frequency Limitations

Interface	Interface Operating Frequency (MHz)	Max Interface Bit Rate (Mbps)	Min QUICC Engine Operating Frequency[1] (MHz)	Notes
Ethernet Management: MDC/MDIO	10 (max)	10	20	—
MII	25 (typ)	100	50	—
RMII	50 (typ)	100	50	—
GMII/RGMII/TBI/RTBI	125 (typ)	1000	250	—
SPI (master/slave)	10 (max)	10	20	—
UCC through TDM	50 (max)	70	8 × F	2
MCC	25 (max)	16.67	16 × F	2, 4
UTOPIA L2	50 (max)	800	2 × F	2
POS-PHY L2	50 (max)	800	2 × F	2
HDLC bus	10 (max)	10	20	—
HDLC/transparent	50 (max)	50	8/3 × F	2, 3
UART/async HDLC	3.68 (max internal ref clock)	115 (Kbps)	20	—
BISYNC	2 (max)	2	20	—
USB	48 (ref clock)	12	96	—

Notes:
1. The QUICC Engine module needs to run at a frequency higher than or equal to what is listed in this table.
2. 'F' is the actual interface operating frequency.\
3. The bit rate limit is independent of the data bus width (that is, the same for serial, nibble, or octal interfaces).
4. TDM in high-speed mode for serial data interface.

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR and DDR2 SDRAM interface of the MPC8360E/58E.

This table provides the input AC timing specifications for the DDR SDRAM interface when GV_{DD}(typ) = 2.5 V.

Table 19. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V	—

Table 20. DDR and DDR2 SDRAM Input AC Timing Specifications Mode

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
MDQS—MDQ/MECC input skew per byte 333 MHz 266 MHz 200 MHz	t_{DISKEW}	 –750 –1125 –1250	 750 1125 1250	ps	1, 2

Notes:
1. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.
2. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 ≤ n ≤ 7) or ECC (MECC[{0...7}] if n = 8).

This figure shows the input timing diagram for the DDR controller.

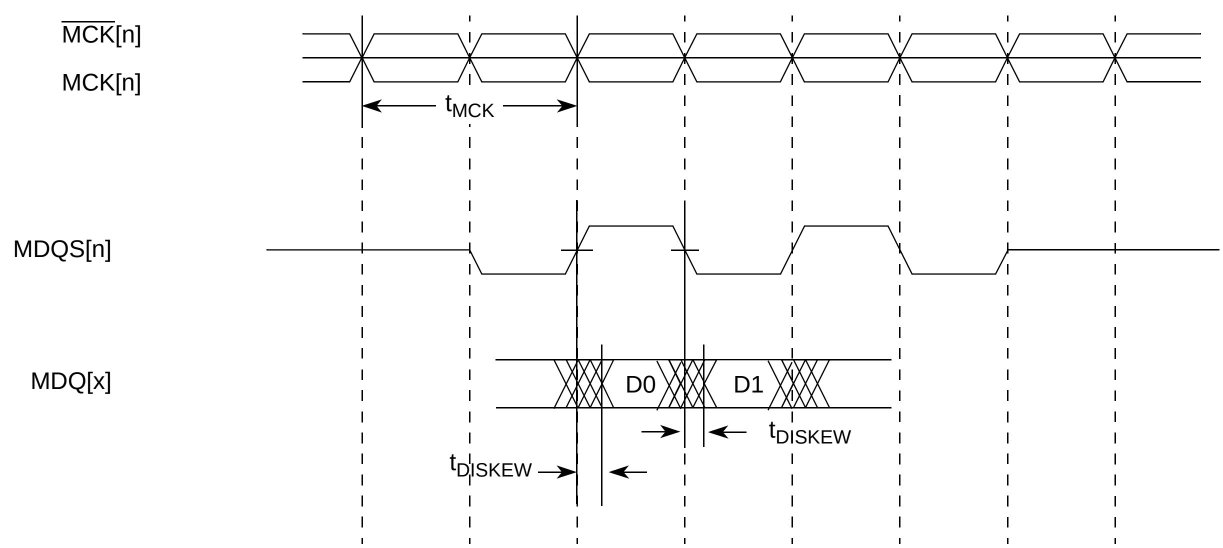

Figure 6. DDR Input Timing Diagram

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8360E/58E.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface of the device.

Table 23. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V	—
Low-level input voltage OV_{DD}	V_{IL}	–0.3	0.8	V	—
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.4	—	V	—
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V	—
Input current (0 V $\leq V_{IN} \leq OV_{DD}$)	I_{IN}	—	±10	µA	1

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface of the device.

Table 24. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	—
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	—	2

Notes:

1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

8 UCC Ethernet Controller: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

8.1 Three-Speed Ethernet Controller (10/100/1000 Mbps)—GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), MII (media independent interface), RMII (reduced media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The MII, RMII, GMII, and TBI interfaces are only defined for 3.3 V, while the RGMII and RTBI interfaces are only defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet

8.2.1.1 GMII Transmit AC Timing Specifications

This table provides the GMII transmit AC timing specifications.

Table 27. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns	—
GTX_CLK duty cycle	$t_{GTXH/tGTX}$	40	—	60	%	—
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX} t_{GTKHDV}	0.5 —	—	— 5.0	ns	3
GTX_CLK clock rise time, (20% to 80%)	t_{GTXR}	—	—	1.0	ns	—
GTX_CLK clock fall time, (80% to 20%)	t_{GTXF}	—	—	1.0	ns	—
GTX_CLK125 clock period	t_{G125}	—	8.0	—	ns	2
GTX_CLK125 reference clock duty cycle measured at $LV_{DD/2}$	t_{G125H}/t_{G125}	45	—	55	%	2

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This symbol is used to represent the external GTX_CLK125 signal and does not follow the original symbol naming convention.
3. In rev. 2.0 silicon, due to errata, t_{GTKHDX} minimum and t_{GTKHDV} maximum are not supported when the GTX_CLK is selected. Refer to Errata *QE_ENET18* in *Chip Errata for the MPC8360E, Rev. 1*.

This figure shows the GMII transmit AC timing diagram.

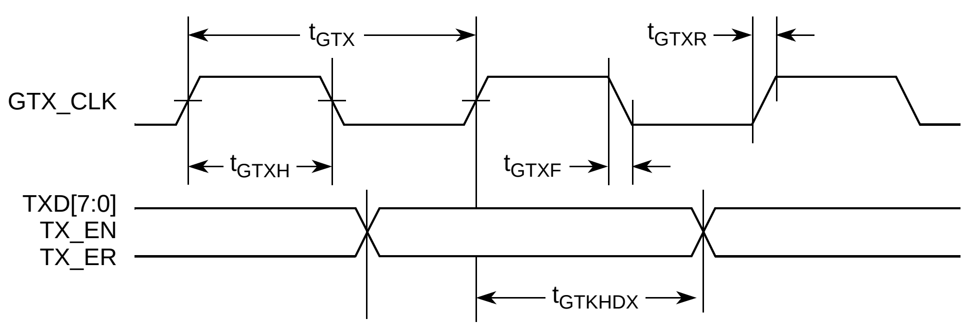

Figure 10. GMII Transmit AC Timing Diagram

8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.2.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 29. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX} t_{MTKHDV}	1 —	5	— 15	ns
TX_CLK data clock rise time, (20% to 80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall time, (80% to 20%)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the MII transmit AC timing diagram.

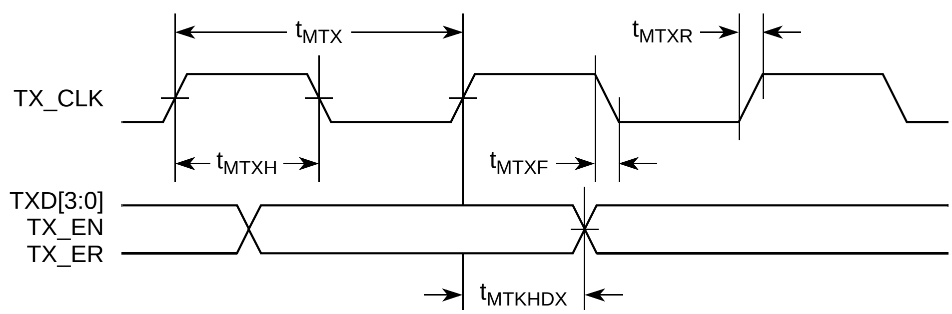

Figure 12. MII Transmit AC Timing Diagram

10.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device.

This table provides the JTAG AC timing specifications as defined in Figure 30 through Figure 33.

Table 43. JTAG AC Timing Specifications (Independent of CLKIN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock duty cycle	t_{JTKHKL}/t_{JTG}	45	55	%	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 22). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

11.2 I^2C AC Electrical Specifications

This table provides the AC timing parameters for the I^2C interface of the device.

Table 45. I^2C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 44).

Parameter	Symbol[1]	Min	Max	Unit	Note
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	µs	—
High period of the SCL clock	t_{I2CH}	0.6	—	µs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	µs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	µs	—
Data setup time	t_{I2DVKH}	100	—	ns	3
Data hold time: CBUS compatible masters I^2C bus devices	t_{I2DXKL}	— 0[2]	— 0.9[3]	µs	—
Rise time of both SDA and SCL signals	t_{I2CR}	$20 + 0.1\ C_b$[4]	300	ns	—
Fall time of both SDA and SCL signals	t_{I2CF}	$20 + 0.1\ C_b$[4]	300	ns	—
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	µs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I^2C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I^2C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I^2C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.

This figure provides the AC test load for the I^2C.

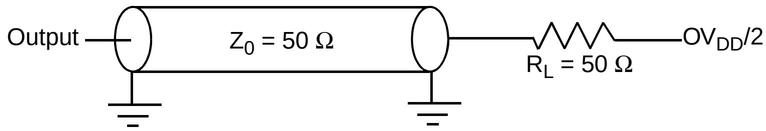

Figure 34. I^2C AC Test Load

This figure shows the AC timing diagram for the I^2C bus.

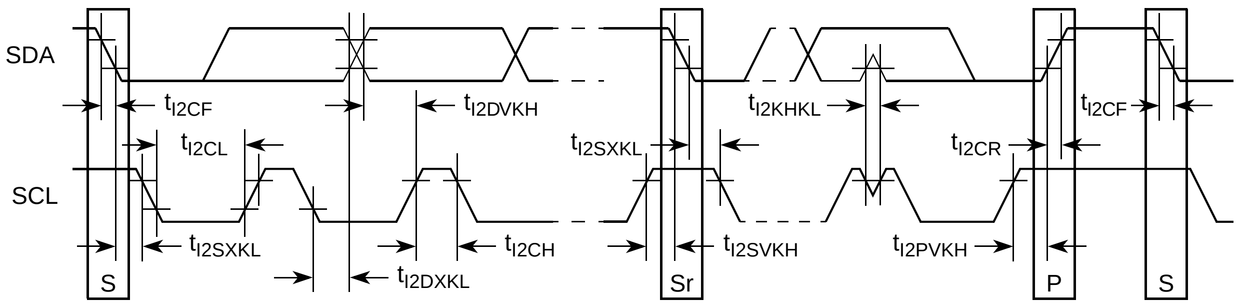

Figure 35. I^2C Bus AC Timing Diagram

12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8360E/58E.

12.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface of the device.

Table 46. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	$0.5 \times OV_{DD}$	$OV_{DD} + 0.5$	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	-0.5	$0.3 \times OV_{DD}$	V
High-level output voltage	V_{OH}	$I_{OH} = –500\ \mu A$	$0.9 \times OV_{DD}$	—	V
Low-level output voltage	V_{OL}	$I_{OL} = 1500\ \mu A$	—	$0.1 \times OV_{DD}$	V
Input current	I_{IN}	$0\ V \leq V_{IN}$[1] $\leq OV_{DD}$	—	±10	μA

12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the device. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. This table provides the PCI AC timing specifications at 66 MHz.

Table 47. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2, 5
Output hold from clock	t_{PCKHOX}	1	—	ns	2

Table 47. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0.3	—	ns	2, 4, 6

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. In rev. 2.0 silicon, due to errata, t_{PCIHOV} maximum is 6.6 ns. Refer to Errata PCI21 in *Chip Errata for the MPC8360E, Rev. 1*.
6. In rev. 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Refer to Errata PCI17 in *Chip Errata for the MPC8360E, Rev. 1*.

Table 48. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	7.0	—	ns	2, 2
Input hold from clock	t_{PCIXKH}	0.3	—	ns	2, 4, 5

Notes:
1. The symbols used for timing specifications herein follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. In rev. 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Refer to Errata PCI17 in *Chip Errata for the MPC8360E, Rev. 1*.

This figure provides the AC test load for PCI.

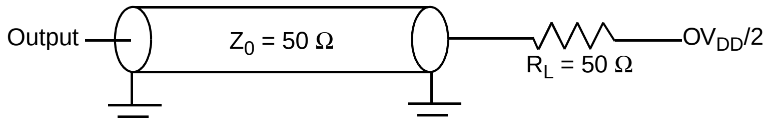

Figure 36. PCI AC Test Load

This figure shows the PCI input AC timing conditions.

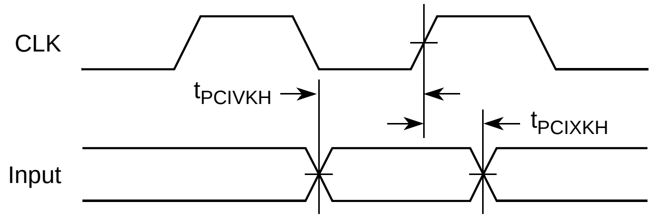

Figure 37. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.

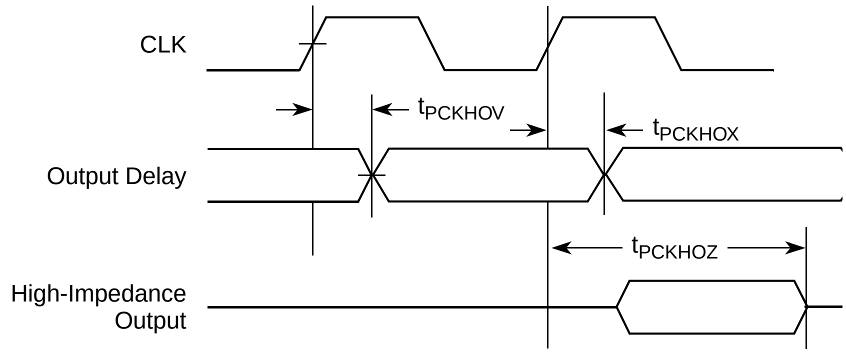

Figure 38. PCI Output AC Timing Measurement Condition

13 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8360E/58E.

13.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the device timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 49. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V $\leq V_{IN} \leq OV_{DD}$	—	±10	μA

13.2 Timers AC Timing Specifications

This table provides the timer input and output AC timing specifications.

Table 50. Timers Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Typ	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

This figure provides the AC test load for the timers.

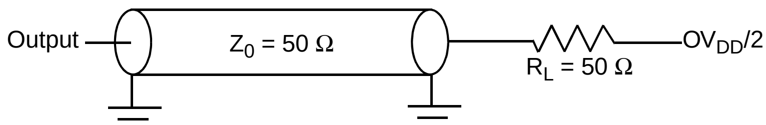

Figure 39. Timers AC Test Load

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8360E/58E.

14.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the device GPIO.

Table 51. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	0 V $\leq V_{IN} \leq OV_{DD}$	—	±10	μA	—

Note:
1. This specification applies when operating from 3.3-V supply.

This figure shows the TDM/SI timing with external clock.

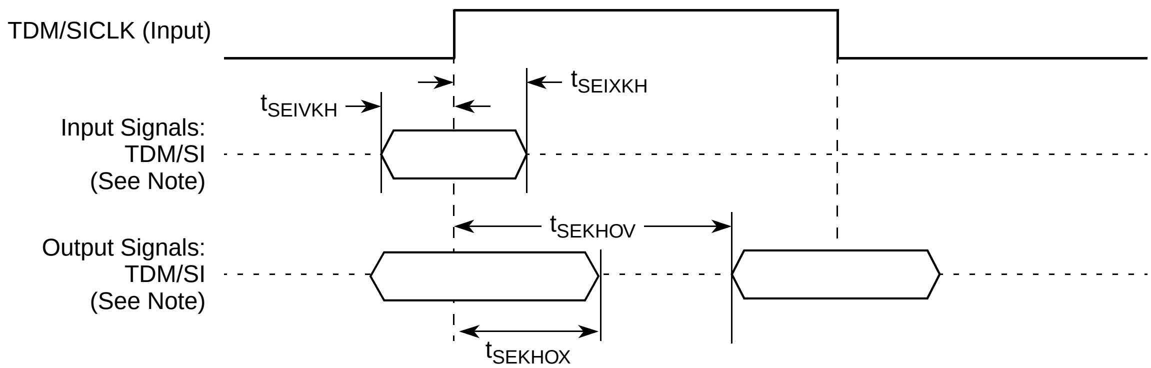

Figure 45. TDM/SI AC Timing (External Clock) Diagram

17.3 UTOPIA/POS

This section describes the DC and AC electrical specifications for the UTOPIA/POS of the MPC8360E/58E.

17.4 UTOPIA/POS DC Electrical Characteristics

This table provides the DC electrical characteristics for the device UTOPIA.

Table 59. UTOPIA DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤V_{IN} ≤OV_{DD}	—	±10	μA

17.5 UTOPIA/POS AC Timing Specifications

This table provides the UTOPIA input and output AC timing specifications.

Table 60. UTOPIA AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit	Notes
UTOPIA outputs—Internal clock delay	t_{UIKHOV}	0	11.5	ns	—
UTOPIA outputs—External clock delay	t_{UEKHOV}	1	11.6	ns	—
UTOPIA outputs—Internal clock high impedance	t_{UIKHOX}	0	8.0	ns	—
UTOPIA outputs—External clock high impedance	t_{UEKHOX}	1	10.0	ns	—
UTOPIA inputs—Internal clock input setup time	t_{UIIVKH}	6	—	ns	—
UTOPIA inputs—External clock input setup time	t_{UEIVKH}	4	—	ns	3

This figure shows the UTOPIA timing with internal clock.

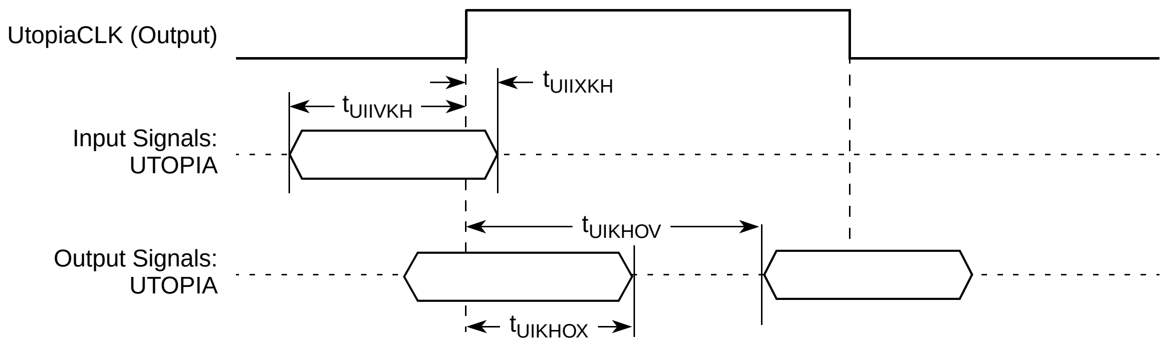

Figure 48. UTOPIA AC Timing (Internal Clock) Diagram

18 HDLC, BISYNC, Transparent, and Synchronous UART

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent, and synchronous UART protocols of the MPC8360E/58E.

18.1 HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

This table provides the DC electrical characteristics for the device HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 61. HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±10	μA

18.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

These tables provide the input and output AC timing specifications for HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 62. HDLC, BISYNC, and Transparent AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	t_{HIKHOV}	0	11.2	ns
Outputs—External clock delay	t_{HEKHOV}	1	10.8	ns

Table 62. HDLC, BISYNC, and Transparent AC Timing Specifications[1] (continued)

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock high impedance	t_{HIKHOX}	-0.5	5.5	ns
Outputs—External clock high impedance	t_{HEKHOX}	1	8	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	8.5	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns
Inputs—Internal clock input hold time	t_{HIIXKH}	1.4	—	ns
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Table 63. Synchronous UART AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	$t_{UAIKHOV}$	0	11.3	ns
Outputs—External clock delay	$t_{UAEKHOV}$	1	14	ns
Outputs—Internal clock high impedance	$t_{UAIKHOX}$	0	11	ns
Outputs—External clock high impedance	$t_{UAEKHOX}$	1	14	ns
Inputs—Internal clock input setup time	$t_{UAIIVKH}$	6	—	ns
Inputs—External clock input setup time	$t_{UAEIVKH}$	8	—	ns
Inputs—Internal clock input hold time	$t_{UAIIXKH}$	1	—	ns
Inputs—External clock input hold time	$t_{UAEIXKH}$	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

This figure provides the AC test load.

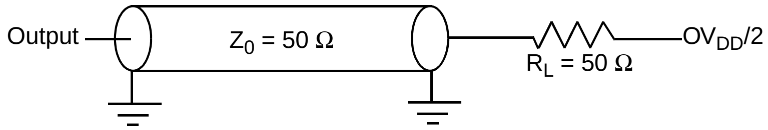

Figure 49. AC Test Load

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
CE_PA[22]	AF3	I/O	OV_{DD}	—
CE_PA[23:26]	C18, D18, E18, A18	I/O	$LV_{DD}1$	—
CE_PA[27:28]	AF2, AE6	I/O	OV_{DD}	—
CE_PA[29]	B19	I/O	$LV_{DD}1$	—
CE_PA[30]	AE5	I/O	OV_{DD}	—
CE_PA[31]	F16	I/O	$LV_{DD}1$	—
CE_PB[0:27]	AE2, AE1, AD5, AD3, AD2, AC6, AC5, AC4, AC2, AC1, AB5, AB4, AB3, AB1, AA6, AA4, AA2, Y6, Y4, Y3, Y2, Y1, W6, W5, W2, V5, V3, V2	I/O	OV_{DD}	—
CE_PC[0:1]	V1, U6	I/O	OV_{DD}	—
CE_PC[2:3]	C16, A15	I/O	$LV_{DD}1$	—
CE_PC[4:6]	U4, U3, T6	I/O	OV_{DD}	—
CE_PC[7]	C19	I/O	$LV_{DD}2$	—
CE_PC[8:9]	A4, C5	I/O	$LV_{DD}0$	—
CE_PC[10:30]	T5, T4, T2, T1, R5, R3, R1, C11, D12, F13, B10, C10, E12, A9, B8, D10, A14, E15, B14, D15, AH2	I/O	OV_{DD}	—
CE_PD[0:27]	E11, D9, C8, F11, A7, E9, C7, A6, F10, B6, D7, E8, B5, A5, C2, E4, F5, B1, D2, G5, D1, E2, H6, F3, E1, F2, G3, H4	I/O	OV_{DD}	—
CE_PE[0:31]	K3, J2, F1, G2, J5, H3, G1, H2, K6, J3, K5, K4, L6, P6, P4, P3, P1, N4, N5, N2, N1, M2, M3, M5, M6, L1, L2, L4, E14, C13, C14, B13	I/O	OV_{DD}	—
CE_PF[0:3]	F14, D13, A12, A11	I/O	OV_{DD}	—
Clocks				
PCI_CLK_OUT[0]/CE_PF[26]	B22	I/O	$LV_{DD}2$	—
PCI_CLK_OUT[1:2]/CE_PF[27:28]	D22, A23	I/O	OV_{DD}	—
CLKIN	E37	I	OV_{DD}	—
PCI_CLOCK/PCI_SYNC_IN	M36	I	OV_{DD}	—
PCI_SYNC_OUT/CE_PF[29]	D37	I/O	OV_{DD}	3
JTAG				
TCK	K33	I	OV_{DD}	—
TDI	K34	I	OV_{DD}	4
TDO	H37	O	OV_{DD}	3
TMS	J36	I	OV_{DD}	4
$\overline{\text{TRST}}$	L32	I	OV_{DD}	4
Test				
TEST	L35	I	OV_{DD}	7
TEST_SEL	AU34	I	GV_{DD}	7

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
CE_PB[0:27]	AE2, AE1, AD5, AD3, AD2, AC6, AC5, AC4, AC2, AC1, AB5, AB4, AB3, AB1, AA6, AA4, AA2, Y6, Y4, Y3, Y2, Y1, W6, W5, W2, V5, V3, V2	I/O	OV_{DD}	—
CE_PC[0:1]	V1, U6	I/O	OV_{DD}	
CE_PC[2:3]	C16, A15	I/O	$LV_{DD}1$	—
CE_PC[4:6]	U4, U3, T6	I/O	OV_{DD}	—
CE_PC[7]	C19	I/O	$LV_{DD}2$	—
CE_PC[8:9]	A4, C5	I/O	$LV_{DD}0$	—
CE_PC[10:30]	T5, T4, T2, T1, R5, R3, R1, C11, D12, F13, B10, C10, E12, A9, B8, D10, A14, E15, B14, D15, AH2	I/O	OV_{DD}	—
CE_PD[0:27]	E11, D9, C8, F11, A7, E9, C7, A6, F10, B6, D7, E8, B5, A5, C2, E4, F5, B1, D2, G5, D1, E2, H6, F3, E1, F2, G3, H4	I/O	OV_{DD}	—
CE_PE[0:31]	K3, J2, F1, G2, J5, H3, G1, H2, K6, J3, K5, K4, L6, P6, P4, P3, P1, N4, N5, N2, N1, M2, M3, M5, M6, L1, L2, L4, E14, C13, C14, B13	I/O	OV_{DD}	—
CE_PF[0:3]	F14, D13, A12, A11	I/O	OV_{DD}	—
Clocks				
PCI_CLK_OUT[0]/CE_PF[26]	B22	I/O	$LV_{DD}2$	—
PCI_CLK_OUT[1:2]/CE_PF[27:28]	D22, A23	I/O	OV_{DD}	—
CLKIN	E37	I	OV_{DD}	—
PCI_CLOCK/PCI_SYNC_IN	M36	I	OV_{DD}	—
PCI_SYNC_OUT/CE_PF[29]	D37	I/O	OV_{DD}	3
JTAG				
TCK	K33	I	OV_{DD}	—
TDI	K34	I	OV_{DD}	4
TDO	H37	O	OV_{DD}	3
TMS	J36	I	OV_{DD}	4
$\overline{\text{TRST}}$	L32	I	OV_{DD}	4
Test				
TEST	L35	I	OV_{DD}	7
$\overline{\text{TEST\_SEL}}$	AU34	I	GV_{DD}	10
PMC				
$\overline{\text{QUIESCE}}$	B36	O	OV_{DD}	—
System Control				

This figure shows the internal distribution of clocks within the MPC8358E.

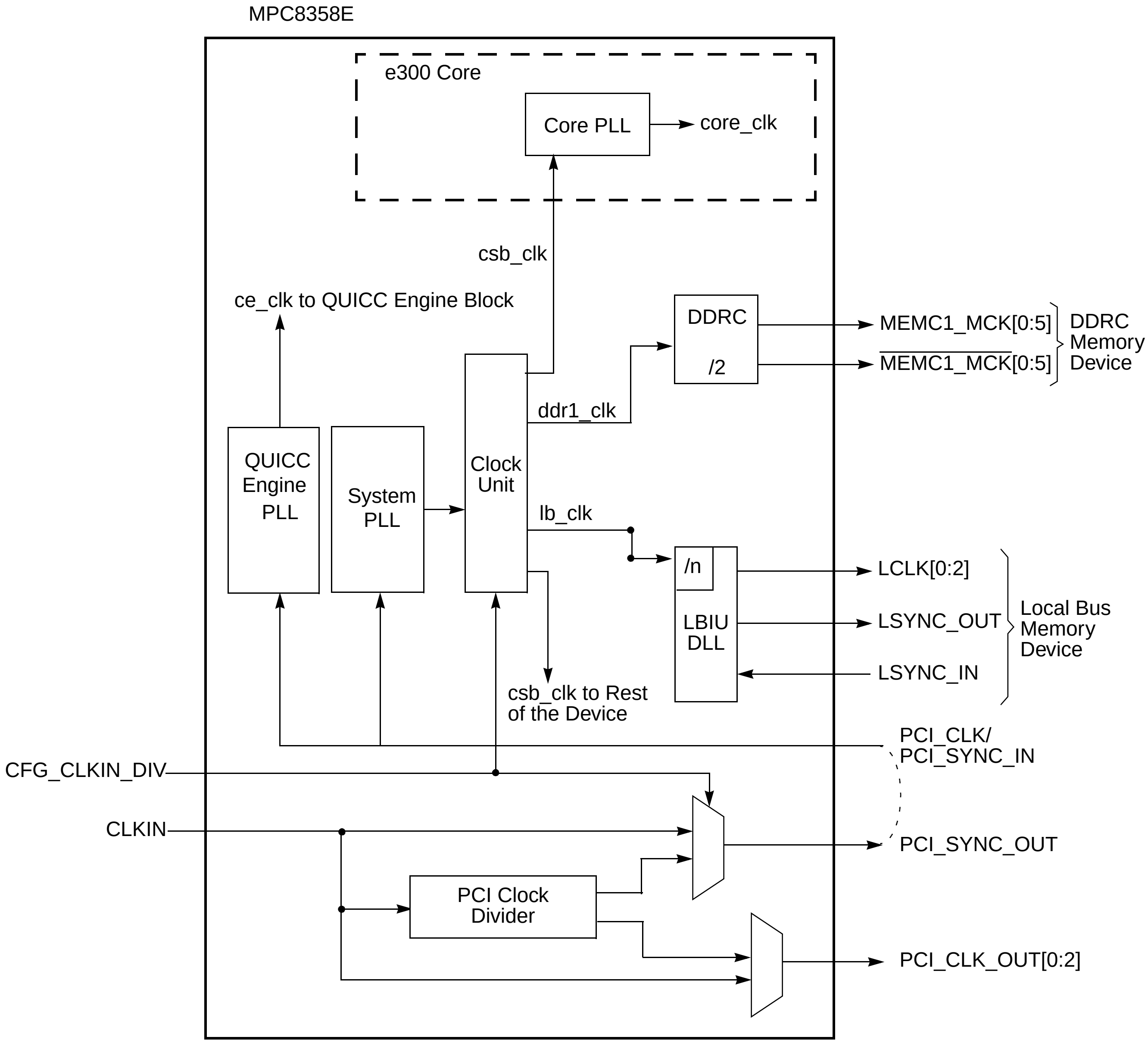

Figure 55. MPC8358E Clock Subsystem

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Note that in PCI host mode, the primary clock input also depends on whether PCI clock outputs are selected with RCWH[PCICKDRV]. When the device is configured as a PCI host device (RCWH[PCIHOST] = 1) and PCI clock output is selected (RCWH[PCICKDRV] = 1), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCIOEN*n*] parameters enable the PCI_CLK_OUT*n*, respectively.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input ordered, see Section 24.1, “Part Numbers Fully Addressed by this Document,” for part ordering details and contact your Freescale sales representative or authorized distributor for more information.

Table 69. Operating Frequencies for the TBGA Package

Characteristic[1]	400 MHz	533 MHz	667 MHz[2]	Unit
e300 core frequency (*core_clk*)	266–400	266–533	266–667	MHz
Coherent system bus frequency (*csb_clk*)	133–333			MHz
QUICC Engine frequency[3] (*ce_clk*)	266–500			MHz
DDR and DDR2 memory bus frequency (MCLK)[4]	100–166.67			MHz
Local bus frequency (LCLK*n*)[5]	16.67–133			MHz
PCI input frequency (CLKIN or PCI_CLK)	25–66.67			MHz
Security core maximum internal operating frequency	133	133	166	MHz

Notes:
1. The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
2. The 667 MHz core frequency is based on a 1.3 V V_{DD} supply voltage.
3. The 500 MHz QE frequency is based on a 1.3 V V_{DD} supply voltage.
4. The DDR data rate is 2x the DDR memory bus frequency.
5. The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWL[LBCM]).

21.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] and RCWL[SVCOD] parameters. This table shows the multiplication factor encodings for the system PLL.

Table 70. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	× 16
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11

23.7 Pull-Up Resistor Requirements

The device requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including I^2C pins, Ethernet Management MDIO pin, and EPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, see *MPC8360E/MPC8358E PowerQUICC Design Checklist* (AN3097).

24 Ordering Information

24.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the MPC8360E/58E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. Additionally to the processor frequency, the part numbering scheme also includes an application modifier, which may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number.

Table 80. Part Numbering Nomenclature[1]

MPC	***nnnn***	***e***	***t***	***pp***	***aa***	***a***	***a***	***A***
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range**	**Package[2]**	**Processor Frequency[3]**	**Platform Frequency**	**QUICC Engine Frequency**	**Die Revision**
MPC	8358	Blank = not included E = included	Blank = 0° C T_A to 105° C T_J C= –40° C T_A to 105° C T_J	ZU = TBGA VV = TBGA (no lead)	e300 core speed AD = 266 MHz AG = 400 MHz	D = 266 MHz	E = 300 MHz G = 400 MHz	A = rev. 2.1 silicon
	8360				e300 core speed AG = 400 MHz AJ = 533 MHz AL = 667 MHz	D = 266 MHz F = 333 MHz	G = 400 MHz H = 500 MHz	A = rev. 2.1 silicon
MPC (rev. 2.0 silicon only)	8360	Blank = not included E = included	0° C T_A to 70° C T_J	ZU = TBGA VV = TBGA (no lead)	e300 core speed AH = 500 MHz AL = 667 MHz	F = 333 MHz	G = 400 MHz H = 500 MHz	—

Notes:
1. Not all processor, platform, and QUICC Engine block frequency combinations are supported. For available frequency combinations, contact your local Freescale sales office or authorized distributor.
2. See Section 20, "Package and Pin Listings," for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

This table shows the SVR settings by device and package type.

Table 81. SVR Settings

Device	Package	SVR (Rev. 2.0)	SVR (Rev. 2.1)
MPC8360E	TBGA	0x8048_0020	0x8048_0021
MPC8360	TBGA	0x8049_0020	0x8049_0021