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NXP USA Inc. - KMPC8360VVAHFH Datasheet



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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8360vvahfh

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Power Sequencing

This table shows the estimated typical I/O power dissipation for the device.

Interface	Parameter	GV _{DD} (1.8 V)	GV _{DD} (2.5 V)	OV _{DD} (3.3 V)	LV _{DD} (3.3 V)	LV _{DD} (2.5 V)	Unit	Comments
DDR I/O	200 MHz, 1 \times 32 bits	0.3	0.46	_	_	—	W	—
$R_s = 20 \Omega$	200 MHz, 1 \times 64 bits	0.4	0.58			—	W	—
$R_t = 50 \Omega$	200 MHz, 2×32 bits	0.6	0.92	_	_	—	W	_
	266 MHz, 1 \times 32 bits	0.35	0.56	_	_	—	W	_
	266 MHz, 1 \times 64 bits	0.46	0.7	_	_	—	W	_
	266 MHz, 2×32 bits	0.7	1.11		—	—	W	_
	333 MHz, 1 \times 32 bits	0.4	0.65	_	_	—	W	_
	333 MHz, 1 \times 64 bits	0.53	0.82		—	—	W	_
	333 MHz, 2×32 bits	0.81	1.3		—	—	W	_
Local Bus I/O	133 MHz, 32 bits	—	—	0.22	_	_	W	_
3 pairs of clocks	83 MHz, 32 bits	—	—	0.14	—	—	W	—
	66 MHz, 32 bits	—	—	0.12	—	—	W	_
	50 MHz, 32 bits	—	—	0.09	—	—	W	_
PCI I/O	33 MHz, 32 bits	—	—	0.05	—	—	W	_
Load = 30 pF	66 MHz, 32 bits	—	—	0.07	—	—	W	—
10/100/1000	MII or RMII	—	—	_	0.01	—	W	Multiply by
Load = 20 pF	GMII or TBI	—	—	_	0.04	—	W	interfaces used.
	RGMII or RTBI	—	—	—	—	0.04	W	
Other I/O	_	—	_	0.1	—	—	W	_

Table 6. Estimated Typical I/O Power Dissipation

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8360E/58E.

NOTE

The rise/fall time on QUICC Engine block input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of V_{DD} ; fall time refers to transitions from 90% to 10% of V_{DD} .

DC Electrical Characteristics



4.1 DC Electrical Characteristics

This table provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the device.

|--|

Parameter	Condition	Symbol	Min	Мах	Unit
Input high voltage	—	V _{IH}	2.7	OV _{DD} + 0.3	V
Input low voltage	—	V _{IL}	-0.3	0.4	V
CLKIN input current	0 V ≤V _{IN} ≤OV _{DD}	I _{IN}	—	±10	μA
PCI_SYNC_IN input current	0 V ≤V _{IN} ≤0.5V or OV _{DD} – 0.5V ≤V _{IN} ≤OV _{DD}	I _{IN}	_	±10	μΑ
PCI_SYNC_IN input current	0.5 V ≤V _{IN} ≤OV _{DD} – 0.5 V	I _{IN}	—	±100	μA

4.2 AC Electrical Characteristics

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 8.	CLKIN	AC	Timing	Specifications
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Parameter/Condition	Symbol	Min	Typical	Мах	Unit	Notes
CLKIN/PCI_CLK frequency	f _{CLKIN}	—	—	66.67	MHz	1
CLKIN/PCI_CLK cycle time	t _{CLKIN}	15	—	_	ns	—
CLKIN/PCI_CLK rise and fall time	t _{KH} , t _{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t _{KHK} /t _{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:

- 1. **Caution:** The system, core, USB, security, and 10/100/1000 Ethernet must not exceed their respective maximum or minimum operating frequencies.
- 2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 V and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the total input jitter-short term and long term-and is guaranteed by design.
- 5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.

4.3 Gigabit Reference Clock Input Timing

This table provides the Gigabit reference clocks (GTX_CLK125) AC timing specifications.

Table 9. GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 \pm 0.125 mV/ 3.3 V \pm 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
GTX_CLK125 frequency	t _{G125}	_	125	_	MHz	_
GTX_CLK125 cycle time	t _{G125}	_	8		ns	



DDR and DDR2 SDRAM AC Electrical Characteristics

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 21 and Table 22 provide the output AC timing specifications and measurement conditions for the DDR and DDR2 SDRAM interface.

Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter ⁸	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time, (MCK[n]/MCK[n] crossing)	t _{MCK}	6	10	ns	2
Skew between any MCK to ADDR/CMD 333 MHz 266 MHz 200 MHz	t _{AOSKEW}	-1.0 -1.1 -1.2	0.2 0.3 0.4	ns	3
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz 200 MHz	^t DDKHAS	2.1 2.8 3.5	_	ns	4
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz—DDR1 266 MHz—DDR2 200 MHz	t _{DDKHAX}	2.0 2.7 2.8 3.5		ns	4
MCS(n) output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t _{DDKHCS}	2.1 2.8 3.5	_	ns	4
MCS(n) output hold with respect to MCK 333 MHz 266 MHz 200 MHz	t _{DDKHCX}	2.0 2.7 3.5	_	ns	4
MCK to MDQS	t _{DDKHMH}	-0.8	0.7	ns	5, 9
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	t _{DDKHDS} , t _{DDKLDS}	0.7 1.0 1.2	_	ns	6
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	t _{DDKHDX} , t _{DDKLDX}	0.7 1.0 1.2	_	ns	6
MDQS preamble start	t _{DDKHMP}	$-0.5\timest_{MCK}-0.6$	$-0.5\timest_{\text{MCK}}\text{+}0.6$	ns	7



8.2.1.1 GMII Transmit AC Timing Specifications

This table provides the GMII transmit AC timing specifications.

Table 27. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
GTX_CLK clock period	t _{GTX}	_	8.0		ns	_
GTX_CLK duty cycle	t _{GTXH/tGTX}	40	_	60	%	—
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	^t GTKHDX ^t GTKHDV	0.5	_	 5.0	ns	3
GTX_CLK clock rise time, (20% to 80%)	t _{GTXR}	_	_	1.0	ns	_
GTX_CLK clock fall time, (80% to 20%)	t _{GTXF}	_	_	1.0	ns	—
GTX_CLK125 clock period	t _{G125}	_	8.0	_	ns	2
GTX_CLK125 reference clock duty cycle measured at $LV_{DD/2}$	t _{G125H} /t _{G125}	45		55	%	2

Notes:

- 1. The symbols used for timing specifications follow the pattern t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{ignx} clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- 2. This symbol is used to represent the external GTX_CLK125 signal and does not follow the original symbol naming convention.
- In rev. 2.0 silicon, due to errata, t_{GTKHDX} minimum and t_{GTKHDV} maximum are not supported when the GTX_CLK is selected. Refer to Errata QE_ENET18 in Chip Errata for the MPC8360E, Rev. 1.

This figure shows the GMII transmit AC timing diagram.



Figure 10. GMII Transmit AC Timing Diagram



GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

8.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

Table 34. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
PMA_RX_CLK clock period	t _{TRX}	_	16.0	_	ns	—
PMA_RX_CLK skew	t _{SKTRX}	7.5	_	8.5	ns	—
RX_CLK duty cycle	t _{TRXH} /t _{TRX}	40	_	60	%	—
RCG[9:0] setup time to rising PMA_RX_CLK	t _{TRDVKH}	2.5	—		ns	2
RCG[9:0] hold time to rising PMA_RX_CLK	t _{trdxkh}	1.0	_	_	ns	2
RX_CLK clock rise time, $V_{IL}(min)$ to $V_{IH}(max)$	t _{TRXR}	0.7	_	2.4	ns	—
RX_CLK clock fall time, $V_{IH}(max)$ to $V_{IL}(min)$	t _{TRXF}	0.7	_	2.4	ns	—

Notes:

- 1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).}
- 2. Setup and hold time of even numbered RCG are measured from riding edge of PMA_RX_CLK1. Setup and hold time of odd numbered RCG are measured from riding edge of PMA_RX_CLK0.

This figure shows the TBI receive AC timing diagram.



Figure 19. TBI Receive AC Timing Diagram



8.3.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 37. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC frequency	f _{MDC}	—	2.5	—	MHz	2
MDC period	t _{MDC}	—	400	—	ns	—
MDC clock pulse width high	t _{MDCH}	32	—	—	ns	_
MDC to MDIO delay	^t мрткнрх ^t мрткнрv	10 —	_	 110	ns	3
MDIO to MDC setup time	t _{MDRDVKH}	10	—	—	ns	—
MDIO to MDC hold time	t _{MDRDXKH}	0	—	—	ns	—
MDC rise time	t _{MDCR}	—	—	10	ns	—
MDC fall time	t _{MDHF}	_	_	10	ns	

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDRDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
 </sub>
- This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
- 3. This parameter is dependent on the ce_clk speed (that is, for a ce_clk of 200 MHz, the delay is 90 ns and for a ce_clk of 300 MHz, the delay is 63 ns).

This figure shows the MII management AC timing diagram.



Figure 21. MII Management Interface Timing Diagram





Figure 27. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (DLL Bypass Mode)



10.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device.

This table provides the JTAG AC timing specifications as defined in Figure 30 through Figure 33.

Table 43. JTAG AC Timing Specifications (Independent of CLKIN)¹

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f _{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t _{JTG}	30	—	ns	_
JTAG external clock duty cycle	t _{JTKHKL} /t _{JTG}	45	55	%	_
JTAG external clock rise and fall times	t _{JTGR} & t _{JTGF}	0	2	ns	_
TRST assert time	t _{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	t _{JTDVKH} t _{JTIVKH}	4 4	_	ns	4
Input hold times: Boundary-scan data TMS, TDI	t _{JTDXKH} t _{JTIXKH}	10 10	_	ns	4
Valid times: Boundary-scan data TDO	t _{JTKLDV} t _{JTKLOV}	2 2	11 11	ns	5
Output hold times: Boundary-scan data TDO	t _{jtkldx} t _{jtklox}	2 2	_	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	t _{JTKLDZ} t _{JTKLOZ}	2 2	19 9	ns	5, 6

Notes:

- 2. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
- 4. Non-JTAG signal input timing with respect to t_{TCLK}.
- 5. Non-JTAG signal output timing with respect to t_{TCLK}.
- 6. Guaranteed by design and characterization.

All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 22). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.



This figure shows the PCI input AC timing conditions.



Figure 37. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.



13 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8360E/58E.

13.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the device timer pins, including TIN, TOUT, TGATE, and RTC_CLK.

Table 49. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	_	V
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	$0 \ V \leq V_{IN} \leq OV_{DD}$	_	±10	μA



Timers AC Timing Specifications

13.2 Timers AC Timing Specifications

This table provides the timer input and output AC timing specifications.

Table 50. Timers Input AC Timing Specifications¹

Characteristic	Symbol ²	Тур	Unit
Timers inputs—minimum pulse width	t _{TIWID}	20	ns

Notes:

- 1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
- 2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

This figure provides the AC test load for the timers.



Figure 39. Timers AC Test Load

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8360E/58E.

14.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the device GPIO.

Table 51. GPIO DC Electrical Characteristic

Characteristic	Symbol	Condition	Min	Мах	Unit	Notes
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	_	V	1
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V	1
Input low voltage	V _{IL}	—	-0.3	0.8	V	—
Input current	I _{IN}	0 V ≤V _{IN} ≤OV _{DD}	—	±10	μA	—

Note:

1. This specification applies when operating from 3.3-V supply.



HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

Characteristic	Symbol ²	Min	Мах	Unit
Outputs—Internal clock high impedance	t _{нікнох}	-0.5	5.5	ns
Outputs—External clock high impedance	t _{НЕКНОХ}	1	8	ns
Inputs—Internal clock input setup time	t _{HIIVKH}	8.5	_	ns
Inputs—External clock input setup time	t _{HEIVKH}	4	-	ns
Inputs—Internal clock input hold time	t _{HIIXKH}	1.4	_	ns
Inputs—External clock input hold time	t _{HEIXKH}	1	_	ns

Table 62. HDLC, BISYNC, and Transparent AC Timing Specifications¹ (continued)

Notes:

- 1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
 </sub>

Characteristic	Symbol ²	Min	Мах	Unit
Outputs—Internal clock delay	t _{UAIKHOV}	0	11.3	ns
Outputs—External clock delay	t _{UAEKHOV}	1	14	ns
Outputs—Internal clock high impedance	t _{UAIKHOX}	0	11	ns
Outputs—External clock high impedance	t _{UAEKHOX}	1	14	ns
Inputs—Internal clock input setup time	t _{UAIIVKH}	6	—	ns
Inputs—External clock input setup time	t _{UAEIVKH}	8	—	ns
Inputs—Internal clock input hold time	t _{UAIIXKH}	1	—	ns
Inputs—External clock input hold time	t _{UAEIXKH}	1	—	ns

Notes:

- 1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
 </sub></sub>

This figure provides the AC test load.



Figure 49. AC Test Load



18.3 AC Test Load

These figures represent the AC timing from Table 62 and Table 63. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the timing with external clock.



Figure 50. AC Timing (External Clock) Diagram

This figure shows the timing with internal clock.



Figure 51. AC Timing (Internal Clock) Diagram



USB DC Electrical Characteristics

19 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8360E/58E.

19.1 USB DC Electrical Characteristics

This table provides the DC electrical characteristics for the USB interface.

Table 64. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
High-level output voltage, $I_{OH} = -100 \ \mu A$	V _{OH}	OV _{DD} - 0.4	—	V
Low-level output voltage, I _{OL} = 100 μA	V _{OL}	—	0.2	V
Input current	I _{IN}	—	±10	μA

19.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface of the device.

Table 65. USB General Timing Parameters

Parameter	Symbol ¹	Min	Max	Unit	Notes	Note
USB clock cycle time	t _{USCK}	20.83		ns	Full speed 48 MHz	_
USB clock cycle time	t _{USCK}	166.67		ns	Low speed 6 MHz	_
Skew between TXP and TXN	t _{USTSPN}	_	5	ns	—	2
Skew among RXP, RXN, and RXD	t _{USRSPND}	_	10	ns	Full speed transitions	2
Skew among RXP, RXN, and RXD	t _{USRPND}		100	ns	Low speed transitions	2

Notes:

The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(state)(signal)} for receive signals and t_{(first two letters of functional block)(state)(signal)} for transmit signals. For example, t_{USRSPND} symbolizes USB timing (US) for the USB receive signals skew (RS) among RXP, RXN, and RXD (PND). Also, t_{USTSPN} symbolizes USB timing (US) for the USB transmit signals skew (TS) between TXP and TXN (PN).

2. Skew measurements are done at $OV_{DD}/2$ of the rising or falling edge of the signals.

This figure provide the AC test load for the USB.



Figure 52. USB AC Test Load



Pinout Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC1_MCKE[0:1]	AL32, AU33	0	GV _{DD}	3
MEMC1_MCK[0:1]	AK37, AT37	0	GV _{DD}	
MEMC1_MCK[2:3]/ MEMC2_MCK[0:1]	AN1, AR2	0	GV _{DD}	_
MEMC1_MCK[4:5]/ MEMC2_MCKE[0:1]	AN25, AK1	0	GV _{DD}	_
MEMC1_MCK[0:1]	AL37, AT36	0	GV _{DD}	_
MEMC1_MCK[2:3]/ MEMC2_MCK[0:1]	AP2, AT2	0	GV _{DD}	_
MEMC1_MCK[4]/ MEMC2_MDM[8]	AN24	0	GV _{DD}	
MEMC1_MCK[5]/ MEMC2_MDQS[8]	AL1	0	GV _{DD}	_
MDIC[0:1]	АН6, АР30	I/O	GV _{DD}	10
Sec	ondary DDR SDRAM Memory Controller Interface			
MEMC2_MECC[0:7]	AN16, AP18, AM16, AM17, AN17, AP13, AP15, AN13	I/O	GV _{DD}	_
MEMC2_MBA[0:2]	AU12, AU15, AU13	0	GV _{DD}	_
MEMC2_MA[0:14]	AT12, AP11, AT13, AT14, AR13, AR15, AR16, AT16, AT18, AT17, AP10, AR20, AR17, AR14, AR11	0	GV _{DD}	_
MEMC2_MWE	AU10	0	GV _{DD}	_
MEMC2_MRAS	AT11	0	GV _{DD}	_
MEMC2_MCAS	AU11	0	GV _{DD}	
	PCI			
PCI_INTA/IRQ_OUT/CE_PF[5]	A20	I/O	LV _{DD} 2	2
PCI_RESET_OUT/CE_PF[6]	E19	I/O	LV _{DD} 2	_
PCI_AD[31:30]/CE_PG[31:30]	D20, D21	I/O	LV _{DD} 2	
PCI_AD[29:25]/CE_PG[29:25]	A24, B23, C23, E23, A26	I/O	OV _{DD}	
PCI_AD[24]/CE_PG[24]	B21	I/O	LV _{DD} 2	_
PCI_AD[23:0]/CE_PG[23:0]	C24, C25, D25, B25, E24, F24, A27, A28, F27, A30, C30, D30, E29, B31, C31, D31, D32, A32, C33, B33, F30, E31, A34, D33	I/O	OV _{DD}	
PCI_C/BE[3:0]/CE_PF[10:7]	E22, B26, E28, F28	I/O	OV _{DD}	
PCI_PAR/CE_PF[11]	D28	I/O	OV _{DD}	
PCI_FRAME/CE_PF[12]	D26	I/O	OV _{DD}	5
PCI_TRDY/CE_PF[13]	C27	I/O	OV _{DD}	5
PCI_IRDY/CE_PF[14]	C28	I/O	OV _{DD}	5
PCI_STOP/CE_PF[15]	B28	I/O	OV _{DD}	5



Pinout Listings

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes				
	PMC							
QUIESCE	B36	0	OV _{DD}	_				
	System Control							
PORESET	L37	I	OV _{DD}	—				
HRESET	L36	I/O	OV _{DD}	1				
SRESET	M33	I/O	OV _{DD}	2				
	Thermal Management							
THERM0	AP19	Ι	GV _{DD}	—				
THERM1	AT31	I	GV _{DD}	—				
	Power and Ground Signals							
AV _{DD} 1	K35	Power for LBIU DLL (1.2 V)	AV _{DD} 1	_				
AV _{DD} 2	К36	Power for CE PLL (1.2 V)	AV _{DD} 2	_				
AV _{DD} 5	AM29	Power for e300 PLL (1.2 V)	AV _{DD} 5	_				
AV _{DD} 6	К37	Power for system PLL (1.2 V)	AV _{DD} 6	_				
GND	A2, A8, A13, A19, A22, A25, A31, A33, A36, B7, B12, B24, B27, B30, C4, C6, C9, C15, C26, C32, D3, D8, D11, D14, D17, D19, D23, D27, E7, E13, E25, E30, E36, F4, F37, G34, H1, H5, H32, H33, J4, J32, J37, K1, L3, L5, L33, L34, M1, M34, M35, N37, P2, P5, P35, P36, R4, T3, U1, U5, U35, V37, W1, W4, W33, W36, Y34, AA3, AA5, AC3, AC32, AC35, AD1, AD37, AE4, AE34, AE36, AF33, AG4, AG6, AG32, AH35, AJ1, AJ4, AJ32, AJ35, AJ37, AK36, AL3, AL34, AM4, AN6, AN23, AN30, AP8, AP12, AP14, AP16, AP17, AP20, AP25, AR6, AR8, AR9, AR19, AR24, AR31, AR35, AR37, AT4, AT10, AT19, AT20, AT25, AU14, AU22, AU28, AU35	_	_	_				
GV _{DD}	AD4, AE3, AF1, AF5, AF35, AF37, AG2, AG36, AH33, AH34, AK5, AM1, AM35, AM37, AN2, AN10, AN11, AN12, AN14, AN32, AN36, AP5, AP23, AP28, AR1, AR7, AR10, AR12, AR21, AR25, AR27, AR33, AT15, AT22, AT28, AT33, AU2, AU5, AU16, AU31, AU36	Power for DDR DRAM I/O voltage (2.5 or 1.8 V)	GV _{DD}					



This figure shows the internal distribution of clocks within the MPC8358E.





The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Note that in PCI host mode, the primary clock input also depends on whether PCI clock outputs are selected with RCWH[PCICKDRV]. When the device is configured as a PCI host device (RCWH[PCIHOST] = 1) and PCI clock output is selected (RCWH[PCICKDRV] = 1), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (\div 2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCIOEN*n*] parameters enable the PCI_CLK_OUT*n*, respectively.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input



Core PLL Configuration

21.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). This table shows the encodings for RCWL[COREPLL]. COREPLL values not listed in this table should be considered reserved.

RCWL[COREPLL]			core_clk:csb_clk	VCO divider	
0–1	2–5	6	Ratio		
nn	0000	n	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)	
00	0001	0	1:1	÷2	
01	0001	0	1:1	÷4	
10	0001	0	1:1	÷8	
11	0001	0	1:1	÷8	
00	0001	1	1.5:1	÷2	
01	0001	1	1.5:1	÷4	
10	0001	1	1.5:1	÷8	
11	0001	1	1.5:1	÷8	
00	0010	0	2:1	÷2	
01	0010	0	2:1	÷4	
10	0010	0	2:1	÷8	
11	0010	0	2:1	÷8	
00	0010	1	2.5:1	÷2	
01	0010	1	2.5:1	÷4	
10	0010	1	2.5:1	÷8	
11	0010	1	2.5:1	÷8	
00	0011	0	3:1	÷2	
01	0011	0	3:1	÷4	
10	0011	0	3:1	÷8	
11	0011	0	3:1	÷8	

Table 73. e300 Core PLL Configuration

NOTE

Core VCO frequency = Core frequency \times VCO divider. The VCO divider (RCWL[COREPLL[0:1]]) must be set properly so that the core VCO frequency is in the range of 800–1800 MHz. Having a core frequency below the CSB frequency is not a possible option because the core frequency must be equal to or greater than the CSB frequency.



21.3 QUICC Engine Block PLL Configuration

The QUICC Engine block PLL is controlled by the RCWL[CEPMF], RCWL[CEPDF], and RCWL[CEVCOD] parameters. This table shows the multiplication factor encodings for the QUICC Engine block PLL.

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF])
00000	0	× 16
00001	0	Reserved
00010	0	× 2
00011	0	× 3
00100	0	× 4
00101	0	× 5
00110	0	× 6
00111	0	× 7
01000	0	× 8
01001	0	× 9
01010	0	× 10
01011	0	× 11
01100	0	× 12
01101	0	× 13
01110	0	× 14
01111	0	× 15
10000	0	× 16
10001	0	× 17
10010	0	× 18
10011	0	× 19
10100	0	× 20
10101	0	× 21
10110	0	× 22
10111	0	× 23
11000	0	× 24
11001	0	× 25
11010	0	× 26
11011	0	× 27
11100	0	× 28

Table 74. QUICC Engine Block PLL Multiplication Factors



QUICC Engine Block PLL Configuration

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF])
11101	0	× 29
11110	0	× 30
11111	0	× 31
00011	1	× 1.5
00101	1	× 2.5
00111	1	× 3.5
01001	1	× 4.5
01011	1	× 5.5
01101	1	× 6.5
01111	1	× 7.5
10001	1	× 8.5
10011	1	× 9.5
10101	1	× 10.5
10111	1	× 11.5
11001	1	× 12.5
11011	1	× 13.5
11101	1	× 14.5

Table 74. QUICC Engine Block PLL Multiplication Factors (continued)

Note:

1. Reserved modes are not listed.

The RCWL[CEVCOD] denotes the QUICC Engine Block PLL VCO internal frequency as shown in this table.

Table 75. QUICC Engine Block PLL VCO Divider

RCWL[CEVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine block VCO frequency is in the range of 600–1400 MHz. The QUICC Engine block frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine block frequencies should be selected according to the performance requirements.



23.7 Pull-Up Resistor Requirements

The device requires high resistance pull-up resistors (10 k Ω is recommended) on open drain type pins including I²C pins, Ethernet Management MDIO pin, and EPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, see *MPC8360E/MPC8358E PowerQUICC Design Checklist* (AN3097).

24 Ordering Information

24.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the MPC8360E/58E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. Additionally to the processor frequency, the part numbering scheme also includes an application modifier, which may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number.

MPC	nnnn	е	t	рр	aa	а	а	Α
Product Code	Part Identifier	Encryption Acceleration	Temperature Range	Package ²	Processor Frequency ³	Platform Frequency	QUICC Engine Frequency	Die Revision
MPC	8358	Blank = not included E = included	Blank = 0° C T _A to 105° C T _J	ZU = TBGA VV = TBGA (no lead)	e300 core speed AD = 266 MHz AG = 400 MHz	D = 266 MHz	E = 300 MHz G = 400 MHz	A = rev. 2.1 silicon
	8360		$C = -40^{\circ} C T_{A}$ to 105° C T _J		e300 core speed AG = 400 MHz AJ = 533 MHz AL = 667 MHz	D = 266 MHz F = 333 MHz	G = 400 MHz H = 500 MHz	A = rev. 2.1 silicon
MPC (rev. 2.0 silicon only)	8360	Blank = not included E = included	0° C T _A to 70° C T _J	ZU = TBGA VV = TBGA (no lead)	e300 core speed AH = 500 MHz AL = 667 MHz	F = 333 MHz	G = 400 MHz H = 500 MHz	_

Table 80. Part Numbering Nomenclature¹

Notes:

1. Not all processor, platform, and QUICC Engine block frequency combinations are supported. For available frequency combinations, contact your local Freescale sales office or authorized distributor.

2. See Section 20, "Package and Pin Listings," for more information on available package types.

Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this
specification support all core frequencies. Additionally, parts addressed by part number specifications may support other
maximum core frequencies.

This table shows the SVR settings by device and package type.

Table 81.	SVR	Settings
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Device	Package	SVR (Rev. 2.0)	SVR (Rev. 2.1)
MPC8360E	TBGA	0x8048_0020	0x8048_0021
MPC8360	TBGA	0x8049_0020	0x8049_0021