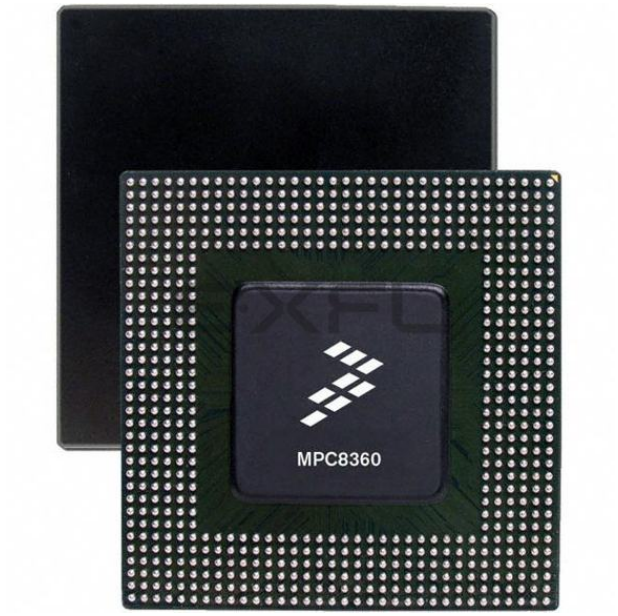

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8360zuajdga

This figure shows the MPC8358E block diagram.

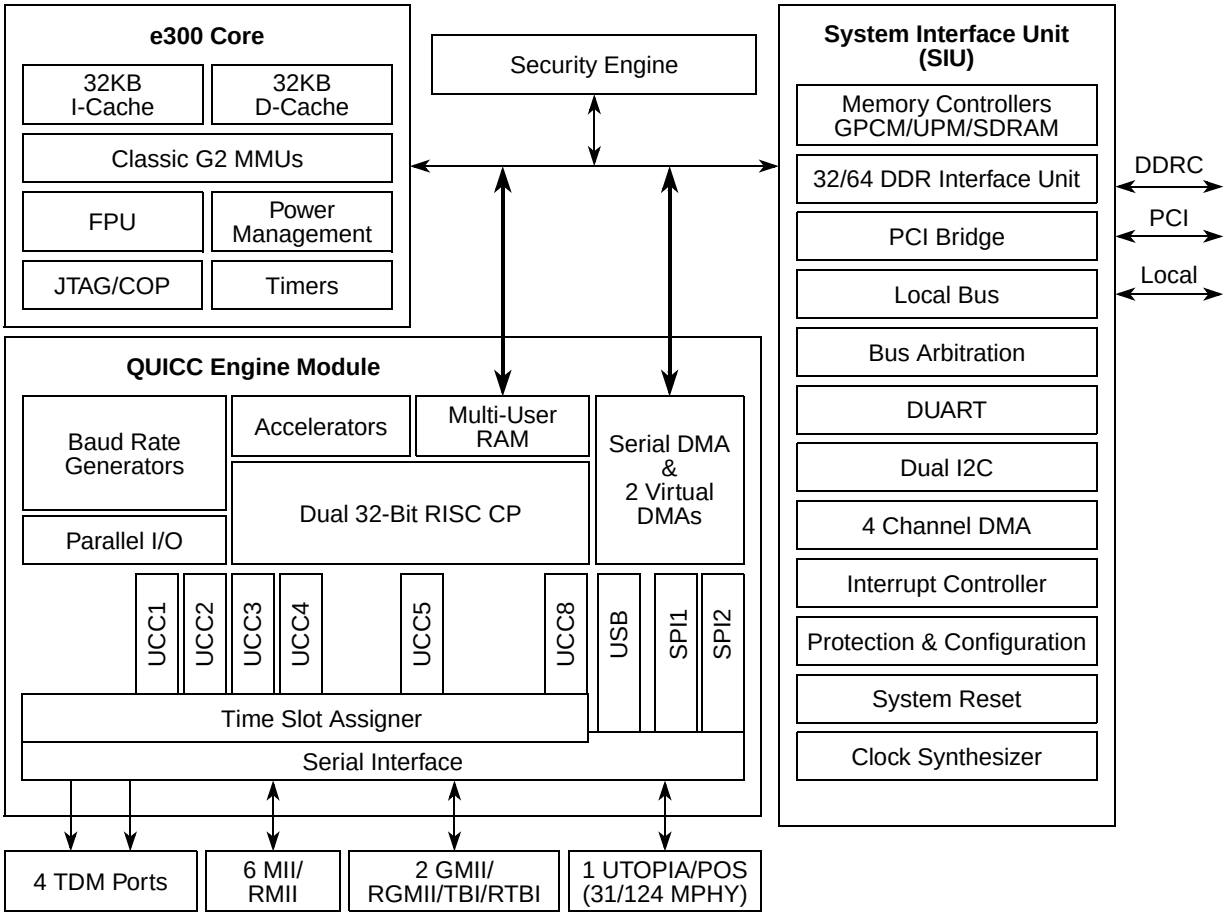

Figure 2. MPC8358E Block Diagram

Major features of the MPC8360E/58E are as follows:

- e300 PowerPC processor core (enhanced version of the MPC603e core)
  - Operates at up to 667 MHz (for the MPC8360E) and 400 MHz (for the MPC8358E)
  - High-performance, superscalar processor core
  - Floating-point, integer, load/store, system register, and branch processing units
  - 32-Kbyte instruction cache, 32-Kbyte data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - Software-compatible with the Freescale processor families implementing the Power Architecture™ technology
- QUICC Engine unit
  - Two 32-bit RISC controllers for flexible support of the communications peripherals, each operating up to 500 MHz (for the MPC8360E) and 400 MHz (for the MPC8358E)
  - Serial DMA channel for receive and transmit on all serial channels
  - QUICC Engine module peripheral request interface (for SEC, PCI, IEEE Std. 1588™)
  - Eight universal communication controllers (UCCs) on the MPC8360E and six UCCs on the MPC8358E supporting the following protocols and interfaces (not all of them simultaneously):
    - IEEE 1588 protocol supported

2.2.1 Power-Up Sequencing

MPC8360E/58E does not require the core supply voltage (V_{DD} and AV_{DD}) and I/O supply voltages (GV_{DD}, LV_{DD}, and OV_{DD}) to be applied in any particular order. During the power ramp up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there may be a period of time that all input and output pins are actively be driven and cause contention and excessive current from 3A to 5A. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD}, LV_{DD}, and OV_{DD}) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V, see this figure.

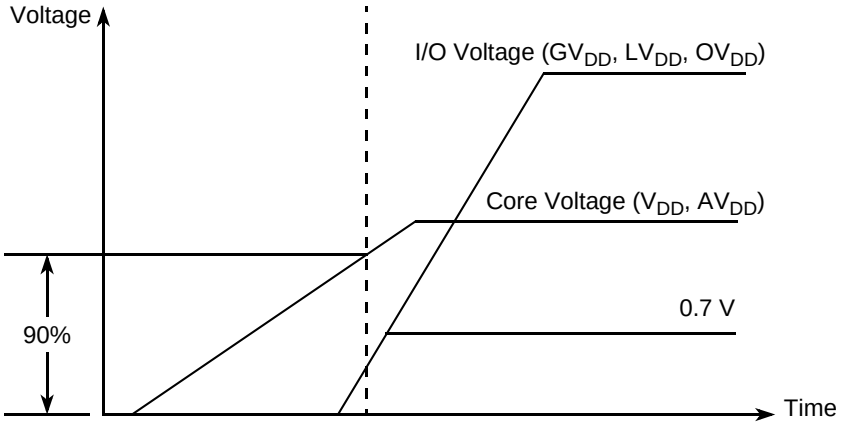

Figure 5. Power Sequencing Example

I/O voltage supplies (GV_{DD}, LV_{DD}, and OV_{DD}) do not have any ordering requirements with respect to one another.

2.2.2 Power-Down Sequencing

The MPC8360E/58E does not require the core supply voltage and I/O supply voltages to be powered down in any particular order.

3 Power Characteristics

The estimated typical power dissipation values are shown in these tables.

Table 4. MPC8360E TBGA Core Power Dissipation[1]

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	500	5.0	5.6	W	2, 3, 5
400	266	400	4.5	5.0	W	2, 3, 4
533	266	400	4.8	5.3	W	2, 3, 4
667	333	400	5.8	6.3	W	3, 6, 7, 8
500	333	500	5.9	6.4	W	3, 6, 7, 8

This table shows the estimated typical I/O power dissipation for the device.

Table 6. Estimated Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	Unit	Comments
DDR I/O 65% utilization R_S = 20 Ω R_t = 50 Ω 2 pairs of clocks	200 MHz, 1 × 32 bits	0.3	0.46	—	—	—	W	—
	200 MHz, 1 × 64 bits	0.4	0.58	—	—	—	W	—
	200 MHz, 2 × 32 bits	0.6	0.92	—	—	—	W	—
	266 MHz, 1 × 32 bits	0.35	0.56	—	—	—	W	—
	266 MHz, 1 × 64 bits	0.46	0.7	—	—	—	W	—
	266 MHz, 2 × 32 bits	0.7	1.11	—	—	—	W	—
	333 MHz, 1 × 32 bits	0.4	0.65	—	—	—	W	—
	333 MHz, 1 × 64 bits	0.53	0.82	—	—	—	W	—
	333 MHz, 2 × 32 bits	0.81	1.3	—	—	—	W	—
Local Bus I/O Load = 25 pf 3 pairs of clocks	133 MHz, 32 bits	—	—	0.22	—	—	W	—
	83 MHz, 32 bits	—	—	0.14	—	—	W	—
	66 MHz, 32 bits	—	—	0.12	—	—	W	—
	50 MHz, 32 bits	—	—	0.09	—	—	W	—
PCI I/O Load = 30 pF	33 MHz, 32 bits	—	—	0.05	—	—	W	—
	66 MHz, 32 bits	—	—	0.07	—	—	W	—
10/100/1000 Ethernet I/O Load = 20 pF	MII or RMII	—	—	—	0.01	—	W	Multiply by number of interfaces used.
	GMII or TBI	—	—	—	0.04	—	W	
	RGMII or RTBI	—	—	—	—	0.04	W	
Other I/O	—	—	—	0.1	—	—	W	—

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8360E/58E.

NOTE

The rise/fall time on QUICC Engine block input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of V_{DD}; fall time refers to transitions from 90% to 10% of V_{DD}.

4.1 DC Electrical Characteristics

This table provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the device.

Table 7. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.4	V
CLKIN input current	0 V ≤V_{IN} ≤OV_{DD}	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	0 V ≤V_{IN} ≤0.5V or OV_{DD} – 0.5V ≤V_{IN} ≤OV_{DD}	I_{IN}	—	±10	μA
PCI_SYNC_IN input current	0.5 V ≤V_{IN} ≤OV_{DD} – 0.5 V	I_{IN}	—	±100	μA

4.2 AC Electrical Characteristics

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 8. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
CLKIN/PCI_CLK frequency	f_{CLKIN}	—	—	66.67	MHz	1
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	—	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:

1. **Caution:** The system, core, USB, security, and 10/100/1000 Ethernet must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.

4.3 Gigabit Reference Clock Input Timing

This table provides the Gigabit reference clocks (GTX_CLK125) AC timing specifications.

Table 9. GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—

Table 16. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	MV_{REF} + 0.18	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.18	V	—
Output leakage current	I_{OZ}	—	±10	µA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–15.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	15.2	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	±10	µA	—
Input current (0 V ≤V_{IN} ≤OV_{DD})	I_{IN}	—	±10	µA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤V_{OUT} ≤GV_{DD}.

This table provides the DDR capacitance when GV_{DD}(typ) = 2.5 V.

Table 17. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25° C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM interface when GV_{DD}(typ) = 1.8 V.

Table 18. DDR2 SDRAM Input AC Timing Specifications for GV_{DD}(typ) = 1.8 V

At recommended operating conditions with GV_{DD} of 1.8 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V	—

This figure provides the AC test load for the DDR bus.

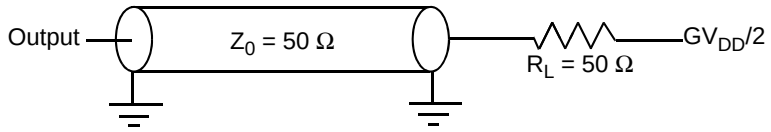

Figure 8. DDR AC Test Load

Table 22. DDR and DDR2 SDRAM Measurement Conditions

Symbol	DDR	DDR2	Unit	Notes
V_{TH}	MV_{REF} ± 0.31 V	MV_{REF} ± 0.25 V	V	1
V_{OUT}	0.5 × GV_{DD}	0.5 × GV_{DD}	V	2

Notes:
1. Data input threshold measurement point.
2. Data output measurement point.

This figure shows the DDR SDRAM output timing diagram for source synchronous mode.

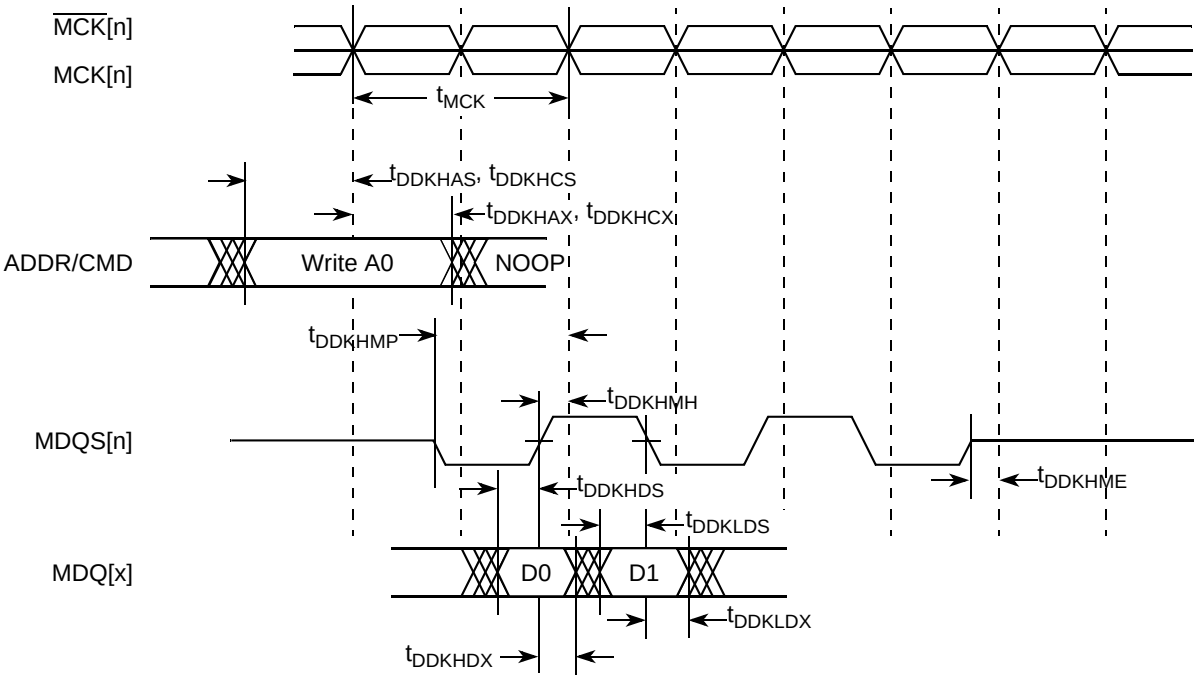

Figure 9. DDR SDRAM Output Timing Diagram for Source Synchronous Mode

Table 40. Local Bus General Timing Parameters—DLL Enabled (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3.0	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to LALE rise	t_{LBKHLR}	—	4.5	ns	—
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	4.5	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	4.5	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	4.5	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	1.0	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	1.0	—	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	3.8	ns	8

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to rising edge of LSYNC_IN.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This table describes the general timing parameters of the local bus interface of the device.

Table 41. Local Bus General Timing Parameters—DLL Bypass Mode[9]

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7

10.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device.

This table provides the JTAG AC timing specifications as defined in Figure 30 through Figure 33.

Table 43. JTAG AC Timing Specifications (Independent of CLKIN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock duty cycle	t_{JTKHKL}/t_{JTG}	45	55	%	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 22). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

This figure provides the AC test load for the I^2C.

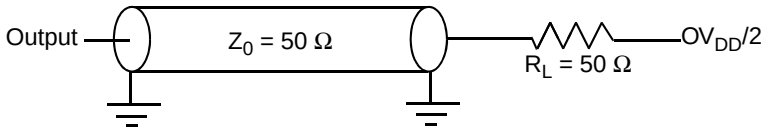

Figure 34. I^2C AC Test Load

This figure shows the AC timing diagram for the I^2C bus.

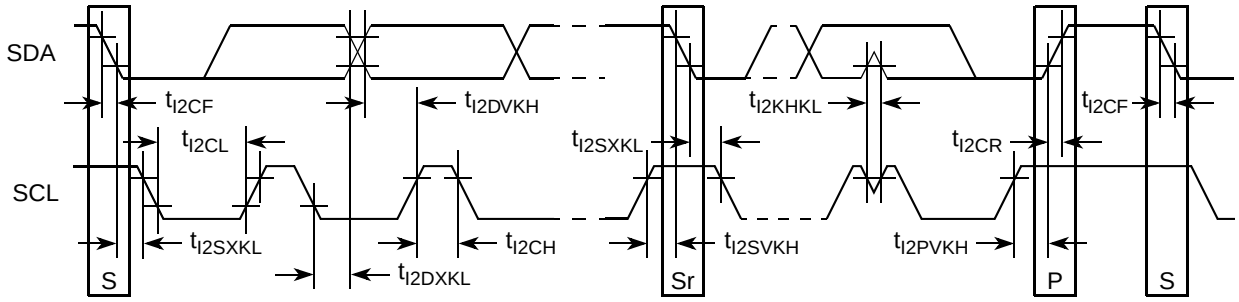

Figure 35. I^2C Bus AC Timing Diagram

12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8360E/58E.

12.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface of the device.

Table 46. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	$0.5 \times OV_{DD}$	$OV_{DD} + 0.5$	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	-0.5	$0.3 \times OV_{DD}$	V
High-level output voltage	V_{OH}	I_{OH} = –500 µA	$0.9 \times OV_{DD}$	—	V
Low-level output voltage	V_{OL}	I_{OL} = 1500 µA	—	$0.1 \times OV_{DD}$	V
Input current	I_{IN}	$0 V \leq V_{IN}$[1] $\leq OV_{DD}$	—	±10	µA

12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the device. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. This table provides the PCI AC timing specifications at 66 MHz.

Table 47. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2, 5
Output hold from clock	t_{PCKHOX}	1	—	ns	2

Table 47. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0.3	—	ns	2, 4, 6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. In rev. 2.0 silicon, due to errata, t_{PCIHOV} maximum is 6.6 ns. Refer to Errata PCI21 in *Chip Errata for the MPC8360E, Rev. 1*.
6. In rev. 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Refer to Errata PCI17 in *Chip Errata for the MPC8360E, Rev. 1*.

Table 48. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	7.0	—	ns	2, 2
Input hold from clock	t_{PCIXKH}	0.3	—	ns	2, 4, 5

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. In rev. 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Refer to Errata PCI17 in *Chip Errata for the MPC8360E, Rev. 1*.

This figure provides the AC test load for PCI.

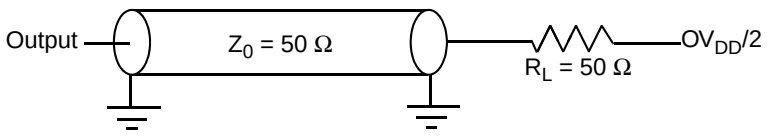

Figure 36. PCI AC Test Load

This figure shows the PCI input AC timing conditions.

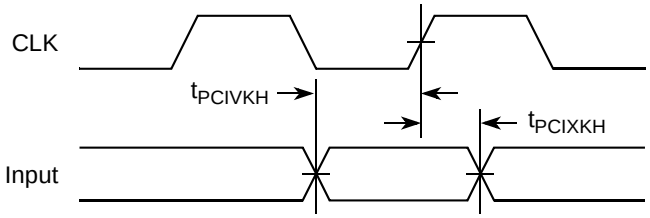

Figure 37. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.

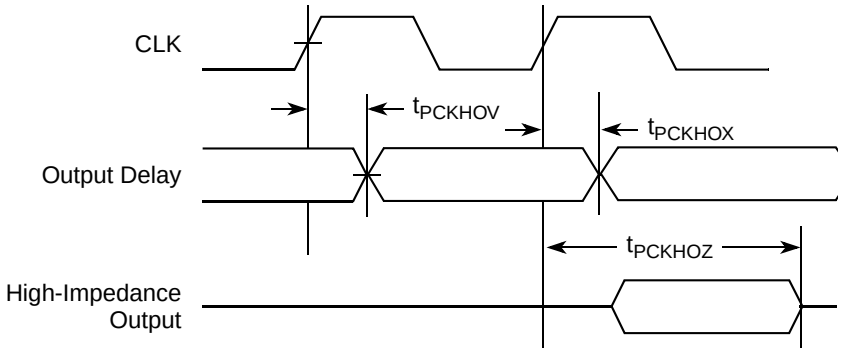

Figure 38. PCI Output AC Timing Measurement Condition

13 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8360E/58E.

13.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the device timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 49. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤V_{IN} ≤OV_{DD}	—	±10	μA

17 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8360E/58E.

17.1 TDM/SI DC Electrical Characteristics

This table provides the DC electrical characteristics for the device TDM/SI.

Table 57. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤V_{IN} ≤OV_{DD}	—	±10	μA

17.2 TDM/SI AC Timing Specifications

This table provides the TDM/SI input and output AC timing specifications.

Table 58. TDM/SI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max[3]	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	10	ns
TDM/SI outputs—External clock high impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
3. Timings are measured from the positive or negative edge of the clock, according to SIxMR [CE] and SITXCEI[TXCEIx]. Refer *MPC8360E Integrated Communications Processor Reference Manual* for more details.

This figure provides the AC test load for the TDM/SI.

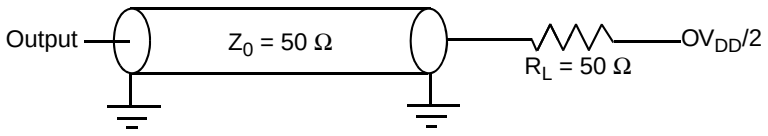

Figure 44. TDM/SI AC Test Load

Figure 45 represents the AC timing from Table 56. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Table 60. UTOPIA AC Timing Specifications[1] (continued)

Characteristic	Symbol[2]	Min	Max	Unit	Notes
UTOPIA inputs—Internal clock input hold time	t_{UIIXKH}	2.4	—	ns	—
UTOPIA inputs—External clock input hold time	t_{UEIXKH}	1	—	ns	3

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{UIKHOX} symbolizes the UTOPIA outputs internal timing (UI) for the time t_{UTOPIA} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
3. In rev. 2.0 silicon, due to errata, t_{UEIVKH} minimum is 4.3 ns and t_{UEIXKH} minimum is 1.4 ns under specific conditions. Refer to Errata QE_UPC3 in *Chip Errata for the MPC8360E, Rev. 1*.

This figure provides the AC test load for the UTOPIA.

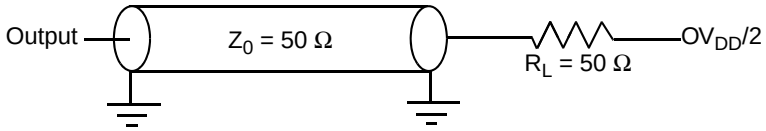

Figure 46. UTOPIA AC Test Load

These figures represent the AC timing from Table 56. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the UTOPIA timing with external clock.

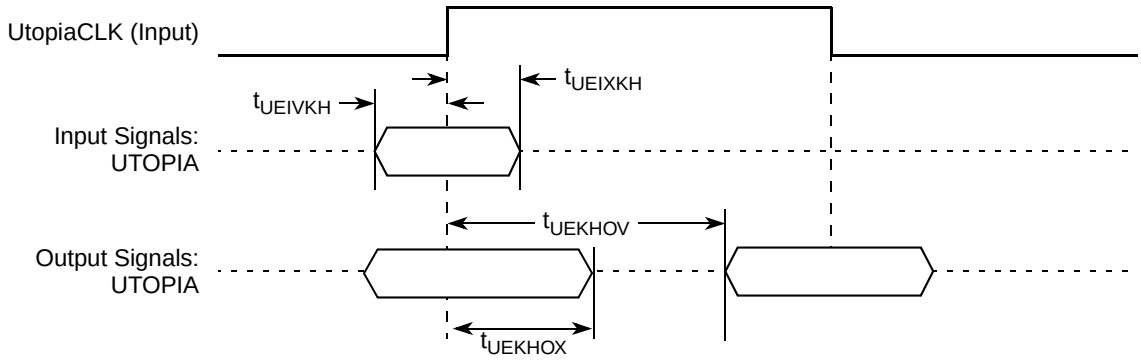

Figure 47. UTOPIA AC Timing (External Clock) Diagram

20 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8360E/58E is available in a tape ball grid array (TBGA), see Section 20.1, “Package Parameters for the TBGA Package,” and Section 20.2, “Mechanical Dimensions of the TBGA Package,” for information on the package.

20.1 Package Parameters for the TBGA Package

The package parameters for rev. 2.0 silicon are as provided in the following list. The package type is 37.5 mm × 37.5 mm, 740 tape ball grid array (TBGA).

Package outline	37.5 mm × 37.5 mm
Interconnects	740
Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder Balls	62 Sn/36 Pb/2 Ag (ZU package) 95.5 Sn/0.5 Cu/4Ag (VV package)
Ball diameter (typical)	0.64 mm

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_MODE	D36	I	OV_{DD}	—
M66EN/CE_PF[4]	B37	I/O	OV_{DD}	—
Local Bus Controller Interface				
LAD[0:31]	N32, N33, N35, N36, P37, P32, P34, R36, R35, R34, R33, T37, T35, T34, T33, U37, T32, U36, U34, V36, V35, W37, W35, V33, V32, W34, Y36, W32, AA37, Y33, AA35, AA34	I/O	OV_{DD}	—
LDP[0]/CKSTOP_OUT	AB37	I/O	OV_{DD}	—
LDP[1]/CKSTOP_IN	AB36	I/O	OV_{DD}	—
LDP[2]/LCS[6]	AB35	I/O	OV_{DD}	—
LDP[3]/LCS[7]	AA33	I/O	OV_{DD}	—
LA[27:31]	AC37, AA32, AC36, AC34, AD36	O	OV_{DD}	—
LCS[0:5]	AD33, AG37, AF34, AE33, AD32, AH37	O	OV_{DD}	—
LWE[0:3]/LSDDQM[0:3]/LBS[0:3]	AG35, AG34, AH36, AE32	O	OV_{DD}	—
LBCTL	AD35	O	OV_{DD}	—
LALE	M37	O	OV_{DD}	—
LGPL0/LSDA10/cfg_reset_source0	AB32	I/O	OV_{DD}	—
LGPL1/LSDWE/cfg_reset_source1	AE37	I/O	OV_{DD}	—
LGPL2/LSDRAS/LOE	AC33	O	OV_{DD}	—
LGPL3/LSDCAS/cfg_reset_source2	AD34	I/O	OV_{DD}	—
LGPL4/LGTA/LUPWAIT/LPBSE	AE35	I/O	OV_{DD}	—
LGPL5/cfg_clkin_div	AF36	I/O	OV_{DD}	—
LCKE	G36	O	OV_{DD}	—
LCLK[0]	J33	O	OV_{DD}	—
LCLK[1]/LCS[6]	J34	O	OV_{DD}	—
LCLK[2]/LCS[7]	G37	O	OV_{DD}	—
LSYNC_OUT	F34	O	OV_{DD}	—
LSYNC_IN	G35	I	OV_{DD}	—
Programmable Interrupt Controller				
MCP_OUT	E34	O	OV_{DD}	2
IRQ0/MCP_IN	C37	I	OV_{DD}	—
IRQ[1]/M1SRCID[4]/M2SRCID[4]/ LSRCID[4]	F35	I/O	OV_{DD}	—
IRQ[2]/M1DVAL/M2DVAL/LDVAL	F36	I/O	OV_{DD}	—
IRQ[3]/CORE_SRESET	H34	I/O	OV_{DD}	—

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{PORESET}}$	L37	I	OV_{DD}	—
$\overline{\text{HRESET}}$	L36	I/O	OV_{DD}	1
$\overline{\text{SRESET}}$	M33	I/O	OV_{DD}	2
Thermal Management				
THERM0	AP19	I	GV_{DD}	—
THERM1	AT31	I	GV_{DD}	—
Power and Ground Signals				
$AV_{DD}1$	K35	Power for LBIU DLL (1.2 V)	$AV_{DD}1$	—
$AV_{DD}2$	K36	Power for CE PLL (1.2 V)	$AV_{DD}2$	—
$AV_{DD}5$	AM29	Power for e300 PLL (1.2 V)	$AV_{DD}5$	—
$AV_{DD}6$	K37	Power for system PLL (1.2 V)	$AV_{DD}6$	—
GND	A2, A8, A13, A19, A22, A25, A31, A33, A36, B7, B12, B24, B27, B30, C4, C6, C9, C15, C26, C32, D3, D8, D11, D14, D17, D19, D23, D27, E7, E13, E25, E30, E36, F4, F37, G34, H1, H5, H32, H33, J4, J32, J37, K1, L3, L5, L33, L34, M1, M34, M35, N37, P2, P5, P35, P36, R4, T3, U1, U5, U35, V37, W1, W4, W33, W36, Y34, AA3, AA5, AC3, AC32, AC35, AD1, AD37, AE4, AE34, AE36, AF33, AG4, AG6, AG32, AH35, AJ1, AJ4, AJ32, AJ35, AJ37, AK36, AL3, AL34, AM4, AN6, AN23, AN30, AP8, AP12, AP14, AP16, AP17, AP20, AP25, AR6, AR8, AR9, AR19, AR24, AR31, AR35, AR37, AT4, AT10, AT19, AT20, AT25, AU14, AU22, AU28, AU35	—	—	—
GV_{DD}	AD4, AE3, AF1, AF5, AF35, AF37, AG2, AG36, AH33, AH34, AK5, AM1, AM35, AM37, AN2, AN10, AN11, AN12, AN14, AN32, AN36, AP5, AP23, AP28, AR1, AR7, AR10, AR12, AR21, AR25, AR27, AR33, AT15, AT22, AT28, AT33, AU2, AU5, AU16, AU31, AU36	Power for DDR DRAM I/O voltage (2.5 or 1.8 V)	GV_{DD}	—
$LV_{DD}0$	D5, D6	Power for UCC1 Ethernet interface (2.5 V, 3.3 V)	$LV_{DD}0$	—

Table 74. QUICC Engine Block PLL Multiplication Factors (continued)

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF])
11101	0	× 29
11110	0	× 30
11111	0	× 31
00011	1	× 1.5
00101	1	× 2.5
00111	1	× 3.5
01001	1	× 4.5
01011	1	× 5.5
01101	1	× 6.5
01111	1	× 7.5
10001	1	× 8.5
10011	1	× 9.5
10101	1	× 10.5
10111	1	× 11.5
11001	1	× 12.5
11011	1	× 13.5
11101	1	× 14.5

Note:
1. Reserved modes are not listed.

The RCWL[CEVCOD] denotes the QUICC Engine Block PLL VCO internal frequency as shown in this table.

Table 75. QUICC Engine Block PLL VCO Divider

RCWL[CEVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine block VCO frequency is in the range of 600–1400 MHz. The QUICC Engine block frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine block frequencies should be selected according to the performance requirements.

The QUICC Engine block VCO frequency is derived from the following equations:

ce_clk = (primary clock input × CEPMF) ÷ (1 + CEPDF)

QE VCO Frequency = *ce_clk* × VCO divider × (1 + CEPDF)

21.4 Suggested PLL Configurations

To simplify the PLL configurations, the device might be separated into two clock domains. The first domain contains the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine block PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. This table shows suggested PLL configurations for 33 and 66 MHz input clocks and illustrates each of the clock domains separately. Any combination of clock domains setting with same input clock are valid. Refer to Section 21, "Clocking," for the appropriate operating frequencies for your device.

Table 76. Suggested PLL Configurations

Conf No.[1]	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock Freq (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
33 MHz CLKIN/PCI_SYNC_IN Options											
s1	**0100**	**0000100**	æ	æ	33	133	266	—	∞	∞	∞
s2	**0100**	**0000101**	æ	æ	33	133	333	—	∞	∞	∞
s3	**0101**	**0000100**	æ	æ	33	166	333	—	∞	∞	∞
s4	**0101**	**0000101**	æ	æ	33	166	416	—	—	∞	∞
s5	**0110**	**0000100**	æ	æ	33	200	400	—	∞	∞	∞
s6	**0110**	**0000110**	æ	æ	33	200	600	—	—	—	∞
s7	**0111**	**0000011**	æ	æ	33	233	350	—	∞	∞	∞
s8	**0111**	**0000100**	æ	æ	33	233	466	—	—	∞	∞
s9	**0111**	**0000101**	æ	æ	33	233	583	—	—	—	∞
s10	**1000**	**0000011**	æ	æ	33	266	400	—	∞	∞	∞
s11	**1000**	**0000100**	æ	æ	33	266	533	—	—	∞	∞
s12	**1000**	**0000101**	æ	æ	33	266	667	—	—	—	∞
s13	**1001**	**0000010**	æ	æ	33	300	300	—	∞	∞	∞
s14	**1001**	**0000011**	æ	æ	33	300	450	—	—	∞	∞
s15	**1001**	**0000100**	æ	æ	33	300	600	—	—	—	∞
s16	**1010**	**0000010**	æ	æ	33	333	333	—	∞	∞	∞
s17	**1010**	**0000011**	æ	æ	33	333	500	—	—	∞	∞
s18	**1010**	**0000100**	æ	æ	33	333	667	—	—	—	∞
c1	æ	æ	**01001**	**0**	33	—	—	300	∞	∞	∞
c2	æ	æ	**01100**	**0**	33	—	—	400	∞	∞	∞
c3	æ	æ	**01110**	**0**	33	—	—	466	—	∞	∞
c4	æ	æ	**01111**	**0**	33	—	—	500	—	∞	∞

Table 76. Suggested PLL Configurations (continued)

Conf No.[1]	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock Freq (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
c5	æ	æ	**10000**	**0**	33	—	—	533	—	∞	∞
c6	æ	æ	**10001**	**0**	33	—	—	566	—	—	∞
66 MHz CLKIN/PCI_SYNC_IN Options											
s1h	**0011**	**0000110**	æ	æ	66	200	400	—	∞	∞	∞
s2h	**0011**	**0000101**	æ	æ	66	200	500	—	—	∞	∞
s3h	**0011**	**0000110**	æ	æ	66	200	600	—	—	—	∞
s4h	**0100**	**0000011**	æ	æ	66	266	400	—	∞	∞	∞
s5h	**0100**	**0000100**	æ	æ	66	266	533	—	—	∞	∞
s6h	**0100**	**0000101**	æ	æ	66	266	667	—	—	—	∞
s7h	**0101**	**0000010**	æ	æ	66	333	333	—	∞	∞	∞
s8h	**0101**	**0000011**	æ	æ	66	333	500	—	—	∞	∞
s9h	**0101**	**0000100**	æ	æ	66	333	667	—	—	—	∞
c1h	æ	æ	**00101**	**0**	66	—	—	333	∞	∞	∞
c2h	æ	æ	**00110**	**0**	66	—	—	400	∞	∞	∞
c3h	æ	æ	**00111**	**0**	66	—	—	466	—	∞	∞
c4h	æ	æ	**01000**	**0**	66	—	—	533	—	∞	∞
c5h	æ	æ	**01001**	**0**	66	—	—	600	—	—	∞

Note:

1. The Conf No. consist of prefix, an index and a postfix. The prefix “s” and “c” stands for “syset” and “ce” respectively. The postfix “h” stands for “high input clock.”"The index is a serial number.

The following steps describe how to use above table. See Example 1.

2. Choose the up or down sections in the table according to input clock rate 33 MHz or 66 MHz.
3. Select a suitable CSB and core clock rates from Table 76. Copy the SPMF and CORE PLL configuration bits.
4. Select a suitable QUICC Engine block clock rate from Table 76. Copy the CEPMF and CEPDF configuration bits.
5. Insert the chosen SPMF, COREPLL, CEPMF and CEPDF to the RCWL fields, respectively.

Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-millennium.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Interface material vendors include the following:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

22.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb force (4.5 kg force). If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.