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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8360zualfha

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core and PLL supply voltage for MPC8358 Device Part Number with Processor Frequency label of AD=266MHz and AG=400MHz & QUICC Engine Frequency label of E=300MHz & G=400MHz MPC8360 Device Part Number with Processor Frequency label of AG=400MHz and AJ=533MHz & QUICC Engine Frequency label of G=400MHz		V_{DD} & AV_{DD}	–0.3 to 1.32	V	—
Core and PLL supply voltage for MPC8360 device Part Number with Processor Frequency label of AL=667MHz and QUICC Engine Frequency label of H=500MHz		V_{DD} & AV_{DD}	–0.3 to 1.37	V	—
DDR and DDR2 DRAM I/O voltage DDR DDR2		GV_{DD}	 –0.3 to 2.75 –0.3 to 1.89	V	—
Three-speed Ethernet I/O, MII management voltage		LV_{DD}	–0.3 to 3.63	V	—
PCI, local bus, DUART, system control and power management, I^2C, SPI, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	4, 5
	Local bus, DUART, CLKIN, system control and power management, I^2C, SPI, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3, 5
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6

2.2.1 Power-Up Sequencing

MPC8360E/58E does not require the core supply voltage (V_{DD} and AV_{DD}) and I/O supply voltages (GV_{DD}, LV_{DD}, and OV_{DD}) to be applied in any particular order. During the power ramp up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there may be a period of time that all input and output pins are actively be driven and cause contention and excessive current from 3A to 5A. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD}, LV_{DD}, and OV_{DD}) and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V, see this figure.

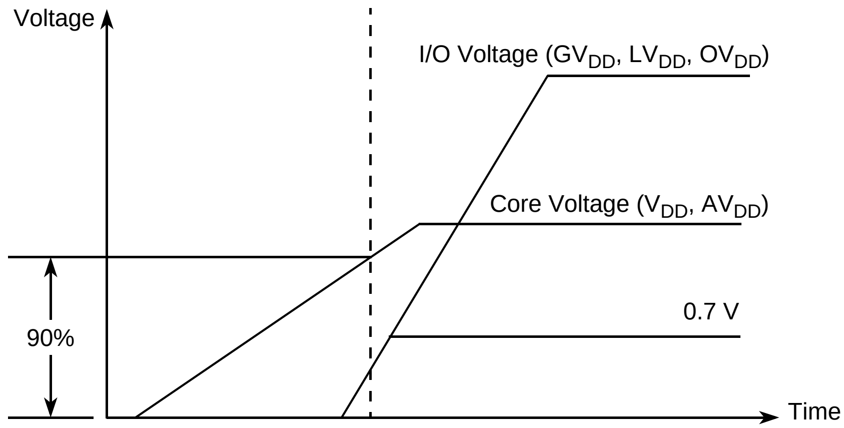

Figure 5. Power Sequencing Example

I/O voltage supplies (GV_{DD}, LV_{DD}, and OV_{DD}) do not have any ordering requirements with respect to one another.

2.2.2 Power-Down Sequencing

The MPC8360E/58E does not require the core supply voltage and I/O supply voltages to be powered down in any particular order.

3 Power Characteristics

The estimated typical power dissipation values are shown in these tables.

Table 4. MPC8360E TBGA Core Power Dissipation[1]

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	500	5.0	5.6	W	2, 3, 5
400	266	400	4.5	5.0	W	2, 3, 4
533	266	400	4.8	5.3	W	2, 3, 4
667	333	400	5.8	6.3	W	3, 6, 7, 8
500	333	500	5.9	6.4	W	3, 6, 7, 8

5.2 RESET AC Electrical Characteristics

This section describes the AC electrical specifications for the reset initialization timing requirements of the device. This table provides the reset initialization AC timing specifications for the DDR SDRAM component(s).

Table 11. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{HRESET}$ or $\overline{SRESET}$ (input) to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{PORESET}$ with stable clock applied to CLKIN when the device is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{PORESET}$ with stable clock applied to PCI_SYNC_IN when the device is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{HRESET}$/$\overline{SRESET}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{HRESET}$ negation to $\overline{SRESET}$ negation (output)	16	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{PORESET}$ when the device is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{PORESET}$ when the device is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR config signals with respect to negation of $\overline{HRESET}$	0	—	ns	—
Time for the device to turn off POR config signals with respect to the assertion of $\overline{HRESET}$	—	4	ns	3
Time for the device to turn on POR config signals with respect to the negation of $\overline{HRESET}$	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. Refer *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the device is in PCI host mode. Refer *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
3. POR config signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

This table provides the PLL and DLL lock times.

Table 12. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	µs	—
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 21, "Clocking," for more information.

8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.2.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 29. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX} t_{MTKHDV}	1 —	5	— 15	ns
TX_CLK data clock rise time, (20% to 80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall time, (80% to 20%)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the MII transmit AC timing diagram.

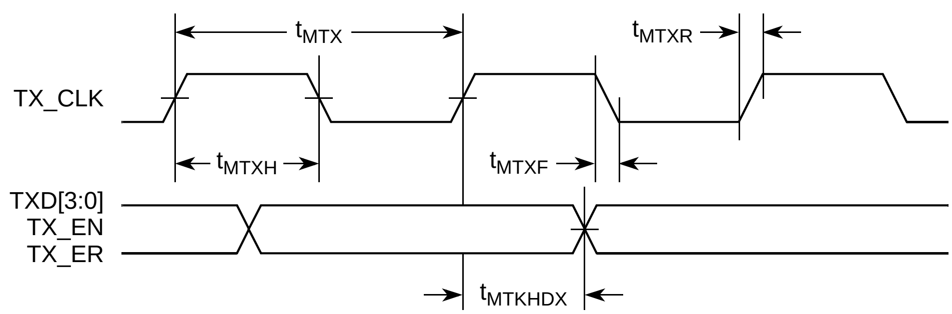

Figure 12. MII Transmit AC Timing Diagram

Table 32. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise time	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{(first\ three\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load.

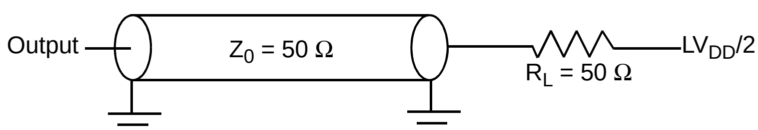

Figure 16. AC Test Load

This figure shows the RMII receive AC timing diagram.

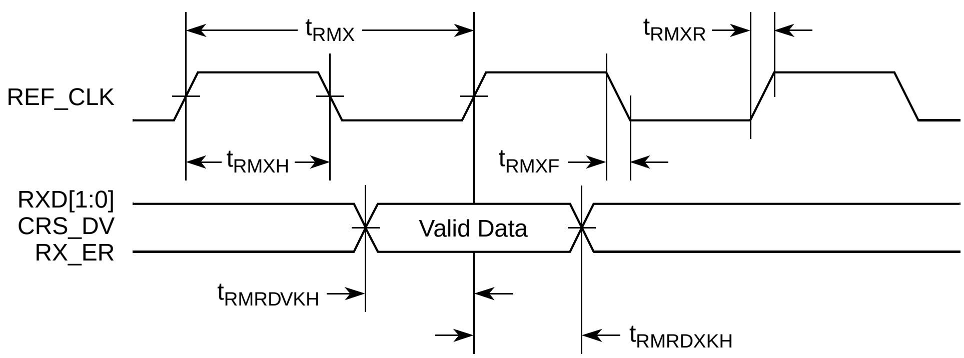

Figure 17. RMII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.3.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 37. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	$t_{MDTKHDX}$ $t_{MDTKHDV}$	10 —	—	— 110	ns	3
MDIO to MDC setup time	$t_{MDRDVKH}$	10	—	—	ns	—
MDIO to MDC hold time	$t_{MDRDXKH}$	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDRDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
3. This parameter is dependent on the ce_clk speed (that is, for a ce_clk of 200 MHz, the delay is 90 ns and for a ce_clk of 300 MHz, the delay is 63 ns).

This figure shows the MII management AC timing diagram.

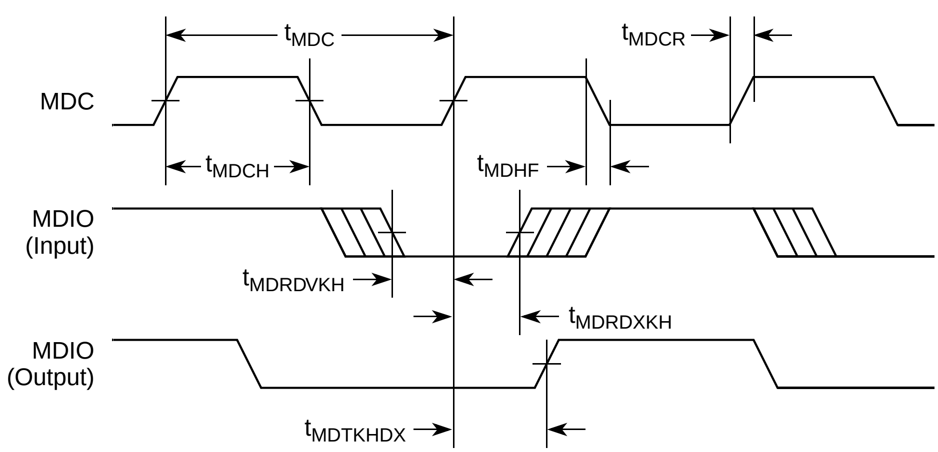

Figure 21. MII Management Interface Timing Diagram

Table 40. Local Bus General Timing Parameters—DLL Enabled (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3.0	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to LALE rise	t_{LBKHLR}	—	4.5	ns	—
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	4.5	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	4.5	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	4.5	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	1.0	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	1.0	—	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	3.8	ns	8

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to rising edge of LSYNC_IN.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This table describes the general timing parameters of the local bus interface of the device.

Table 41. Local Bus General Timing Parameters—DLL Bypass Mode[9]

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7

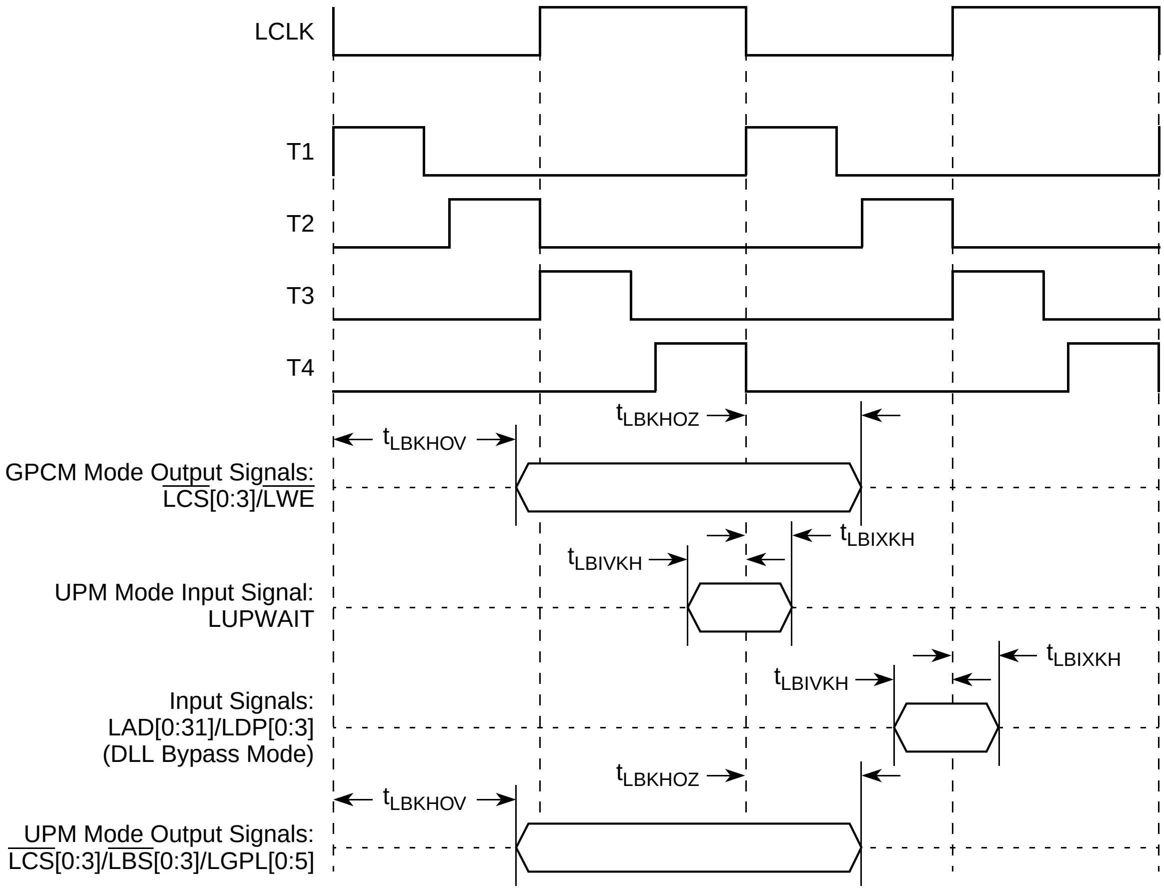

Figure 27. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (DLL Bypass Mode)

10.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device.

This table provides the JTAG AC timing specifications as defined in Figure 30 through Figure 33.

Table 43. JTAG AC Timing Specifications (Independent of CLKIN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock duty cycle	t_{JTKHKL}/t_{JTG}	45	55	%	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	t_{JTDVKH} t_{JTIVKH}	4 4	— —	ns	4
Input hold times: Boundary-scan data TMS, TDI	t_{JTDXKH} t_{JTIXKH}	10 10	— —	ns	4
Valid times: Boundary-scan data TDO	t_{JTKLDV} t_{JTKLOV}	2 2	11 11	ns	5
Output hold times: Boundary-scan data TDO	t_{JTKLDX} t_{JTKLOX}	2 2	— —	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	t_{JTKLDZ} t_{JTKLOZ}	2 2	19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 22). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

18.3 AC Test Load

These figures represent the AC timing from Table 62 and Table 63. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the timing with external clock.

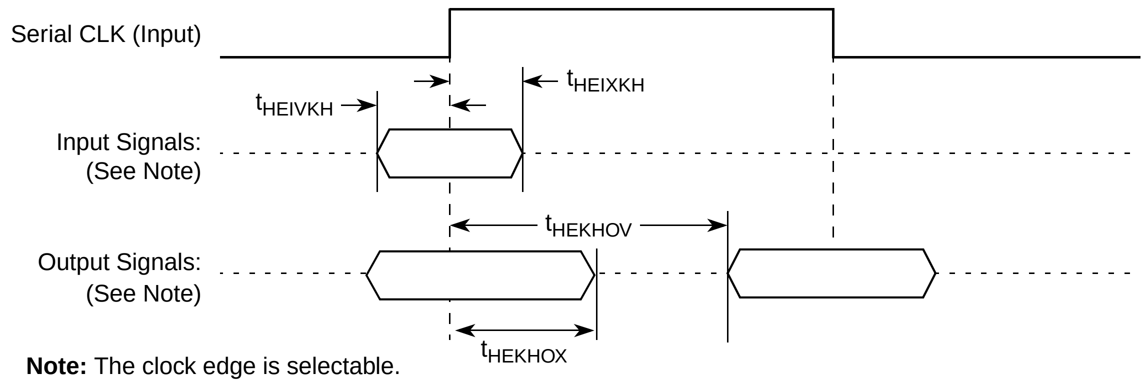

Figure 50. AC Timing (External Clock) Diagram

This figure shows the timing with internal clock.

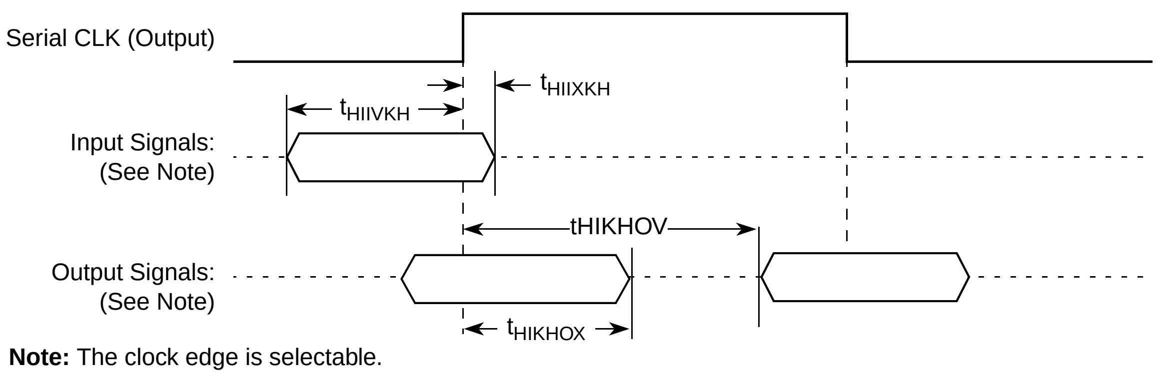

Figure 51. AC Timing (Internal Clock) Diagram

20.3 Pinout Listings

Refer to AN3097, “MPC8360/MPC8358E PowerQUICC Design Checklist,” for proper pin termination and usage.

This table shows the pin list of the MPC8360E TBGA package.

Table 66. MPC8360E TBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Primary DDR SDRAM Memory Controller Interface				
MEMC1_MDQ[0:31]	AJ34, AK33, AL33, AL35, AJ33, AK34, AK32, AM36, AN37, AN35, AR34, AT34, AP37, AP36, AR36, AT35, AP34, AR32, AP32, AM31, AN33, AM34, AM33, AM30, AP31, AM27, AR30, AT32, AN29, AP29, AN27, AR29	I/O	GV_{DD}	—
MEMC1_MDQ[32:63]/ MEMC2_MDQ[0:31]	AN8, AN7, AM8, AM6, AP9, AN9, AT7, AP7, AU6, AP6, AR4, AR3, AT6, AT5, AR5, AT3, AP4, AM5, AP3, AN3, AN5, AL5, AN4, AM2, AL2, AH5, AK3, AJ2, AJ3, AH4, AK4, AH3	I/O	GV_{DD}	—
MEMC1_MECC[0:4]/ MSRCID[0:4]	AP24, AN22, AM19, AN19, AM24	I/O	GV_{DD}	—
MEMC1_MECC[5]/ MDVAL	AM23	I/O	GV_{DD}	—
MEMC1_MECC[6:7]	AM22, AN18	I/O	GV_{DD}	—
MEMC1_MDM[0:3]	AL36, AN34, AP33, AN28	O	GV_{DD}	—
MEMC1_MDM[4:7]/ MEMC2_MDM[0:3]	AT9, AU4, AM3, AJ6	O	GV_{DD}	—
MEMC1_MDM[8]	AP27	O	GV_{DD}	—
MEMC1_MDQS[0:3]	AK35, AP35, AN31, AM26	I/O	GV_{DD}	—
MEMC1_MDQS[4:7]/ MEMC2_MDQS[0:3]	AT8, AU3, AL4, AJ5	I/O	GV_{DD}	—
MEMC1_MDQS[8]	AP26	I/O	GV_{DD}	—
MEMC1_MBA[0:1]	AU29, AU30	O	GV_{DD}	—
MEMC1_MBA[2]	AT30	O	GV_{DD}	—
MEMC1_MA[0:14]	AU21, AP22, AP21, AT21, AU25, AU26, AT23, AR26, AU24, AR23, AR28, AU23, AR22, AU20, AR18	O	GV_{DD}	—
MEMC1_MODT[0:1]	AG33, AJ36	O	GV_{DD}	6
MEMC1_MODT[2:3]/ MEMC2_MODT[0:1]	AT1, AK2	O	GV_{DD}	6
$\overline{\text{MEMC1\_MWE}}$	AT26	O	GV_{DD}	—
$\overline{\text{MEMC1\_MRAS}}$	AT29	O	GV_{DD}	—
$\overline{\text{MEMC1\_MCAS}}$	AT24	O	GV_{DD}	—
$\overline{\text{MEMC1\_MCS}}$[0:1]	AU27, AT27	O	GV_{DD}	—
$\overline{\text{MEMC1\_MCS}}$[2:3]/ $\overline{\text{MEMC2\_MCS}}$[0:1]	AU8, AU7	O	GV_{DD}	—

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_DEVSEL/CE_PF[16]	E26	I/O	OV_{DD}	5
PCI_IDSEL/CE_PF[17]	F22	I/O	OV_{DD}	—
PCI_SERR/CE_PF[18]	B29	I/O	OV_{DD}	5
PCI_PERR/CE_PF[19]	A29	I/O	OV_{DD}	5
PCI_REQ[0]/CE_PF[20]	F19	I/O	$LV_{DD}2$	—
PCI_REQ[1]/CPCI_HS_ES/ CE_PF[21]	A21	I/O	$LV_{DD}2$	—
PCI_REQ[2]/CE_PF[22]	C21	I/O	$LV_{DD}2$	—
PCI_GNT[0]/CE_PF[23]	E20	I/O	$LV_{DD}2$	—
PCI_GNT[1]/CPCI1_HS_LED/ CE_PF[24]	B20	I/O	$LV_{DD}2$	—
PCI_GNT[2]/CPCI1_HS_ENUM/ CE_PF[25]	C20	I/O	$LV_{DD}2$	—
PCI_MODE	D36	I	OV_{DD}	—
M66EN/CE_PF[4]	B37	I/O	OV_{DD}	—
Local Bus Controller Interface				
LAD[0:31]	N32, N33, N35, N36, P37, P32, P34, R36, R35, R34, R33, T37, T35, T34, T33, U37, T32, U36, U34, V36, V35, W37, W35, V33, V32, W34, Y36, W32, AA37, Y33, AA35, AA34	I/O	OV_{DD}	—
LDP[0]/CKSTOP_OUT	AB37	I/O	OV_{DD}	—
LDP[1]/CKSTOP_IN	AB36	I/O	OV_{DD}	—
LDP[2]/LCS[6]	AB35	I/O	OV_{DD}	—
LDP[3]/LCS[7]	AA33	I/O	OV_{DD}	—
LA[27:31]	AC37, AA32, AC36, AC34, AD36	O	OV_{DD}	—
LCS[0:5]	AD33, AG37, AF34, AE33, AD32, AH37	O	OV_{DD}	—
LWE[0:3]/LSDDQM[0:3]/LBS[0:3]	AG35, AG34, AH36, AE32	O	OV_{DD}	—
LBCTL	AD35	O	OV_{DD}	—
LALE	M37	O	OV_{DD}	—
LGPL0/LSDA10/cfg_reset_source0	AB32	I/O	OV_{DD}	—
LGPL1/LSDWE/cfg_reset_source1	AE37	I/O	OV_{DD}	—
LGPL2/LSDRAS/LOE	AC33	O	OV_{DD}	—
LGPL3/LSDCAS/cfg_reset_source2	AD34	I/O	OV_{DD}	—
LGPL4/LGTA/LUPWAIT/LPBSE	AE35	I/O	OV_{DD}	—
LGPL5/cfg_clkin_div	AF36	I/O	OV_{DD}	—
LCKE	G36	O	OV_{DD}	—
LCLK[0]	J33	O	OV_{DD}	—
LCLK[1]/LCS[6]	J34	O	OV_{DD}	—

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LCLK[2]/LCS[7]	G37	O	OV_{DD}	—
LSYNC_OUT	F34	O	OV_{DD}	—
LSYNC_IN	G35	I	OV_{DD}	—
Programmable Interrupt Controller				
$\overline{\text{MCP\_OUT}}$	E34	O	OV_{DD}	2
$\overline{\text{IRQ0}}$/$\overline{\text{MCP\_IN}}$	C37	I	OV_{DD}	—
$\overline{\text{IRQ}}$[1]/M1SRCID[4]/M2SRCID[4]/ LSRCID[4]	F35	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[2]/M1DVAL/M2DVAL/LDVAL	F36	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[3]/CORE_SRESET	H34	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[4:5]	G33, G32	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[6]/$\overline{\text{LCS}}$[6]/$\overline{\text{CKSTOP\_OUT}}$	E35	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[7]/$\overline{\text{LCS}}$[7]/$\overline{\text{CKSTOP\_IN}}$	H36	I/O	OV_{DD}	—
DUART				
UART1_SOUT/M1SRCID[0]/ M2SRCID[0]/LSRCID[0]	E32	O	OV_{DD}	—
UART1_SIN/M1SRCID[1]/ M2SRCID[1]/LSRCID[1]	B34	I/O	OV_{DD}	—
$\overline{\text{UART1\_CTS}}$/M1SRCID[2]/ M2SRCID[2]/LSRCID[2]	C34	I/O	OV_{DD}	—
$\overline{\text{UART1\_RTS}}$/M1SRCID[3]/ M2SRCID[3]/LSRCID[3]	A35	O	OV_{DD}	—
I^2C Interface				
IIC1_SDA	D34	I/O	OV_{DD}	2
IIC1_SCL	B35	I/O	OV_{DD}	2
IIC2_SDA	E33	I/O	OV_{DD}	2
IIC2_SCL	C35	I/O	OV_{DD}	2
QUICC Engine Block				
CE_PA[0]	F8	I/O	LV_{DD0}	—
CE_PA[1:2]	AH1, AG5	I/O	OV_{DD}	—
CE_PA[3:7]	F6, D4, C3, E5, A3	I/O	$LV_{DD}0$	—
CE_PA[8]	AG3	I/O	OV_{DD}	—
CE_PA[9:12]	F7, B3, E6, B4	I/O	$LV_{DD}0$	—
CE_PA[13:14]	AG1, AF6	I/O	OV_{DD}	—
CE_PA[15]	B2	I/O	$LV_{DD}0$	—
CE_PA[16]	AF4	I/O	OV_{DD}	—
CE_PA[17:21]	B16, A16, E17, A17, B17	I/O	$LV_{DD}1$	—

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
CE_PB[0:27]	AE2, AE1, AD5, AD3, AD2, AC6, AC5, AC4, AC2, AC1, AB5, AB4, AB3, AB1, AA6, AA4, AA2, Y6, Y4, Y3, Y2, Y1, W6, W5, W2, V5, V3, V2	I/O	OV_{DD}	—
CE_PC[0:1]	V1, U6	I/O	OV_{DD}	
CE_PC[2:3]	C16, A15	I/O	$LV_{DD}1$	—
CE_PC[4:6]	U4, U3, T6	I/O	OV_{DD}	—
CE_PC[7]	C19	I/O	$LV_{DD}2$	—
CE_PC[8:9]	A4, C5	I/O	$LV_{DD}0$	—
CE_PC[10:30]	T5, T4, T2, T1, R5, R3, R1, C11, D12, F13, B10, C10, E12, A9, B8, D10, A14, E15, B14, D15, AH2	I/O	OV_{DD}	—
CE_PD[0:27]	E11, D9, C8, F11, A7, E9, C7, A6, F10, B6, D7, E8, B5, A5, C2, E4, F5, B1, D2, G5, D1, E2, H6, F3, E1, F2, G3, H4	I/O	OV_{DD}	—
CE_PE[0:31]	K3, J2, F1, G2, J5, H3, G1, H2, K6, J3, K5, K4, L6, P6, P4, P3, P1, N4, N5, N2, N1, M2, M3, M5, M6, L1, L2, L4, E14, C13, C14, B13	I/O	OV_{DD}	—
CE_PF[0:3]	F14, D13, A12, A11	I/O	OV_{DD}	—
Clocks				
PCI_CLK_OUT[0]/CE_PF[26]	B22	I/O	$LV_{DD}2$	—
PCI_CLK_OUT[1:2]/CE_PF[27:28]	D22, A23	I/O	OV_{DD}	—
CLKIN	E37	I	OV_{DD}	—
PCI_CLOCK/PCI_SYNC_IN	M36	I	OV_{DD}	—
PCI_SYNC_OUT/CE_PF[29]	D37	I/O	OV_{DD}	3
JTAG				
TCK	K33	I	OV_{DD}	—
TDI	K34	I	OV_{DD}	4
TDO	H37	O	OV_{DD}	3
TMS	J36	I	OV_{DD}	4
$\overline{\text{TRST}}$	L32	I	OV_{DD}	4
Test				
TEST	L35	I	OV_{DD}	7
$\overline{\text{TEST\_SEL}}$	AU34	I	GV_{DD}	10
PMC				
$\overline{\text{QUIESCE}}$	B36	O	OV_{DD}	—
System Control				

This figure shows the internal distribution of clocks within the MPC8358E.

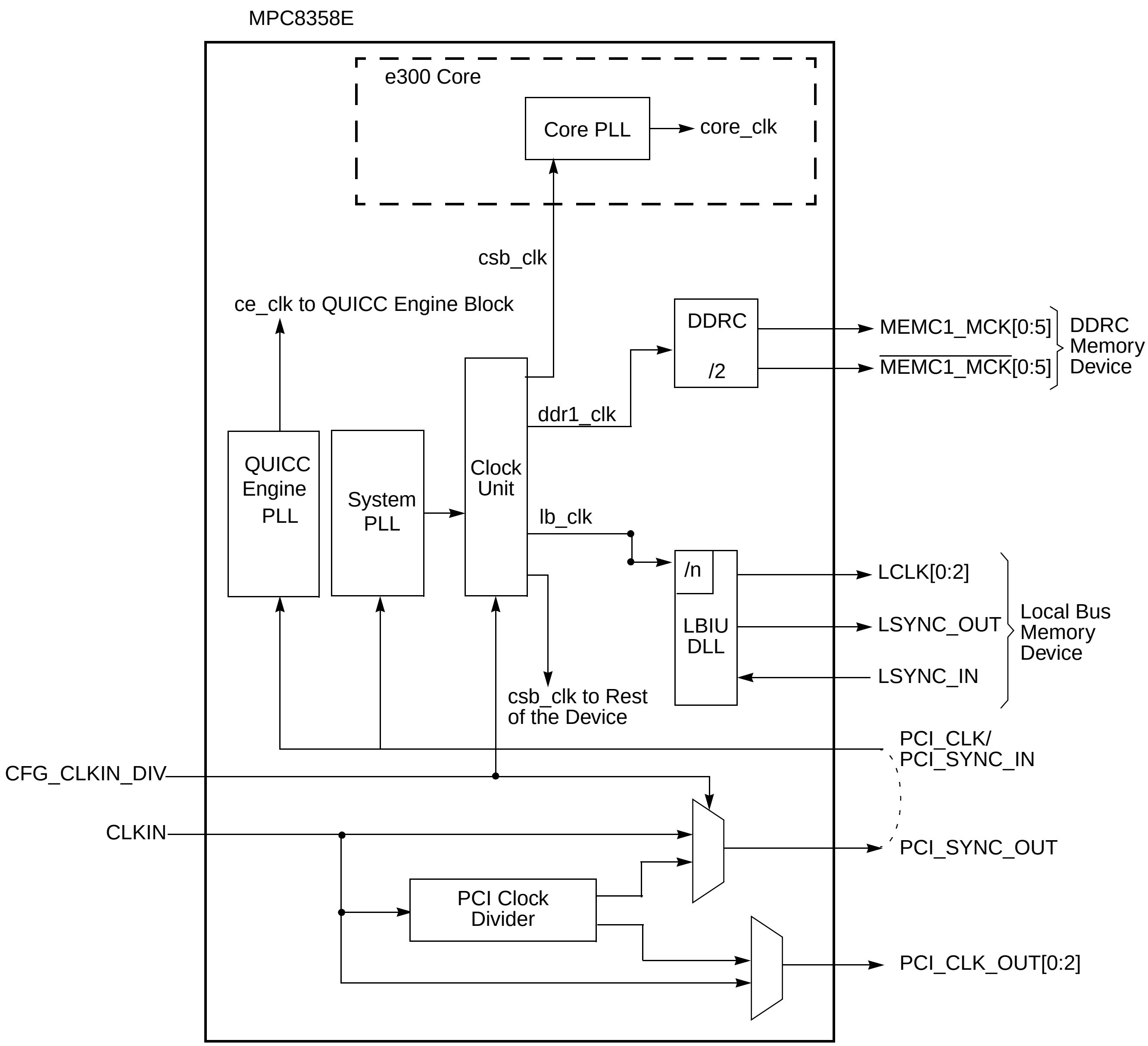

Figure 55. MPC8358E Clock Subsystem

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Note that in PCI host mode, the primary clock input also depends on whether PCI clock outputs are selected with RCWH[PCICKDRV]. When the device is configured as a PCI host device (RCWH[PCIHOST] = 1) and PCI clock output is selected (RCWH[PCICKDRV] = 1), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCIOEN*n*] parameters enable the PCI_CLK_OUT*n*, respectively.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input

Table 77. Package Thermal Characteristics for the TBGA Package (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-package natural convection on top	ψ_{JT}	1	°C/W	6

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and SEMI G38-87 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal. 1 m/sec is approximately equal to 200 linear feet per minute (LFM).
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

22.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See Table 6 for typical power dissipations values.

22.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (° C)

T_A = ambient temperature for the package (° C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (° C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

22.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. Additionally, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device. At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (° C)

T_B = board temperature at the package perimeter (° C)

$R_{\theta JA}$ = junction to board thermal resistance (° C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

22.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (° C)

T_T = thermocouple temperature on top of package (° C)

Ψ_{JT} = junction-to-ambient thermal resistance (° C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

22.2.4 Heat Sinks and Junction-to-Ambient Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (° C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (° C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (° C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-millennium.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Interface material vendors include the following:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

22.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb force (4.5 kg force). If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

22.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_J = junction temperature (° C)

T_C = case temperature of the package (° C)

$R_{\theta JC}$ = junction to case thermal resistance (° C/W)

P_D = power dissipation (W)

23 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8360E/58E. Additional information can be found in *MPC8360E/MPC8358E PowerQUICC Design Checklist* (AN3097).

23.1 System Clocking

The device includes two PLLs, as follows.

- The platform PLL ($AV_{DD}1$) generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in Section 21.1, "System PLL Configuration."
- The e300 core PLL ($AV_{DD}2$) generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 21.2, "Core PLL Configuration."

23.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins ($AV_{DD}1$, $AV_{DD}2$, respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in Figure 56, one to each of the five AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Table 81. SVR Settings (continued)

Device	Package	SVR (Rev. 2.0)	SVR (Rev. 2.1)
MPC8358E	TBGA	0x804A_0020	0x804A_0021
MPC8358	TBGA	0x804B_0020	0x804B_0021

25 Document Revision History

This table provides a revision history for this document.

Table 82. Revision History

Rev. Number	Date	Substantive Change(s)
5	09/2011	• Section 2.2.1, "Power-Up Sequencing", added the current limitation "3A to 5A" for the excessive current. • Section 2.1.2, "Power Supply Voltage Specification, Updated the Characteristic for TBGA (MPC8358 & MPC8360 Device) with specific frequency for Core and PLL voltages. • Added table footnote 3 to Table 2. • Applied table footnotes 1 and 2 to Table 10. • Removed table footnotes from Table 19. • Applied table footnote 8 to the last row of Table 40. • Applied table footnotes 8 and 9 to Table 41. • Applied table footnotes 2and 3 to Table 45. • Removed table footnotes from Table 46. • Applied table footnote to last three rows of Table 65.
4	01/2011	• Updated references to the LCRR register throughout • Removed references to DDR DLL mode in Section 6.2.2, "DDR and DDR2 SDRAM Output AC Timing Specifications." • Changed "Junction-to-Case" to "Junction-to-Ambient" in Section 22.2.4, "Heat Sinks and Junction-to-Ambient Thermal Resistance," and Table 78, "Heat Sinks and Junction-to-Ambient Thermal Resistance of TBGA Package," titles.