NXP USA Inc. - MPC8358EVVADDE Datasheet





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Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8358evvadde

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RESET DC Electrical Characteristics

Table 9. GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV (continued)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
GTX_CLK rise and fall time $\label{eq:VDD} \begin{array}{l} \text{LV}_{\text{DD}} = 2.5 \text{ V} \\ \text{LV}_{\text{DD}} = 3.3 \text{ V} \end{array}$	t _{G125R} /t _{G125F}	—	_	0.75 1.0	ns	1
GTX_CLK125 duty cycle GMII & TBI 1000Base-T for RGMII & RTBI	t _{G125H} /t _{G125}	45 47	—	55 53	%	2
GTX_CLK125 jitter	—	—	—	±150	ps	2

Notes:

- 1. Rise and fall times for GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
- GTX_CLK125 is used to generate the GTX clock for the UCC Ethernet transmitter with 2% degradation. The GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by GTX_CLK. See Section 8.2.2, "MII AC Timing Specifications," Section 8.2.3, "RMII AC Timing Specifications," and Section 8.2.5, "RGMII and RTBI AC Timing Specifications" for the duty cycle for 10Base-T and 100Base-T reference clock.

5 **RESET Initialization**

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8360E/58E.

5.1 **RESET DC Electrical Characteristics**

This table provides the DC electrical characteristics for the RESET pins of the device.

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V _{IH}	_	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	_	-0.3	0.8	V
Input current	I _{IN}	_	_	±10	μA
Output high voltage	V _{OH} ²	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V

Table 10. RESET Pins DC Electrical Characteristics ¹

Notes:

1. This table applies for pins PORESET, HRESET, SRESET, and QUIESCE.

2. HRESET and SRESET are open drain pins, thus V_{OH} is not relevant for those pins.



5.2 **RESET AC Electrical Characteristics**

This section describes the AC electrical specifications for the reset initialization timing requirements of the device. This table provides the reset initialization AC timing specifications for the DDR SDRAM component(s).

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of HRESET or SRESET (input) to activate reset flow	32	_	t _{PCI_SYNC_IN}	1
Required assertion time of PORESET with stable clock applied to CLKIN when the device is in PCI host mode	32		^t CLKIN	2
Required assertion time of PORESET with stable clock applied to PCI_SYNC_IN when the device is in PCI agent mode	32	_	^t PCI_SYNC_IN	1
HRESET/SRESET assertion (output)	512	_	t _{PCI_SYNC_IN}	1
HRESET negation to SRESET negation (output)	16	-	t _{PCI_SYNC_IN}	1
Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the device is in PCI host mode	4	_	^t CLKIN	2
Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the device is in PCI agent mode	4	_	^t PCI_SYNC_IN	1
Input hold time for POR config signals with respect to negation of HRESET	0	-	ns	_
Time for the <u>device to</u> turn off POR config signals with respect to the assertion of HRESET		4	ns	3
Time for the device to turn on POR config signals with respect to the negation of HRESET	1	_	^t PCI_SYNC_IN	1, 3

Table 11. RESET Initialization Timing Specifications

Notes:

- t_{PCI_SYNC_IN} is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. Refer MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual for more details.
- t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the device is in PCI host mode. Refer MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual for more details.
- 3. POR config signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

This table provides the PLL and DLL lock times.

Table 12. PLL and DLL Lock Times

Parameter/Condition	Min Max		Unit	Notes
PLL lock times	—	100	μs	
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.

2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 21, "Clocking," for more information.



DDR and DDR2 SDRAM AC Electrical Characteristics

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 21 and Table 22 provide the output AC timing specifications and measurement conditions for the DDR and DDR2 SDRAM interface.

Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter ⁸	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time, (MCK[n]/MCK[n] crossing)	t _{MCK}	6	10	ns	2
Skew between any MCK to ADDR/CMD 333 MHz 266 MHz 200 MHz	t _{AOSKEW}	-1.0 -1.1 -1.2	0.2 0.3 0.4	ns	3
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz 200 MHz	^t DDKHAS	2.1 2.8 3.5	_	ns	4
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz—DDR1 266 MHz—DDR2 200 MHz	t _{ddkhax}	2.0 2.7 2.8 3.5		ns	4
MCS(n) output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t _{DDKHCS}	2.1 2.8 3.5	_	ns	4
MCS(n) output hold with respect to MCK 333 MHz 266 MHz 200 MHz	t _{DDKHCX}	2.0 2.7 3.5	_	ns	4
MCK to MDQS	t _{DDKHMH}	-0.8	0.7	ns	5, 9
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	t _{DDKHDS} , t _{DDKLDS}	0.7 1.0 1.2	_	ns	6
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	t _{DDKHDX} , t _{DDKLDX}	0.7 1.0 1.2	_	ns	6
MDQS preamble start	t _{DDKHMP}	$-0.5\timest_{MCK}-0.6$	$-0.5\timest_{\text{MCK}}\text{+}0.6$	ns	7



GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

Table 32. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with $\text{LV}_{\text{DD}}/\text{OV}_{\text{DD}}$ of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	t _{RMRDVKH}	4.0	_	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	t _{RMRDXKH}	2.0	_	—	ns
REF_CLK clock rise time	t _{RMXR}	1.0	_	4.0	ns
REF_CLK clock fall time	t _{RMXF}	1.0	_	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first three letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{RMRDVKH} symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, t_{RMRDXKL} symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}

This figure provides the AC test load.



Figure 16. AC Test Load

This figure shows the RMII receive AC timing diagram.



Figure 17. RMII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.



8.2.4.1 TBI Transmit AC Timing Specifications

This table provides the TBI transmit AC timing specifications.

Table 33. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
GTX_CLK clock period	t _{TTX}	_	8.0	_	ns	—
GTX_CLK duty cycle	t _{TTXH} /t _{TTX}	40	—	60	%	—
GTX_CLK to TBI data TCG[9:0] delay	t _{TTKHDX} t _{TTKHDV}	1.0	—	 5.0	ns	3
GTX_CLK clock rise time, (20% to 80%)	t _{TTXR}	_	—	1.0	ns	—
GTX_CLK clock fall time, (80% to 20%)	t _{TTXF}	_	_	1.0	ns	—
GTX_CLK125 reference clock period	t _{G125}	_	8.0	_	ns	2
GTX_CLK125 reference clock duty cycle	t _{G125H} /t _{G125}	45	—	55	ns	—

Notes:

- The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 2. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
- 3. In rev. 2.0 silicon, due to errata, t_{TTKHDX} minimum is 0.7 ns for UCC1. Refer to Errata QE_ENET19 in Chip Errata for the MPC8360E, Rev. 1.

This figure shows the TBI transmit AC timing diagram.



Figure 18. TBI Transmit AC Timing Diagram



GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

8.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

Table 34. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
PMA_RX_CLK clock period	t _{TRX}	_	16.0	_	ns	—
PMA_RX_CLK skew	t _{SKTRX}	7.5	_	8.5	ns	—
RX_CLK duty cycle	t _{TRXH} /t _{TRX}	40	_	60	%	—
RCG[9:0] setup time to rising PMA_RX_CLK	t _{TRDVKH}	2.5	—		ns	2
RCG[9:0] hold time to rising PMA_RX_CLK	t _{trdxkh}	1.0	_	_	ns	2
RX_CLK clock rise time, $V_{IL}(min)$ to $V_{IH}(max)$	t _{TRXR}	0.7	_	2.4	ns	—
RX_CLK clock fall time, $V_{IH}(max)$ to $V_{IL}(min)$	t _{TRXF}	0.7	_	2.4	ns	—

Notes:

- 1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).}
- 2. Setup and hold time of even numbered RCG are measured from riding edge of PMA_RX_CLK1. Setup and hold time of odd numbered RCG are measured from riding edge of PMA_RX_CLK0.

This figure shows the TBI receive AC timing diagram.



Figure 19. TBI Receive AC Timing Diagram



Local Bus DC Electrical Characteristics

8.3.3 IEEE 1588 Timer AC Specifications

This table provides the IEEE 1588 timer AC specifications.

Table 38. IEEE 1588 Timer AC Specifications

Parameter	Symbol	Min	Мах	Unit	Notes
Timer clock frequency	t _{TMRCK}	0	70	MHz	1
Input setup to timer clock	t _{TMRCKS}	—	—	—	2, 3
Input hold from timer clock	t _{TMRCKH}	—	—	—	2, 3
Output clock to output valid	t _{GCLKNV}	0	6	ns	_
Timer alarm to output valid	t _{TMRAL}	_		_	2

Notes:

1. The timer can operate on rtc_clock or tmr_clock. These clocks get muxed and any one of them can be selected. The minimum and maximum requirement for both rtc_clock and tmr_clock are the same.

- 2. These are asynchronous signals.
- 3. Inputs need to be stable at least one TMR clock.

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8360E/58E.

9.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface.

Table 39. Local Bus DC Electrical Characteristics

Parameter	Symbol	Symbol Min		Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
High-level output voltage, I _{OH} = −100 μA	V _{OH}	OV _{DD} - 0.4	—	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V _{OL}	—	0.2	V
Input current	I _{IN}	—	±10	μA

9.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface of the device.

Table 40. Local Bus General Timing Parameters—DLL Enabled

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus cycle time	t _{LBK}	7.5	_	ns	2
Input setup to local bus clock (except LUPWAIT)	t _{LBIVKH1}	1.7	_	ns	3, 4
LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.9	_	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	t _{LBIXKH1}	1.0		ns	3, 4



JTAG DC Electrical Characteristics



Figure 28. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (DLL Enabled)

10 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8360E/58E.

10.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface of the device.

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	—	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V
Input high voltage	V _{IH}	—	2.5	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	$0 V \leq V_{IN} \leq OV_{DD}$	_	±10	μA



10.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device.

This table provides the JTAG AC timing specifications as defined in Figure 30 through Figure 33.

Table 43. JTAG AC Timing Specifications (Independent of CLKIN)¹

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f _{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t _{JTG}	30	—	ns	_
JTAG external clock duty cycle	t _{JTKHKL} /t _{JTG}	45	55	%	_
JTAG external clock rise and fall times	t _{JTGR} & t _{JTGF}	0	2	ns	_
TRST assert time	t _{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	t _{JTDVKH} t _{JTIVKH}	4 4	_	ns	4
Input hold times: Boundary-scan data TMS, TDI	t _{JTDXKH} t _{JTIXKH}	10 10	_	ns	4
Valid times: Boundary-scan data TDO	t _{JTKLDV} t _{JTKLOV}	2 2	11 11	ns	5
Output hold times: Boundary-scan data TDO	t _{jtkldx} t _{jtklox}	2 2	_	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	t _{JTKLDZ} t _{JTKLOZ}	2 2	19 9	ns	5, 6

Notes:

- 2. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
- 4. Non-JTAG signal input timing with respect to t_{TCLK}.
- 5. Non-JTAG signal output timing with respect to t_{TCLK}.
- 6. Guaranteed by design and characterization.

All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 22). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.



I2C AC Electrical Specifications

11.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interface of the device.

Table 45. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 44).

Parameter	Symbol ¹	Min	Max	Unit	Note
SCL clock frequency	f _{I2C}	0	400	kHz	2
Low period of the SCL clock	t _{I2CL}	1.3	_	μs	—
High period of the SCL clock	t _{I2CH}	0.6	_	μs	—
Setup time for a repeated START condition	t _{I2SVKH}	0.6	_	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL}	0.6	_	μs	_
Data setup time	t _{I2DVKH}	100	_	ns	3
Data hold time: CBUS compatible masters I ² C bus devices	t _{I2DXKL}	$\frac{1}{0^2}$	 0.9 ³	μs	—
Rise time of both SDA and SCL signals	t _{I2CR}	20 + 0.1 C _b ⁴	300	ns	—
Fall time of both SDA and SCL signals	t _{I2CF}	20 + 0.1 C _b ⁴	300	ns	—
Set-up time for STOP condition	t _{l2PVKH}	0.6	_	μs	—
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	_	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times \text{OV}_{\text{DD}}$	_	V	_
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times \text{OV}_{\text{DD}}$	_	V	_

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional}

block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

 The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of the falling edge of SCL.

3. The maximum t_{12DVKH} has only to be met if the device does not stretch the LOW period (t_{12CL}) of the SCL signal.

4. C_B = capacitance of one bus line in pF.



Timers AC Timing Specifications

13.2 Timers AC Timing Specifications

This table provides the timer input and output AC timing specifications.

Table 50. Timers Input AC Timing Specifications¹

Characteristic	Symbol ²	Тур	Unit
Timers inputs—minimum pulse width	t _{TIWID}	20	ns

Notes:

- 1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
- 2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

This figure provides the AC test load for the timers.



Figure 39. Timers AC Test Load

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8360E/58E.

14.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the device GPIO.

Table 51. GPIO DC Electrical Characteristic

Characteristic	Symbol	Condition	Min	Мах	Unit	Notes
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	_	V	1
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V	1
Input low voltage	V _{IL}	—	-0.3	0.8	V	—
Input current	I _{IN}	0 V ≤V _{IN} ≤OV _{DD}	—	±10	μA	—

Note:

1. This specification applies when operating from 3.3-V supply.

Table 60. UTOPIA AC Timing Specifications¹ (continued)

Characteristic	Symbol ²	Min	Мах	Unit	Notes
UTOPIA inputs—Internal clock input hold time	t _{UIIXKH}	2.4	—	ns	
UTOPIA inputs—External clock input hold time	t _{UEIXKH}	1	—	ns	3

Notes:

- 1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{UIKHOX} symbolizes the UTOPIA outputs internal timing (UI) for the time t_{UTOPIA} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
 </sub>
- In rev. 2.0 silicon, due to errata, t_{UEIVKH} minimum is 4.3 ns and t_{UEIXKH} minimum is 1.4 ns under specific conditions. Refer to Errata QE_UPC3 in *Chip Errata for the MPC8360E, Rev. 1.*

This figure provides the AC test load for the UTOPIA.



Figure 46. UTOPIA AC Test Load

These figures represent the AC timing from Table 56. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the UTOPIA timing with external clock.



Figure 47. UTOPIA AC Timing (External Clock) Diagram



20 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8360E/58E is available in a tape ball grid array (TBGA), see Section 20.1, "Package Parameters for the TBGA Package," and Section 20.2, "Mechanical Dimensions of the TBGA Package," for information on the package.

20.1 Package Parameters for the TBGA Package

The package parameters for rev. 2.0 silicon are as provided in the following list. The package type is $37.5 \text{ mm} \times 37.5 \text{ mm}$, 740 tape ball grid array (TBGA).

Package outline	$37.5 \text{ mm} \times 37.5 \text{ mm}$
Interconnects	740
Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder Balls	62 Sn/36 Pb/2 Ag (ZU package)
	95.5 Sn/0.5 Cu/4Ag (VV package)
Ball diameter (typical)	0.64 mm



Pinout Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC1_MCKE[0:1]	AL32, AU33	0	GV _{DD}	3
MEMC1_MCK[0:1]	AK37, AT37	0	GV _{DD}	
MEMC1_MCK[2:3]/ MEMC2_MCK[0:1]	AN1, AR2	0	GV _{DD}	_
MEMC1_MCK[4:5]/ MEMC2_MCKE[0:1]	AN25, AK1	0	GV _{DD}	_
MEMC1_MCK[0:1]	AL37, AT36	0	GV _{DD}	_
MEMC1_MCK[2:3]/ MEMC2_MCK[0:1]	AP2, AT2	0	GV _{DD}	_
MEMC1_MCK[4]/ MEMC2_MDM[8]	AN24	0	GV _{DD}	
MEMC1_MCK[5]/ MEMC2_MDQS[8]	AL1	0	GV _{DD}	_
MDIC[0:1]	АН6, АР30	I/O	GV _{DD}	10
Sec	ondary DDR SDRAM Memory Controller Interface			
MEMC2_MECC[0:7]	AN16, AP18, AM16, AM17, AN17, AP13, AP15, AN13	I/O	GV _{DD}	_
MEMC2_MBA[0:2]	AU12, AU15, AU13	0	GV _{DD}	_
MEMC2_MA[0:14]	AT12, AP11, AT13, AT14, AR13, AR15, AR16, AT16, AT18, AT17, AP10, AR20, AR17, AR14, AR11	0	GV _{DD}	_
MEMC2_MWE	AU10	0	GV _{DD}	_
MEMC2_MRAS	AT11	0	GV _{DD}	_
MEMC2_MCAS	AU11	0	GV _{DD}	
	PCI			
PCI_INTA/IRQ_OUT/CE_PF[5]	A20	I/O	LV _{DD} 2	2
PCI_RESET_OUT/CE_PF[6]	E19	I/O	LV _{DD} 2	_
PCI_AD[31:30]/CE_PG[31:30]	D20, D21	I/O	LV _{DD} 2	
PCI_AD[29:25]/CE_PG[29:25]	A24, B23, C23, E23, A26	I/O	OV _{DD}	
PCI_AD[24]/CE_PG[24]	B21	I/O	LV _{DD} 2	_
PCI_AD[23:0]/CE_PG[23:0]	C24, C25, D25, B25, E24, F24, A27, A28, F27, A30, C30, D30, E29, B31, C31, D31, D32, A32, C33, B33, F30, E31, A34, D33	I/O	OV _{DD}	
PCI_C/BE[3:0]/CE_PF[10:7]	E22, B26, E28, F28	I/O	OV _{DD}	
PCI_PAR/CE_PF[11]	D28	I/O	OV _{DD}	
PCI_FRAME/CE_PF[12]	D26	I/O	OV _{DD}	5
PCI_TRDY/CE_PF[13]	C27	I/O	OV _{DD}	5
PCI_IRDY/CE_PF[14]	C28	I/O	OV _{DD}	5
PCI_STOP/CE_PF[15]	B28	I/O	OV _{DD}	5



Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_MODE	D36	I	OV _{DD}	
M66EN/CE_PF[4]	B37	I/O	OV _{DD}	
	Local Bus Controller Interface			
LAD[0:31]	N32, N33, N35, N36, P37, P32, P34, R36, R35, R34, R33, T37, T35, T34, T33, U37, T32, U36, U34, V36, V35, W37, W35, V33, V32, W34, Y36, W32, AA37, Y33, AA35, AA34	I/O	OV _{DD}	_
LDP[0]/CKSTOP_OUT	AB37	I/O	OV _{DD}	_
LDP[1]/CKSTOP_IN	AB36	I/O	OV _{DD}	_
LDP[2]/LCS[6]	AB35	I/O	OV _{DD}	_
LDP[3]/LCS[7]	AA33	I/O	OV _{DD}	
LA[27:31]	AC37, AA32, AC36, AC34, AD36	0	OV _{DD}	
LCS[0:5]	AD33, AG37, AF34, AE33, AD32, AH37	0	OV _{DD}	
LWE[0:3]/LSDDQM[0:3]/LBS[0:3]	AG35, AG34, AH36, AE32	0	OV _{DD}	
LBCTL	AD35	0	OV _{DD}	
LALE	M37	0	OV _{DD}	
LGPL0/LSDA10/cfg_reset_source0	AB32	I/O	OV _{DD}	
LGPL1/LSDWE/cfg_reset_source1	AE37	I/O	OV _{DD}	
LGPL2/LSDRAS/LOE	AC33	0	OV _{DD}	
LGPL3/LSDCAS/cfg_reset_source2	AD34	I/O	OV _{DD}	
LGPL4/LGTA/LUPWAIT/LPBSE	AE35	I/O	OV _{DD}	_
LGPL5/cfg_clkin_div	AF36	I/O	OV _{DD}	_
LCKE	G36	0	OV _{DD}	
LCLK[0]	J33	0	OV _{DD}	_
LCLK[1]/LCS[6]	J34	0	OV _{DD}	_
LCLK[2]/LCS[7]	G37	0	OV _{DD}	
LSYNC_OUT	F34	0	OV _{DD}	
LSYNC_IN	G35	I	OV _{DD}	
	Programmable Interrupt Controller			
MCP_OUT	E34	0	OV _{DD}	2
IRQ0/MCP_IN	C37	I	OV _{DD}	_
IRQ[1]/M1SRCID[4]/M2SRCID[4]/ LSRCID[4]	F35	I/O	OV_{DD}	
IRQ[2]/M1DVAL/M2DVAL/LDVAL	F36	I/O	OV _{DD}	_
IRQ[3]/CORE_SRESET	H34	I/O	OV_{DD}	





ordered, see Section 24.1, "Part Numbers Fully Addressed by this Document," for part ordering details and contact your Freescale sales representative or authorized distributor for more information.

Characteristic ¹	400 MHz	533 MHz	667 MHz ²	Unit
e300 core frequency (<i>core_clk</i>)	266–400	266–533	266–667	MHz
Coherent system bus frequency (<i>csb_clk</i>)	133–333		MHz	
QUICC Engine frequency ³ (<i>ce_clk</i>)	266–500		MHz	
DDR and DDR2 memory bus frequency (MCLK) ⁴	100–166.67			MHz
Local bus frequency (LCLK <i>n</i>) ⁵	16.67–133		MHz	
PCI input frequency (CLKIN or PCI_CLK)	25–66.67		MHz	
Security core maximum internal operating frequency	133	133	166	MHz

Table 69. Operating Frequencies for the TBGA Package

Notes:

- 1. The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
- 2. The 667 MHz core frequency is based on a 1.3 V V_{DD} supply voltage.
- 3. The 500 MHz QE frequency is based on a 1.3 V V_{DD} supply voltage.
- 4. The DDR data rate is 2x the DDR memory bus frequency.
- 5. The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWL[LBCM]).

21.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] and RCWL[SVCOD] parameters. This table shows the multiplication factor encodings for the system PLL.

RCWL[SPMF]	System PLL Multiplication Factor
0000	× 16
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11

Table 70. System PLL Multiplication Factors



Core PLL Configuration

21.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). This table shows the encodings for RCWL[COREPLL]. COREPLL values not listed in this table should be considered reserved.

RCWL[COREPLL]		core_clk:csb_clk	VCO dividor	
0–1	2–5	6	Ratio	
nn	0000	n	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)
00	0001	0	1:1	÷2
01	0001	0	1:1	÷4
10	0001	0	1:1	÷8
11	0001	0	1:1	÷8
00	0001	1	1.5:1	÷2
01	0001	1	1.5:1	÷4
10	0001	1	1.5:1	÷8
11	0001	1	1.5:1	÷8
00	0010	0	2:1	÷2
01	0010	0	2:1	÷4
10	0010	0	2:1	÷8
11	0010	0	2:1	÷8
00	0010	1	2.5:1	÷2
01	0010	1	2.5:1	÷4
10	0010	1	2.5:1	÷8
11	0010	1	2.5:1	÷8
00	0011	0	3:1	÷2
01	0011	0	3:1	÷4
10	0011	0	3:1	÷8
11	0011	0	3:1	÷8

Table 73. e300 Core PLL Configuration

NOTE

Core VCO frequency = Core frequency \times VCO divider. The VCO divider (RCWL[COREPLL[0:1]]) must be set properly so that the core VCO frequency is in the range of 800–1800 MHz. Having a core frequency below the CSB frequency is not a possible option because the core frequency must be equal to or greater than the CSB frequency.



Thermal Management Information

This table shows heat sinks and junction-to-ambient thermal resistance for TBGA package.

Table 78. Heat Sinks and Junction-to-Ambien	t Thermal Resistance of TBGA Package
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		35 imes 35 mm TBGA	
Heat Sink Assuming Thermal Grease	Airflow	Junction-to-Ambient Thermal Resistance	
AAVID 30 × 30 × 9.4 mm pin fin	Natural convention	10.7	
AAVID 30 × 30 × 9.4 mm pin fin	1 m/s	6.2	
AAVID 30 × 30 × 9.4 mm pin fin	2 m/s	5.3	
AAVID 31 × 35 × 23 mm pin fin	Natural convention	8.1	
AAVID 31 × 35 × 23 mm pin fin	1 m/s	4.4	
AAVID 31 × 35 × 23 mm pin fin	2 m/s	3.7	
Wakefield, 53 × 53 × 25 mm pin fin	Natural convention	5.4	
Wakefield, 53 × 53 × 25 mm pin fin	1 m/s	3.2	
Wakefield, 53 × 53 × 25 mm pin fin	2 m/s	2.4	
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural convention	6.4	
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	3.8	
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	2.5	
MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass	1 m/s	2.8	

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following:

Aavid Thermalloy 80 Commercial St.	603-224-9988
Concord, NH 03301	
Internet: www.aavidthermalloy.com	
Alpha Novatech	408-749-7601
473 Sapena Ct. #15	
Santa Clara, CA 95054	
Internet: www.alphanovatech.com	
International Electronic Research Corporation (IERC)	818-842-7277
413 North Moss St.	
Burbank, CA 91502	
Internet: www.ctscorp.com	



This figure shows the PLL power supply filter circuit.



Figure 56. PLL Power Supply Filter Circuit

23.3 Decoupling Recommendations

Due to large address and data buses as well as high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the device system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pins of the device. These decoupling capacitors should receive their power from separate V_{DD} , OV_{DD} , GV_{DD} , and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

Additionally, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , OV_{DD} , GV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μ F (AVX TPS tantalum or Sanyo OSCON).

23.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD} , GV_{DD} , or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and GND pins of the device.

23.5 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 57). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_p is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_p then becomes the resistance of the pull-up devices. R_p and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.



Table 82.	Revision	History	(continued)
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Rev. Number	Date	Substantive Change(s)
3	03/2010	 Changed references to RCWH[PCICKEN] to RCWH[PCICKDRV]. In Table 2, added extended temperature characteristics. Added Figure 6, "DDR Input Timing Diagram." In Figure 53, "Mechanical Dimensions and Bottom Surface Nomenclature of the TBGA Package," removed watermark. Updated the title of Table 19,"DDR SDRAM Input AC Timing Specifications." In Table 20, "DDR and DDR2 SDRAM Input AC Timing Specifications Mode," changed table subtitle. In Table 20, "DDR and DDR2 SDRAM Input AC Timing Specifications Mode," changed table subtitle. In Table 27–Table 30, and Table 33—Table 34, changed the rise and fall time specifications to reference 20–80% and 80–20% of the voltage supply, respectively. In Table 38, "IEEE 1588 Timer AC Specifications," changed units to "ns" for t_{I2DVKH}. In Table 45, "I2C AC Electrical Specifications," changed units to "ns" for t_{I2DVKH}. In Table 66, "MPC8360E TBGA Pinout Listing," and Table 67 "MPC8358E TBGA Pinout Listing, added note 7: "This pin must always be tied to GND" to the TEST pin and added a note to SPARE1 stating: "This pin must always be left not connected." In Section 4, "Clock Input Timing," added note regarding rise/fall time on QUICC Engine block input pins. Added Section 4.1, "injol/100/1000 Ethernet DC Electrical Characteristics." In Section 2.1, "Pinout Listing," added sentence stating "Refer to AN3097, 'MPC8360/MPC8358E PowerQUICC Design Checklist,' for proper pin termination and usage." In Section 21, "Clocking," removed statement: "The OCCR[PCICDn] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUTn signals." In Section 21.1, "System PLL Configuration," updated the system VCO frequency conditions. In Table 80, added extended temperature characteristics.
2	12/2007	Initial release.