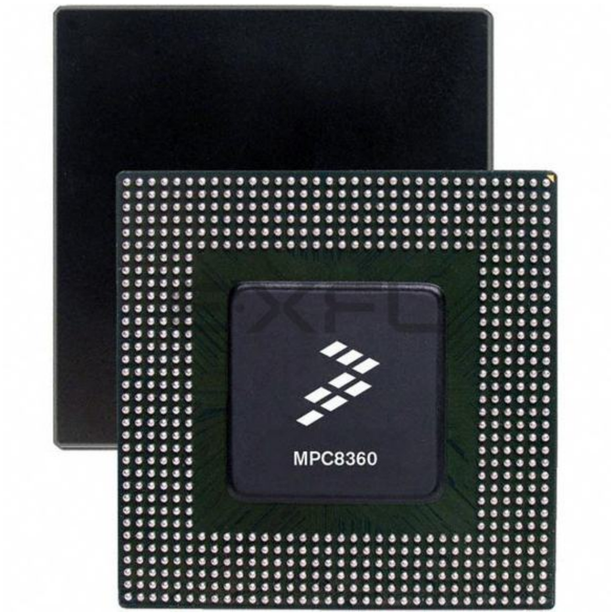
NXP USA Inc. - MPC8358EVVADDEA Datasheet



Welcome to **E-XFL.COM**

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8358evvaddea

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

- 10/100 Mbps Ethernet/IEEE Std. 802.3™ CDMA/CS interface through a media-independent interface (MII, RMII, RGMII)[1]
- 1000 Mbps Ethernet/IEEE 802.3 CDMA/CS interface through a media-independent interface (GMII, RGMII, TBI, RTBI) on UCC1 and UCC2
- 9.6-Kbyte jumbo frames
- ATM full-duplex SAR, up to 622 Mbps (OC-12/STM-4), AAL0, AAL1, and AAL5 in accordance ITU-T I.363.5
- ATM AAL2 CPS, SSSAR, and SSTED up to 155 Mbps (OC-3/STM-1) Mbps full duplex (with 4 CPS packets per cell) in accordance ITU-T I.366.1 and I.363.2
- ATM traffic shaping for CBR, VBR, UBR, and GFR traffic types compatible with ATM forum TM4.1 for up to 64-Kbyte simultaneous ATM channels
- ATM AAL1 structured and unstructured circuit emulation service (CES 2.0) in accordance with ITU-T I.163.1 and ATM Forum af-vtoa-00-0078.000
- IMA (Inverse Multiplexing over ATM) for up to 31 IMA links over 8 IMA groups in accordance with the ATM forum AF-PHY-0086.000 (Version 1.0) and AF-PHY-0086.001 (Version 1.1)
- ATM Transmission Convergence layer support in accordance with ITU-T I.432
- ATM OAM handling features compatible with ITU-T I.610
- PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686, and 3153
- IP support for IPv4 packets including TOS, TTL, and header checksum processing
- Ethernet over first mile IEEE 802.3ah
- Shim header
- Ethernet-to-Ethernet/AAL5/AAL2 inter-working
- L2 Ethernet switching using MAC address or IEEE Std. 802.1P/Q™ VLAN tags
- ATM (AAL2/AAL5) to Ethernet (IP) interworking in accordance with RFC2684 including bridging of ATM ports to Ethernet ports
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- AAL2 protocol rate up to 4 CPS at OC-3/STM-1 rate
- Packet over Sonet (POS) up to 622-Mbps full-duplex 124 MultiPHY
- POS hardware; microcode must be loaded as an IRAM package
- Transparent up to 70-Mbps full-duplex
- HDLC up to 70-Mbps full-duplex
- HDLC BUS up to 10 Mbps
- Asynchronous HDLC
- UART
- BISYNC up to 2 Mbps
- User-programmable Virtual FIFO size
- QUICC multichannel controller (QMC) for 64 TDM channels

- One multichannel communication controller (MCC) only on the MPC8360E supporting the following:
  - 256 HDLC or transparent channels
  - 128 SS7 channels
  - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces
- Two UTOPIA/POS interfaces on the MPC8360E supporting 124 MultiPHY each (optional 2*128 MultiPHY with extended address) and one UTOPIA/POS interface on the MPC8358E supporting 31/124 MultiPHY
- Two serial peripheral interfaces (SPI); SPI2 is dedicated to Ethernet PHY management

---

[1] SMII or SGMII media-independent interface is not currently supported.

This table shows the estimated typical I/O power dissipation for the device.

Table 6. Estimated Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	Unit	Comments
DDR I/O 65% utilization $R_s = 20\ \Omega$ $R_t = 50\ \Omega$ 2 pairs of clocks	200 MHz, 1 × 32 bits	0.3	0.46	—	—	—	W	—
	200 MHz, 1 × 64 bits	0.4	0.58	—	—	—	W	—
	200 MHz, 2 × 32 bits	0.6	0.92	—	—	—	W	—
	266 MHz, 1 × 32 bits	0.35	0.56	—	—	—	W	—
	266 MHz, 1 × 64 bits	0.46	0.7	—	—	—	W	—
	266 MHz, 2 × 32 bits	0.7	1.11	—	—	—	W	—
	333 MHz, 1 × 32 bits	0.4	0.65	—	—	—	W	—
	333 MHz, 1 × 64 bits	0.53	0.82	—	—	—	W	—
	333 MHz, 2 × 32 bits	0.81	1.3	—	—	—	W	—
Local Bus I/O Load = 25 pf 3 pairs of clocks	133 MHz, 32 bits	—	—	0.22	—	—	W	—
	83 MHz, 32 bits	—	—	0.14	—	—	W	—
	66 MHz, 32 bits	—	—	0.12	—	—	W	—
	50 MHz, 32 bits	—	—	0.09	—	—	W	—
PCI I/O Load = 30 pF	33 MHz, 32 bits	—	—	0.05	—	—	W	—
	66 MHz, 32 bits	—	—	0.07	—	—	W	—
10/100/1000 Ethernet I/O Load = 20 pF	MII or RMII	—	—	—	0.01	—	W	Multiply by number of interfaces used.
	GMII or TBI	—	—	—	0.04	—	W	
	RGMII or RTBI	—	—	—	—	0.04	W	
Other I/O	—	—	—	0.1	—	—	W	—

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8360E/58E.

NOTE

The rise/fall time on QUICC Engine block input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of V_{DD}; fall time refers to transitions from 90% to 10% of V_{DD}.

Table 9. GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV (continued)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
GTX_CLK rise and fall time LV_{DD} = 2.5 V LV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1
GTX_CLK125 duty cycle GMII & TBI 1000Base-T for RGMII & RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	2
GTX_CLK125 jitter	—	—	—	±150	ps	2

Notes:

1. Rise and fall times for GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
2. GTX_CLK125 is used to generate the GTX clock for the UCC Ethernet transmitter with 2% degradation. The GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by GTX_CLK. See Section 8.2.2, "MII AC Timing Specifications," Section 8.2.3, "RMII AC Timing Specifications," and Section 8.2.5, "RGMII and RTBI AC Timing Specifications" for the duty cycle for 10Base-T and 100Base-T reference clock.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8360E/58E.

5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins of the device.

Table 10. RESET Pins DC Electrical Characteristics [1]

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±10	µA
Output high voltage	V_{OH}[2]	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:

1. This table applies for pins $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, and $\overline{\text{QUIESCE}}$.
2. $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

5.2 RESET AC Electrical Characteristics

This section describes the AC electrical specifications for the reset initialization timing requirements of the device. This table provides the reset initialization AC timing specifications for the DDR SDRAM component(s).

Table 11. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the device is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the device is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$/$\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the device to turn off POR config signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the device to turn on POR config signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. Refer *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the device is in PCI host mode. Refer *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
3. POR config signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

This table provides the PLL and DLL lock times.

Table 12. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	µs	—
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 21, “Clocking,” for more information.

Table 16. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	MV_{REF} + 0.18	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.18	V	—
Output leakage current	I_{OZ}	—	±10	μA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–15.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	15.2	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	±10	μA	—
Input current ($0 V \le V_{IN} \le OV_{DD}$)	I_{IN}	—	±10	μA	—

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le GV_{DD}$.

This table provides the DDR capacitance when GV_{DD}(typ) = 2.5 V.

Table 17. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25° C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM interface when GV_{DD}(typ) = 1.8 V.

Table 18. DDR2 SDRAM Input AC Timing Specifications for GV_{DD}(typ) = 1.8 V

At recommended operating conditions with GV_{DD} of 1.8 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V	—

8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.2.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 29. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX} t_{MTKHDV}	1 —	5	— 15	ns
TX_CLK data clock rise time, (20% to 80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall time, (80% to 20%)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the MII transmit AC timing diagram.

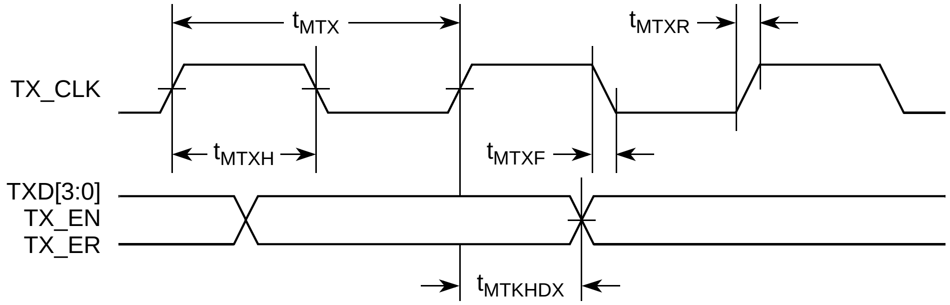


Figure 12. MII Transmit AC Timing Diagram

8.2.3 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.3.1 RMII Transmit AC Timing Specifications

This table provides the RMII transmit AC timing specifications.

Table 31. RMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$ $t_{RMTKHDV}$	2 —	—	— 10	ns
REF_CLK data clock rise time	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall time	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

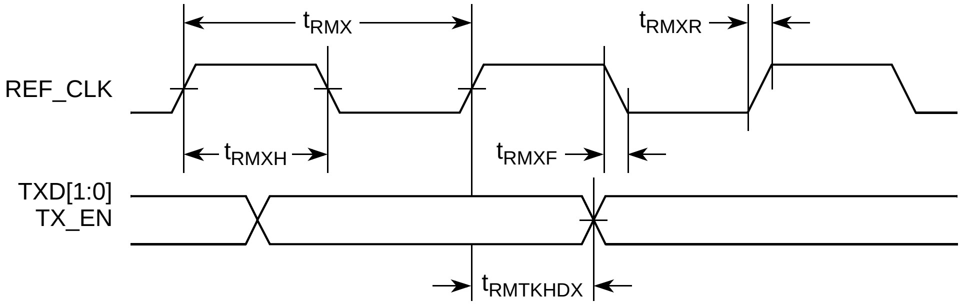


Figure 15. RMII Transmit AC Timing Diagram

8.2.3.2 RMII Receive AC Timing Specifications

This table provides the RMII receive AC timing specifications.

Table 32. RMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%

8.3.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 37. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	$t_{MDTKHDX}$ $t_{MDTKHDV}$	10 —	—	— 110	ns	3
MDIO to MDC setup time	$t_{MDRDVKH}$	10	—	—	ns	—
MDIO to MDC hold time	$t_{MDRDXKH}$	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—
MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDRDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
3. This parameter is dependent on the ce_clk speed (that is, for a ce_clk of 200 MHz, the delay is 90 ns and for a ce_clk of 300 MHz, the delay is 63 ns).

This figure shows the MII management AC timing diagram.

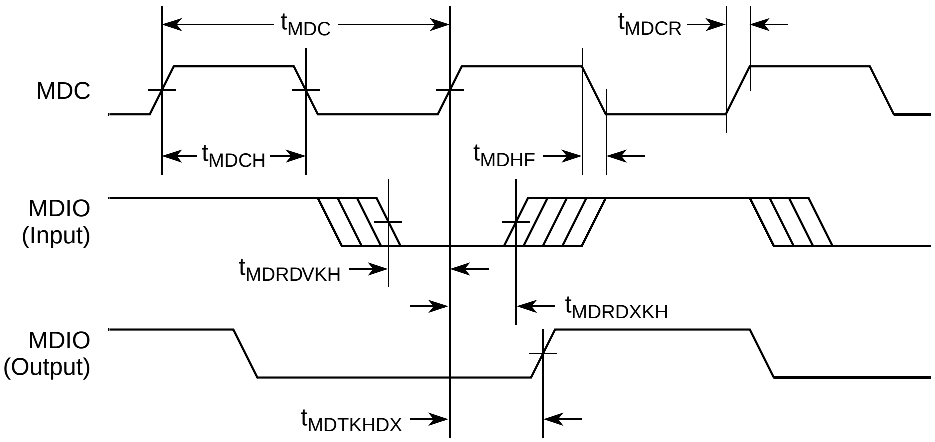


Figure 21. MII Management Interface Timing Diagram

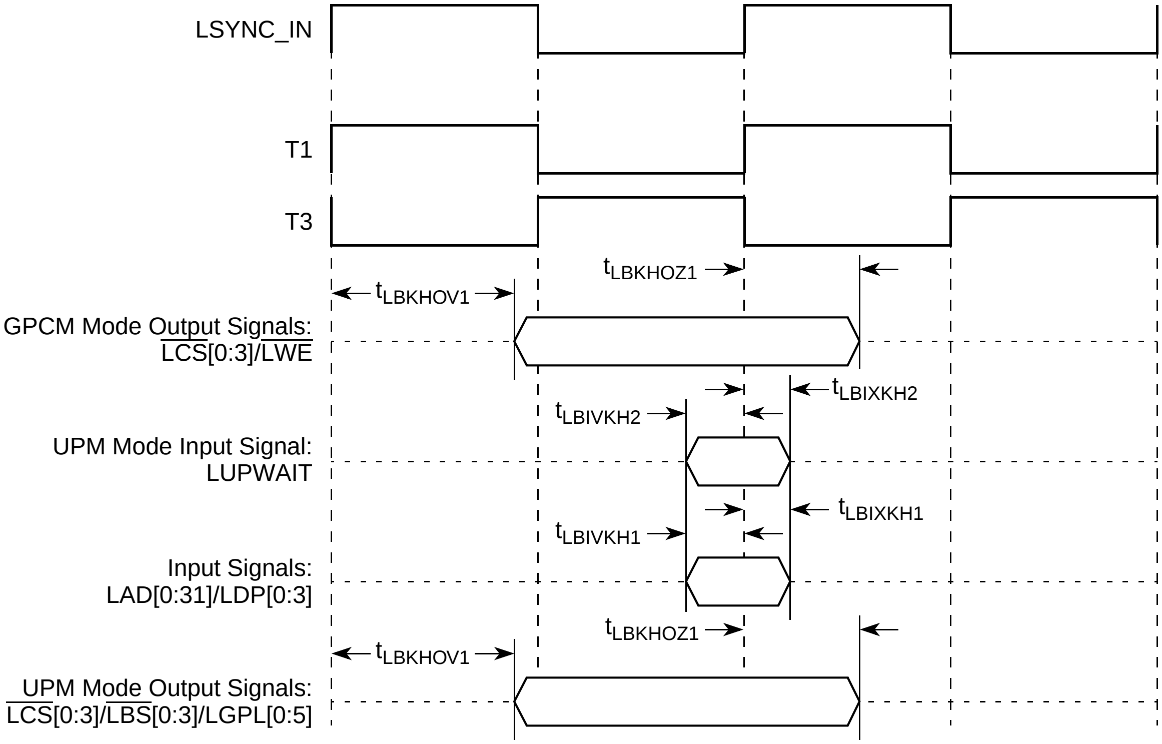


Figure 25. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Enabled)

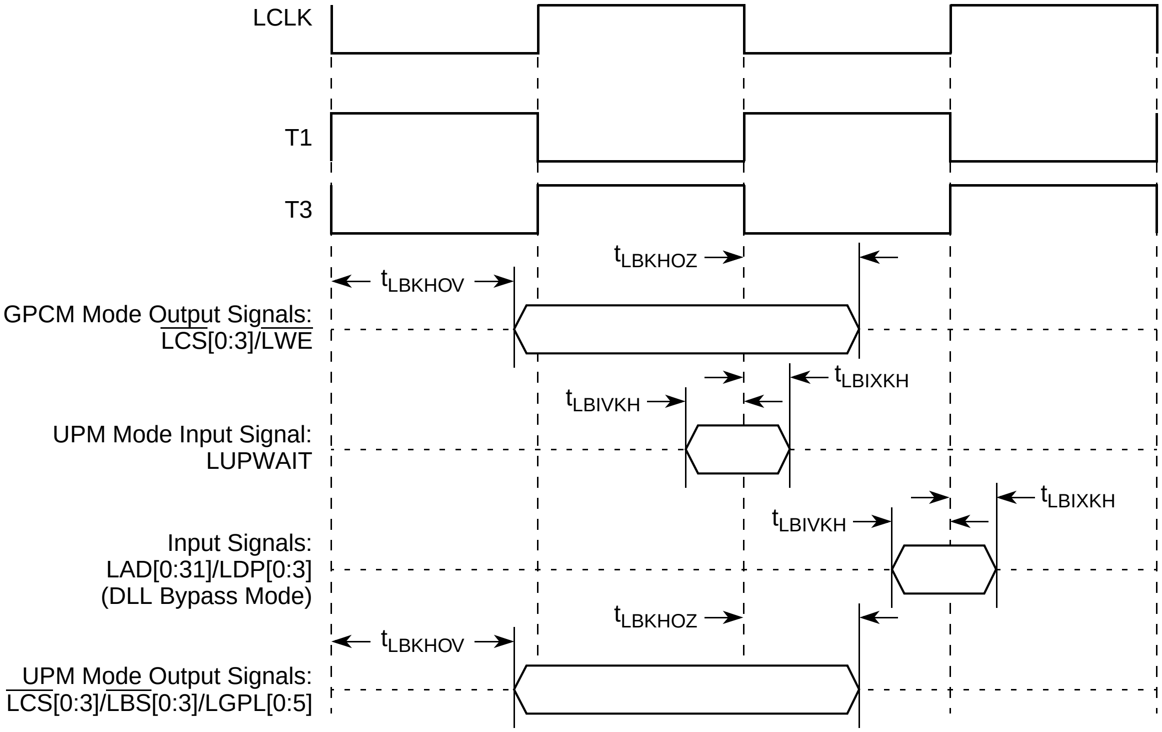


Figure 26. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Bypass Mode)

This figure shows the PCI input AC timing conditions.

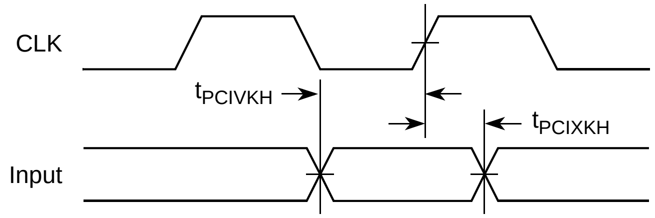


Figure 37. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.

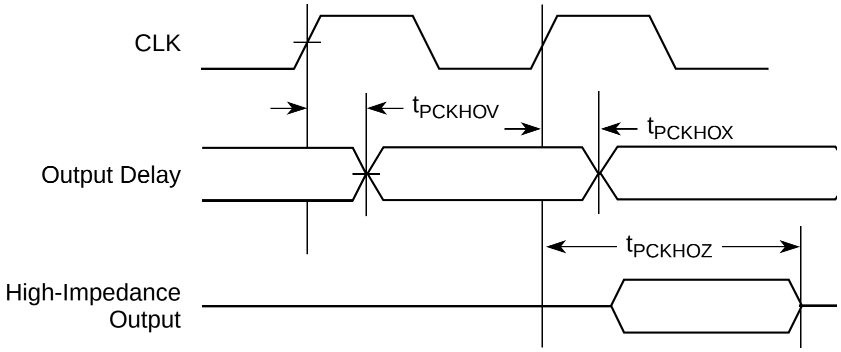


Figure 38. PCI Output AC Timing Measurement Condition

13 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8360E/58E.

13.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the device timer pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 49. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤V_{IN} ≤OV_{DD}	—	±10	μA

13.2 Timers AC Timing Specifications

This table provides the timer input and output AC timing specifications.

Table 50. Timers Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Typ	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

This figure provides the AC test load for the timers.

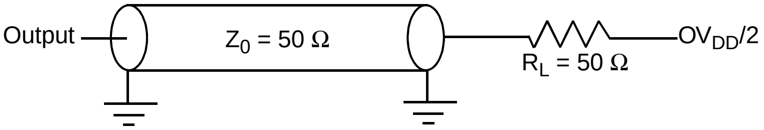


Figure 39. Timers AC Test Load

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8360E/58E.

14.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the device GPIO.

Table 51. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	$I_{OH} = -6.0$ mA	2.4	—	V	1
Output low voltage	V_{OL}	$I_{OL} = 6.0$ mA	—	0.5	V	1
Output low voltage	V_{OL}	$I_{OL} = 3.2$ mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	$0\ V \le V_{IN} \le OV_{DD}$	—	±10	μA	—

Note:

1. This specification applies when operating from 3.3-V supply.

Table 60. UTOPIA AC Timing Specifications[1] (continued)

Characteristic	Symbol[2]	Min	Max	Unit	Notes
UTOPIA inputs—Internal clock input hold time	t_{UIIXKH}	2.4	—	ns	—
UTOPIA inputs—External clock input hold time	t_{UEIXKH}	1	—	ns	3

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{UIKHOX} symbolizes the UTOPIA outputs internal timing (UI) for the time t_{UTOPIA} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
3. In rev. 2.0 silicon, due to errata, t_{UEIVKH} minimum is 4.3 ns and t_{UEIXKH} minimum is 1.4 ns under specific conditions. Refer to Errata QE_UPC3 in *Chip Errata for the MPC8360E, Rev. 1*.

This figure provides the AC test load for the UTOPIA.

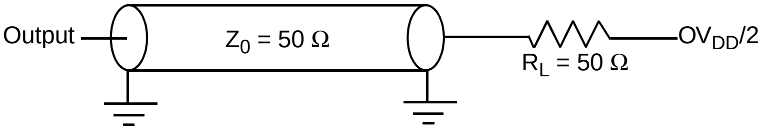


Figure 46. UTOPIA AC Test Load

These figures represent the AC timing from Table 56. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the UTOPIA timing with external clock.

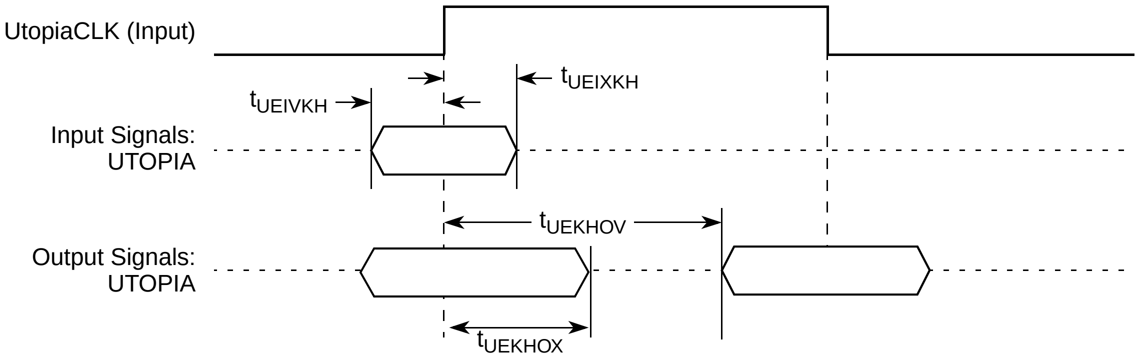


Figure 47. UTOPIA AC Timing (External Clock) Diagram

20 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8360E/58E is available in a tape ball grid array (TBGA), see Section 20.1, “Package Parameters for the TBGA Package,” and Section 20.2, “Mechanical Dimensions of the TBGA Package,” for information on the package.

20.1 Package Parameters for the TBGA Package

The package parameters for rev. 2.0 silicon are as provided in the following list. The package type is 37.5 mm × 37.5 mm, 740 tape ball grid array (TBGA).

Package outline	37.5 mm × 37.5 mm
Interconnects	740
Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder Balls	62 Sn/36 Pb/2 Ag (ZU package) 95.5 Sn/0.5 Cu/4Ag (VV package)
Ball diameter (typical)	0.64 mm

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$LV_{DD}0$	D5, D6	Power for UCC1 Ethernet interface (2.5 V, 3.3 V)	$LV_{DD}0$	—
$LV_{DD}1$	C17, D16	Power for UCC2 Ethernet interface option 1 (2.5 V, 3.3 V)	$LV_{DD}1$	9
$LV_{DD}2$	B18, E21	Power for UCC2 Ethernet interface option 2 (2.5 V, 3.3 V)	$LV_{DD}2$	9
V_{DD}	C36, D29, D35, E16, F9, F12, F15, F17, F18, F20, F21, F23, F25, F26, F29, F31, F32, F33, G6, J6, K32, M32, N6, P33, R6, R32, U32, V6, Y5, Y32, AB6, AB33, AD6, AF32, AK6, AL6, AM7, AM9, AM10, AM11, AM12, AM13, AM14, AM15, AM18, AM21, AM25, AM28, AM32, AN15, AN21, AN26, AU9, AU17	Power for core (1.2 V)	V_{DD}	—
OV_{DD}	A10, B9, B15, B32, C1, C12, C22, C29, D24, E3, E10, E27, G4, H35, J1, J35, K2, M4, N3, N34, R2, R37, T36, U2, U33, V4, V34, W3, Y35, Y37, AA1, AA36, AB2, AB34	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV_{DD}	—
MVREF1	AN20	I	DDR reference voltage	—
MVREF2	AU32	I	DDR reference voltage	—
SPARE1	B11	I/O	OV_{DD}	8
SPARE3	AH32	—	GV_{DD}	8
SPARE4	AU18	—	GV_{DD}	7
SPARE5	AP1	—	GV_{DD}	8

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_MODE	D36	I	OV_{DD}	—
M66EN/CE_PF[4]	B37	I/O	OV_{DD}	—
Local Bus Controller Interface				
LAD[0:31]	N32, N33, N35, N36, P37, P32, P34, R36, R35, R34, R33, T37, T35, T34, T33, U37, T32, U36, U34, V36, V35, W37, W35, V33, V32, W34, Y36, W32, AA37, Y33, AA35, AA34	I/O	OV_{DD}	—
LDP[0]/CKSTOP_OUT	AB37	I/O	OV_{DD}	—
LDP[1]/CKSTOP_IN	AB36	I/O	OV_{DD}	—
LDP[2]/LCS[6]	AB35	I/O	OV_{DD}	—
LDP[3]/LCS[7]	AA33	I/O	OV_{DD}	—
LA[27:31]	AC37, AA32, AC36, AC34, AD36	O	OV_{DD}	—
LCS[0:5]	AD33, AG37, AF34, AE33, AD32, AH37	O	OV_{DD}	—
LWE[0:3]/LSDDQM[0:3]/LBS[0:3]	AG35, AG34, AH36, AE32	O	OV_{DD}	—
LBCTL	AD35	O	OV_{DD}	—
LALE	M37	O	OV_{DD}	—
LGPL0/LSDA10/cfg_reset_source0	AB32	I/O	OV_{DD}	—
LGPL1/LSDWE/cfg_reset_source1	AE37	I/O	OV_{DD}	—
LGPL2/LSDRAS/LOE	AC33	O	OV_{DD}	—
LGPL3/LSDCAS/cfg_reset_source2	AD34	I/O	OV_{DD}	—
LGPL4/LGTA/LUPWAIT/LPBSE	AE35	I/O	OV_{DD}	—
LGPL5/cfg_clkin_div	AF36	I/O	OV_{DD}	—
LCKE	G36	O	OV_{DD}	—
LCLK[0]	J33	O	OV_{DD}	—
LCLK[1]/LCS[6]	J34	O	OV_{DD}	—
LCLK[2]/LCS[7]	G37	O	OV_{DD}	—
LSYNC_OUT	F34	O	OV_{DD}	—
LSYNC_IN	G35	I	OV_{DD}	—
Programmable Interrupt Controller				
MCP_OUT	E34	O	OV_{DD}	2
IRQ0/MCP_IN	C37	I	OV_{DD}	—
IRQ[1]/M1SRCID[4]/M2SRCID[4]/LSRCID[4]	F35	I/O	OV_{DD}	—
IRQ[2]/M1DVAL/M2DVAL/LDVAL	F36	I/O	OV_{DD}	—
IRQ[3]/CORE_SRESET	H34	I/O	OV_{DD}	—

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{PORESET}}$	L37	I	OV_{DD}	—
$\overline{\text{HRESET}}$	L36	I/O	OV_{DD}	1
$\overline{\text{SRESET}}$	M33	I/O	OV_{DD}	2
Thermal Management				
THERM0	AP19	I	GV_{DD}	—
THERM1	AT31	I	GV_{DD}	—
Power and Ground Signals				
$AV_{DD}1$	K35	Power for LBIU DLL (1.2 V)	$AV_{DD}1$	—
$AV_{DD}2$	K36	Power for CE PLL (1.2 V)	$AV_{DD}2$	—
$AV_{DD}5$	AM29	Power for e300 PLL (1.2 V)	$AV_{DD}5$	—
$AV_{DD}6$	K37	Power for system PLL (1.2 V)	$AV_{DD}6$	—
GND	A2, A8, A13, A19, A22, A25, A31, A33, A36, B7, B12, B24, B27, B30, C4, C6, C9, C15, C26, C32, D3, D8, D11, D14, D17, D19, D23, D27, E7, E13, E25, E30, E36, F4, F37, G34, H1, H5, H32, H33, J4, J32, J37, K1, L3, L5, L33, L34, M1, M34, M35, N37, P2, P5, P35, P36, R4, T3, U1, U5, U35, V37, W1, W4, W33, W36, Y34, AA3, AA5, AC3, AC32, AC35, AD1, AD37, AE4, AE34, AE36, AF33, AG4, AG6, AG32, AH35, AJ1, AJ4, AJ32, AJ35, AJ37, AK36, AL3, AL34, AM4, AN6, AN23, AN30, AP8, AP12, AP14, AP16, AP17, AP20, AP25, AR6, AR8, AR9, AR19, AR24, AR31, AR35, AR37, AT4, AT10, AT19, AT20, AT25, AU14, AU22, AU28, AU35	—	—	—
GV_{DD}	AD4, AE3, AF1, AF5, AF35, AF37, AG2, AG36, AH33, AH34, AK5, AM1, AM35, AM37, AN2, AN10, AN11, AN12, AN14, AN32, AN36, AP5, AP23, AP28, AR1, AR7, AR10, AR12, AR21, AR25, AR27, AR33, AT15, AT22, AT28, AT33, AU2, AU5, AU16, AU31, AU36	Power for DDR DRAM I/O voltage (2.5 or 1.8 V)	GV_{DD}	—
$LV_{DD}0$	D5, D6	Power for UCC1 Ethernet interface (2.5 V, 3.3 V)	$LV_{DD}0$	—

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
No Connect				
NC	AM16, AM17, AM20, AN13, AN16, AN17, AP10, AP11, AP13, AP15, AP18, AR11, AR13, AR14, AR15, AR16, AR17, AR20, AT11, AT12, AT13, AT14, AT16, AT17, AT18, AU10, AU11, AU12, AU13, AU15, AU19	—	—	—

Notes:

1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to $OV_{DD.}$
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. These are On Die Termination pins, used to control DDR2 memories internal termination resistance.
7. This pin must always be tied to GND.
8. This pin must always be left not connected.
9. Refer to *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* section on “RGMII Pins,” for information about the two UCC2 Ethernet interface options.
10. This pin must always be tied to GV_{DD}.
11. It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor for DDR2.

21 Clocking

This figure shows the internal distribution of clocks within the MPC8360E.

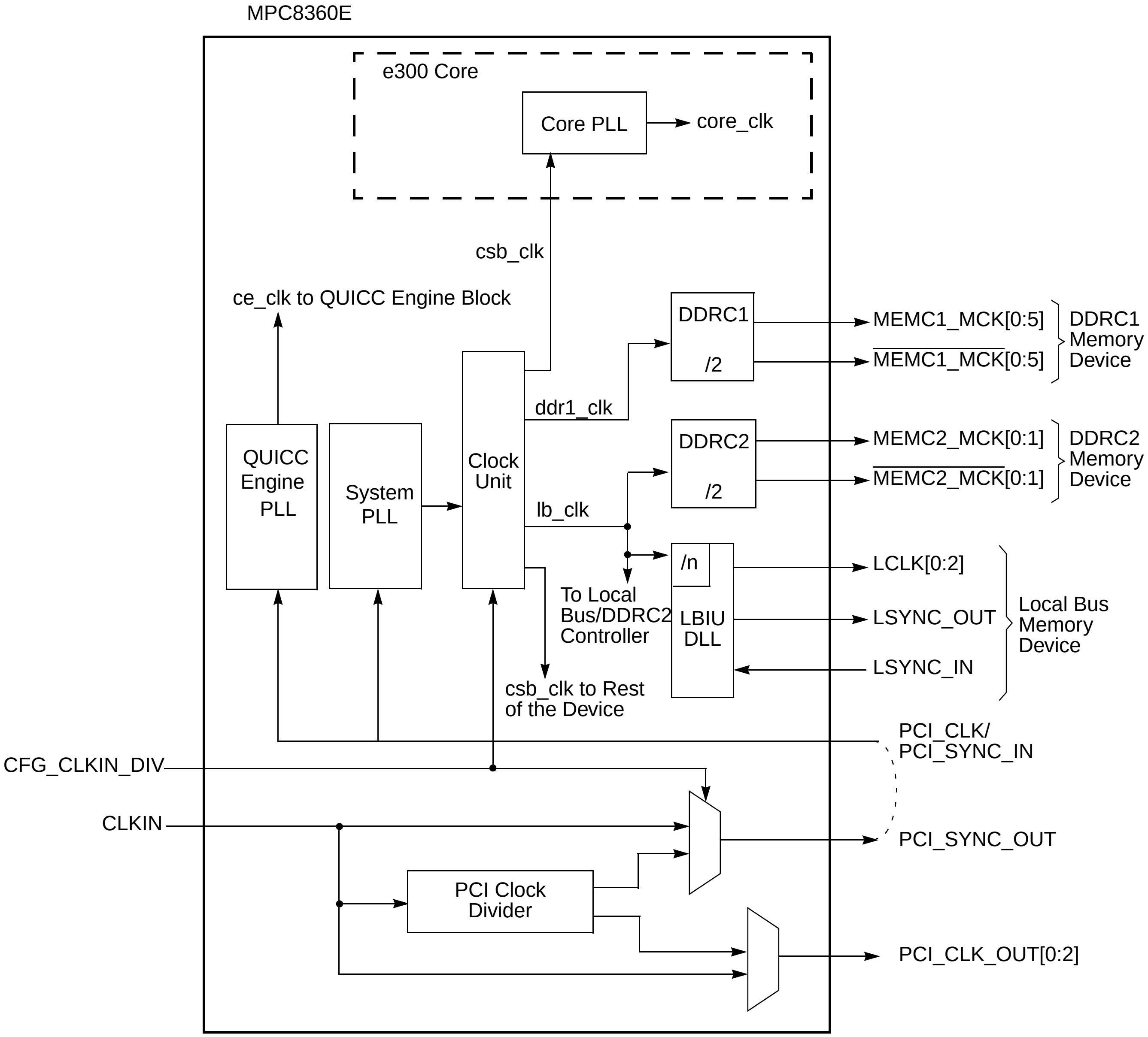


Figure 54. MPC8360E Clock Subsystem

Table 72. CSB Frequency Options (continued)

CFG_CLKIN_DIV at Reset[1]	**SPMF**	***csb_clk*: Input Clock Ratio**[2]	**Input Clock Frequency (MHz)**[2]			
			16.67	**25**	**33.33**	**66.67**
			***csb_clk* Frequency (MHz)**			
Low	0110	6:1	100	150	200	
Low	0111	7:1	116	175	233	
Low	1000	8:1	133	200	266	
Low	1001	9:1	150	225	300	
Low	1010	10:1	166	250	333	
Low	1011	11:1	183	275		
Low	1100	12:1	200	300		
Low	1101	13:1	216	325		
Low	1110	14:1	233			
Low	1111	15:1	250			
Low	0000	16:1	266			
High	0010	2:1				133
High	0011	3:1			100	200
High	0100	4:1			133	266
High	0101	5:1			166	333
High	0110	6:1			200	
High	0111	7:1			233	
High	1000	8:1				
High	1001	9:1				
High	1010	10:1				
High	1011	11:1				
High	1100	12:1				
High	1101	13:1				
High	1110	14:1				
High	1111	15:1				
High	0000	16:1				

[1] CFG_CLKIN_DIV is only used for host mode; CLKIN must be tied low and CFG_CLKIN_DIV must be pulled down (low) in agent mode.

[2] CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (° C)
T_B = board temperature at the package perimeter (° C)
$R_{\theta JA}$ = junction to board thermal resistance (° C/W) per JESD51-8
P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

22.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (° C)
T_T = thermocouple temperature on top of package (° C)
Ψ_{JT} = junction-to-ambient thermal resistance (° C/W)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

22.2.4 Heat Sinks and Junction-to-Ambient Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (° C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (° C/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (° C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.