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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8358evvagdg

- 10/100 Mbps Ethernet/IEEE Std. 802.3™ CDMA/CS interface through a media-independent interface (MII, RMII, RGMII)¹
- 1000 Mbps Ethernet/IEEE 802.3 CDMA/CS interface through a media-independent interface (GMII, RGMII, TBI, RTBI) on UCC1 and UCC2
- 9.6-Kbyte jumbo frames
- ATM full-duplex SAR, up to 622 Mbps (OC-12/STM-4), AAL0, AAL1, and AAL5 in accordance ITU-T I.363.5
- ATM AAL2 CPS, SSSAR, and SSTED up to 155 Mbps (OC-3/STM-1) Mbps full duplex (with 4 CPS packets per cell) in accordance ITU-T I.366.1 and I.363.2
- ATM traffic shaping for CBR, VBR, UBR, and GFR traffic types compatible with ATM forum TM4.1 for up to 64-Kbyte simultaneous ATM channels
- ATM AAL1 structured and unstructured circuit emulation service (CES 2.0) in accordance with ITU-T I.163.1 and ATM Forum af-vtoa-00-0078.000
- IMA (Inverse Multiplexing over ATM) for up to 31 IMA links over 8 IMA groups in accordance with the ATM forum AF-PHY-0086.000 (Version 1.0) and AF-PHY-0086.001 (Version 1.1)
- ATM Transmission Convergence layer support in accordance with ITU-T I.432
- ATM OAM handling features compatible with ITU-T I.610
- PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686, and 3153
- IP support for IPv4 packets including TOS, TTL, and header checksum processing
- Ethernet over first mile IEEE 802.3ah
- Shim header
- Ethernet-to-Ethernet/AAL5/AAL2 inter-working
- L2 Ethernet switching using MAC address or IEEE Std. 802.1P/Q™ VLAN tags
- ATM (AAL2/AAL5) to Ethernet (IP) interworking in accordance with RFC2684 including bridging of ATM ports to Ethernet ports
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- AAL2 protocol rate up to 4 CPS at OC-3/STM-1 rate
- Packet over Sonet (POS) up to 622-Mbps full-duplex 124 MultiPHY
- POS hardware; microcode must be loaded as an IRAM package
- Transparent up to 70-Mbps full-duplex
- HDLC up to 70-Mbps full-duplex
- HDLC BUS up to 10 Mbps
- Asynchronous HDLC
- UART
- BISYNC up to 2 Mbps
- User-programmable Virtual FIFO size
- QUICC multichannel controller (QMC) for 64 TDM channels
- One multichannel communication controller (MCC) only on the MPC8360E supporting the following:
 - 256 HDLC or transparent channels
 - 128 SS7 channels
 - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces
- Two UTOPIA/POS interfaces on the MPC8360E supporting 124 MultiPHY each (optional 2*128 MultiPHY with extended address) and one UTOPIA/POS interface on the MPC8358E supporting 31/124 MultiPHY
- Two serial peripheral interfaces (SPI); SPI2 is dedicated to Ethernet PHY management

1.SMII or SGMII media-independent interface is not currently supported.

This table shows the estimated typical I/O power dissipation for the device.

Table 6. Estimated Typical I/O Power Dissipation

Interface	Parameter	GV _{DD} (1.8 V)	GV _{DD} (2.5 V)	OV _{DD} (3.3 V)	LV _{DD} (3.3 V)	LV _{DD} (2.5 V)	Unit	Comments
DDR I/O 65% utilization R _s = 20 Ω R _t = 50 Ω 2 pairs of clocks	200 MHz, 1 × 32 bits	0.3	0.46	—	—	—	W	—
	200 MHz, 1 × 64 bits	0.4	0.58	—	—	—	W	—
	200 MHz, 2 × 32 bits	0.6	0.92	—	—	—	W	—
	266 MHz, 1 × 32 bits	0.35	0.56	—	—	—	W	—
	266 MHz, 1 × 64 bits	0.46	0.7	—	—	—	W	—
	266 MHz, 2 × 32 bits	0.7	1.11	—	—	—	W	—
	333 MHz, 1 × 32 bits	0.4	0.65	—	—	—	W	—
	333 MHz, 1 × 64 bits	0.53	0.82	—	—	—	W	—
	333 MHz, 2 × 32 bits	0.81	1.3	—	—	—	W	—
Local Bus I/O Load = 25 pF 3 pairs of clocks	133 MHz, 32 bits	—	—	0.22	—	—	W	—
	83 MHz, 32 bits	—	—	0.14	—	—	W	—
	66 MHz, 32 bits	—	—	0.12	—	—	W	—
	50 MHz, 32 bits	—	—	0.09	—	—	W	—
PCI I/O Load = 30 pF	33 MHz, 32 bits	—	—	0.05	—	—	W	—
	66 MHz, 32 bits	—	—	0.07	—	—	W	—
10/100/1000 Ethernet I/O Load = 20 pF	MII or RMII	—	—	—	0.01	—	W	Multiply by number of interfaces used.
	GMII or TBI	—	—	—	0.04	—	W	
	RGMII or RTBI	—	—	—	—	0.04	W	
Other I/O	—	—	—	0.1	—	—	W	—

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8360E/58E.

NOTE

The rise/fall time on QUICC Engine block input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of V_{DD}; fall time refers to transitions from 90% to 10% of V_{DD}.

5.3 QUICC Engine Block Operating Frequency Limitations

This section specifies the limits of the AC electrical characteristics for the operation of the QUICC Engine block's communication interfaces.

NOTE

The settings listed below are required for correct hardware interface operation. Each protocol by itself requires a minimal QUICC Engine block operating frequency setting for meeting the performance target. Because the performance is a complex function of all the QUICC Engine block settings, the user should make use of the QUICC Engine block performance utility tool provided by Freescale to validate their system.

This table lists the maximal QUICC Engine block I/O frequencies and the minimal QUICC Engine block core frequency for each interface.

Table 13. QUICC Engine Block Operating Frequency Limitations

Interface	Interface Operating Frequency (MHz)	Max Interface Bit Rate (Mbps)	Min QUICC Engine Operating Frequency ¹ (MHz)	Notes
Ethernet Management: MDC/MDIO	10 (max)	10	20	—
MII	25 (typ)	100	50	—
RMII	50 (typ)	100	50	—
GMII/RGMII/TBI/RTBI	125 (typ)	1000	250	—
SPI (master/slave)	10 (max)	10	20	—
UCC through TDM	50 (max)	70	$8 \times F$	2
MCC	25 (max)	16.67	$16 \times F$	2, 4
UTOPIA L2	50 (max)	800	$2 \times F$	2
POS-PHY L2	50 (max)	800	$2 \times F$	2
HDLC bus	10 (max)	10	20	—
HDLC/transparent	50 (max)	50	$8/3 \times F$	2, 3
UART/async HDLC	3.68 (max internal ref clock)	115 (Kbps)	20	—
BISYNC	2 (max)	2	20	—
USB	48 (ref clock)	12	96	—

Notes:

1. The QUICC Engine module needs to run at a frequency higher than or equal to what is listed in this table.
2. 'F' is the actual interface operating frequency.
3. The bit rate limit is independent of the data bus width (that is, the same for serial, nibble, or octal interfaces).
4. TDM in high-speed mode for serial data interface.

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR and DDR2 SDRAM interface of the MPC8360E/58E.

Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) $\pm$ 5%.

Parameter ⁸	Symbol ¹	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKHME}	-0.6	0.9	ns	7

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/MCK referenced measurements are made from the crossing of the two signals ± 0.1 V.
- In the source synchronous mode, MCK/MCK can be shifted in $\frac{1}{4}$ applied cycle increments through the clock control register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
- ADDR/CMD includes all DDR SDRAM output signals except $\overline{MCK}/\overline{MCK}$, $\overline{MCS}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by $\frac{1}{2}$ applied cycle.
- Note that t_{DDKMHM} follows the symbol conventions described in note 1. For example, t_{DDKMHM} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKMHM} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. Refer *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the device.
- All outputs are referenced to the rising edge of MCK(n) at the pins of the device. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
- AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.
- In rev. 2.0 silicon, t_{DDKMHM} maximum meets the specification of 0.6 ns. In rev. 2.0 silicon, due to errata, t_{DDKMHM} minimum is -0.9 ns. Refer to Errata DDR18 in *Chip Errata for the MPC8360E, Rev. 1*.

This figure shows the DDR SDRAM output timing for address skew with respect to any MCK.

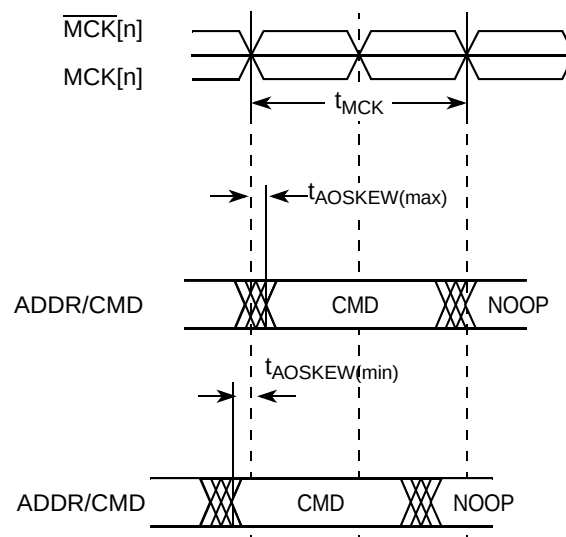


Figure 7. Timing Diagram for t_{AOSKEW} Measurement

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8360E/58E.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface of the device.

Table 23. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V	—
Low-level input voltage OV_{DD}	V_{IL}	-0.3	0.8	V	—
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.4$	—	V	—
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V	—
Input current ($0 V \leq V_{IN} \leq OV_{DD}$)	I_{IN}	—	± 10	μA	1

Note:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface of the device.

Table 24. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	—
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	—	2

Notes:

- Actual attainable baud rate is limited by the latency of interrupt processing.
- The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

8 UCC Ethernet Controller: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

8.1 Three-Speed Ethernet Controller (10/100/1000 Mbps)—GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), MII (media independent interface), RMII (reduced media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The MII, RMII, GMII, and TBI interfaces are only defined for 3.3 V, while the RGMII and RTBI interfaces are only defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet

8.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

Table 34. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
PMA_RX_CLK clock period	t_{TRX}	—	16.0	—	ns	—
PMA_RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns	—
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%	—
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns	2
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.0	—	—	ns	2
RX_CLK clock rise time, V _{IL} (min) to V _{IH} (max)	t_{TRXR}	0.7	—	2.4	ns	—
RX_CLK clock fall time, V _{IH} (max) to V _{IL} (min)	t_{TRXF}	0.7	—	2.4	ns	—

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
- Setup and hold time of even numbered RCG are measured from rising edge of PMA_RX_CLK1. Setup and hold time of odd numbered RCG are measured from rising edge of PMA_RX_CLK0.

This figure shows the TBI receive AC timing diagram.

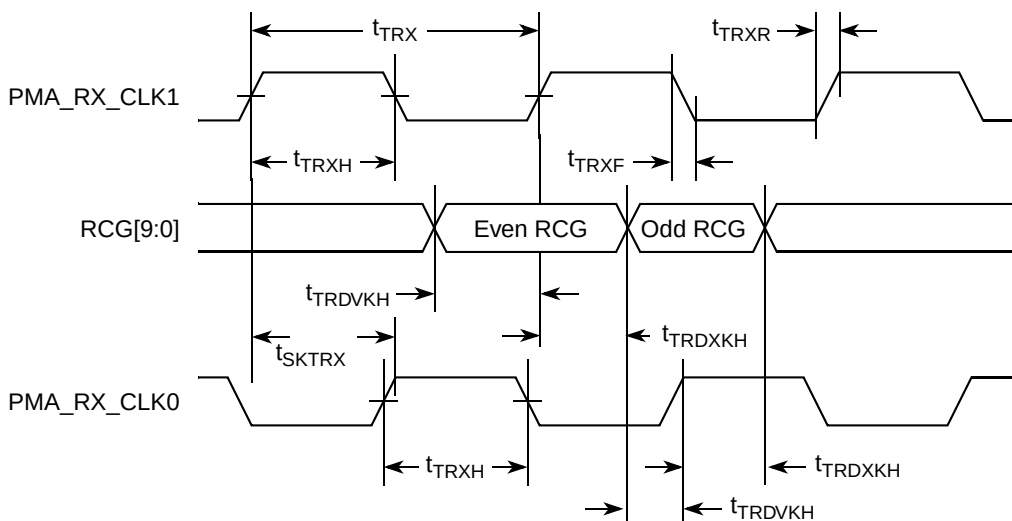


Figure 19. TBI Receive AC Timing Diagram

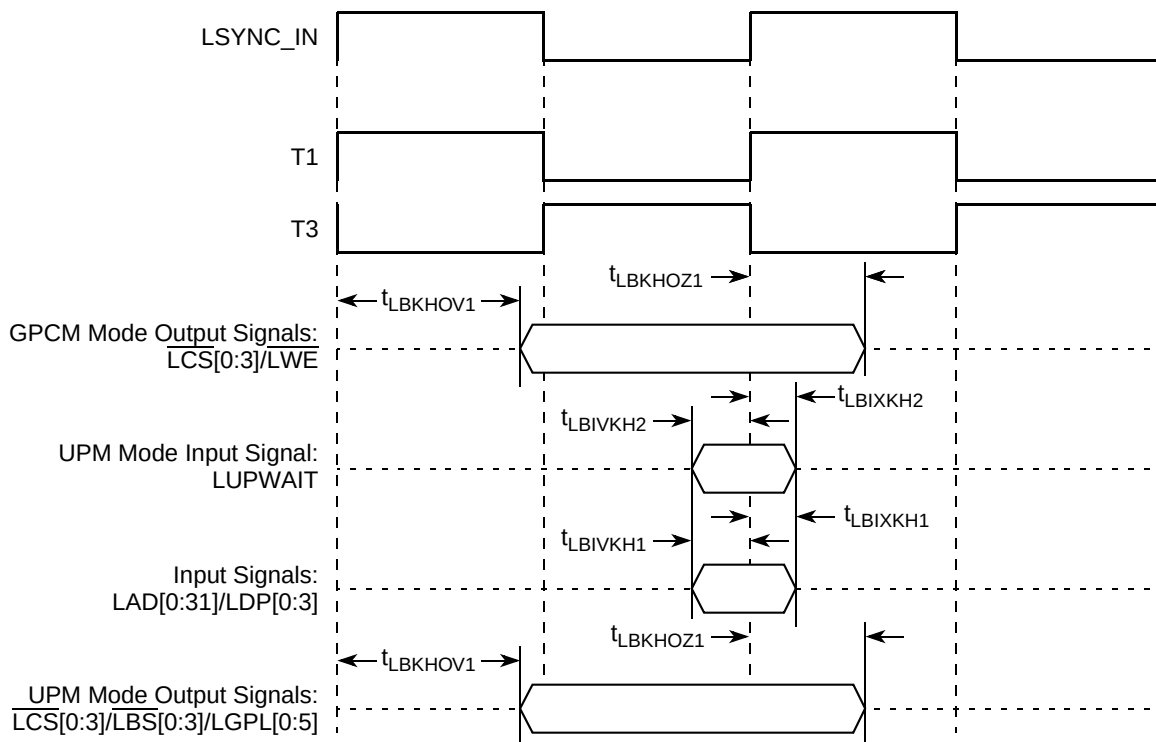


Figure 25. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Enabled)

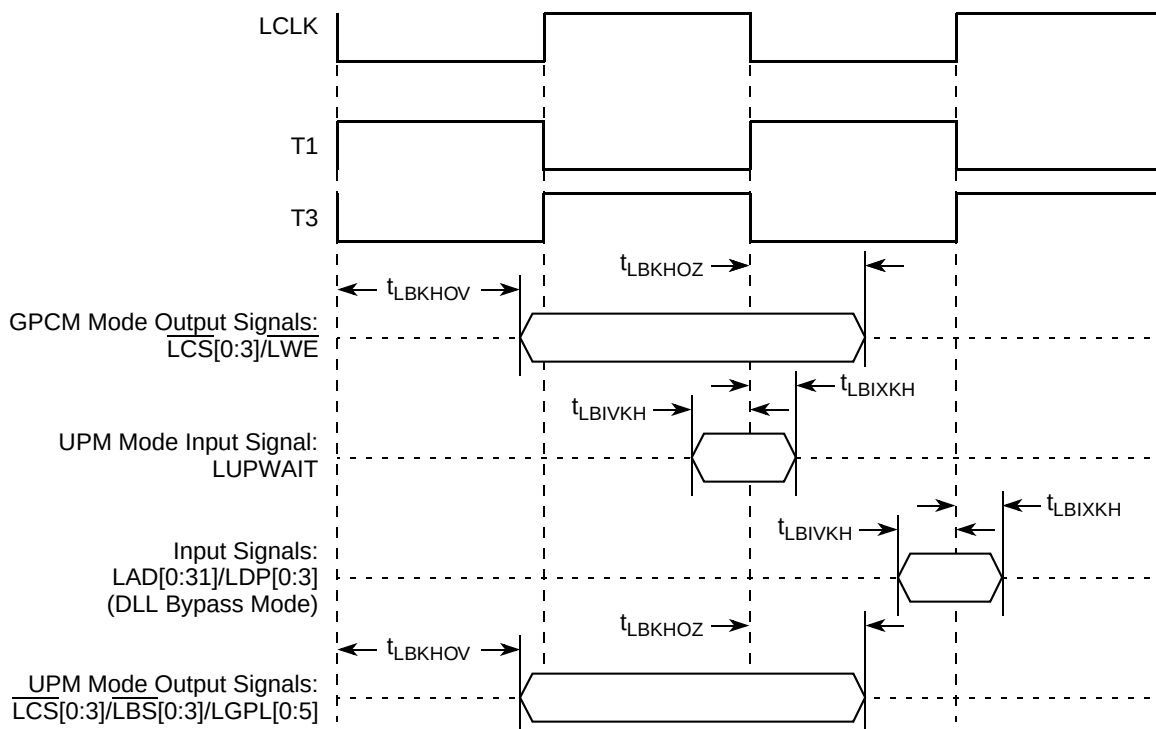


Figure 26. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Bypass Mode)

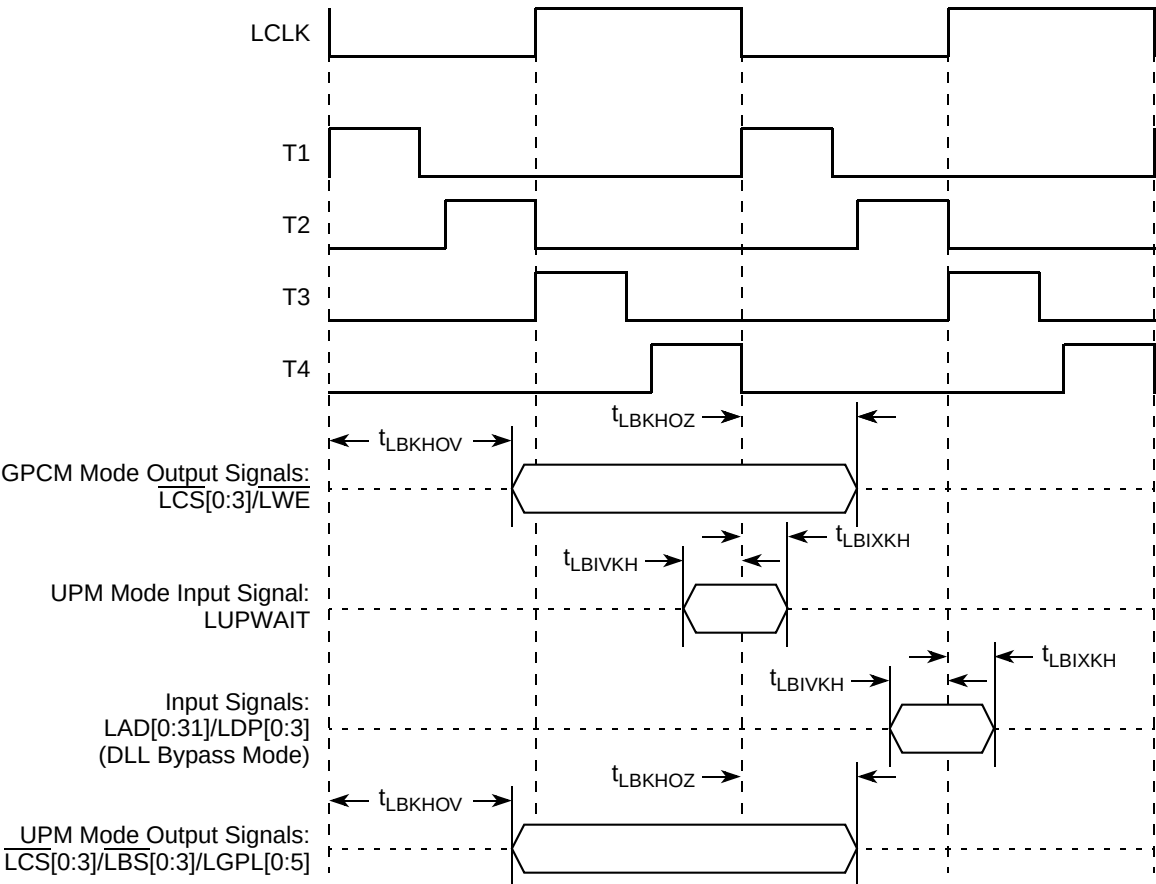


Figure 27. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (DLL Bypass Mode)

This figure provides the test access port timing diagram.

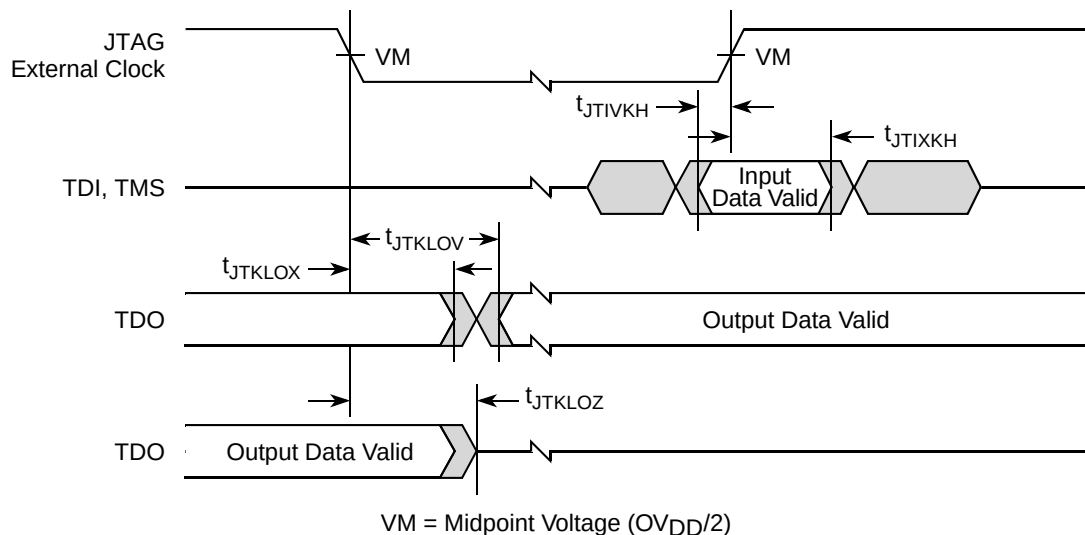


Figure 33. Test Access Port Timing Diagram

11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8360E/58E.

11.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I²C interface of the device.

Table 44. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	-0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	0.4	V	1
Output fall time from $V_{IH}(\text{min})$ to $V_{IL}(\text{max})$ with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current ($0\text{ V} \leq V_{IN} \leq OV_{DD}$)	I_{IN}	—	± 10	μA	4

Notes:

- Output voltage (open drain or open collector) condition = 3 mA sink current.
- C_B = capacitance of one bus line in pF.
- Refer to the *MPC8360E Integrated Communications Processor Reference Manual* for information on the digital filter used.
- I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

This figure provides the AC test load for the I²C.

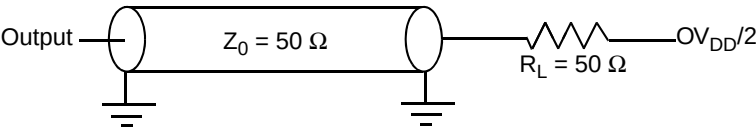


Figure 34. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

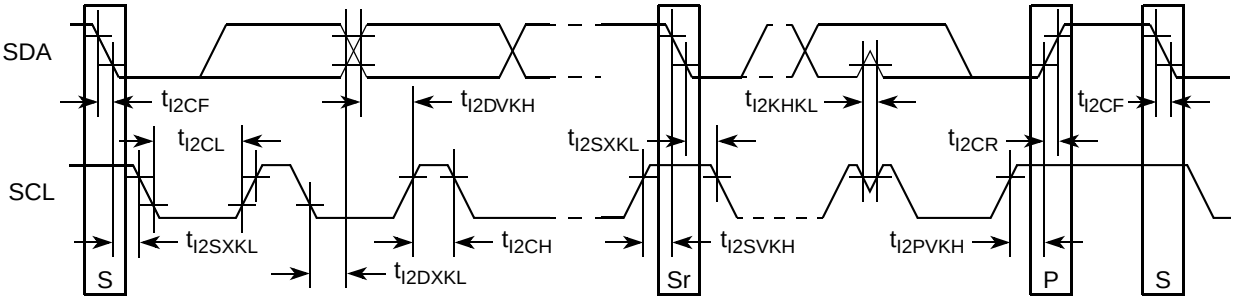


Figure 35. I²C Bus AC Timing Diagram

12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8360E/58E.

12.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface of the device.

Table 46. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH} \text{ (min) or}$	$0.5 \times OV_{DD}$	$OV_{DD} + 0.5$	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL} \text{ (max)}$	-0.5	$0.3 \times OV_{DD}$	V
High-level output voltage	V_{OH}	$I_{OH} = -500 \mu A$	$0.9 \times OV_{DD}$	—	V
Low-level output voltage	V_{OL}	$I_{OL} = 1500 \mu A$	—	$0.1 \times OV_{DD}$	V
Input current	I_{IN}	$0 V \leq V_{IN}^1 \leq OV_{DD}$	—	± 10	μA

12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the device. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. This table provides the PCI AC timing specifications at 66 MHz.

Table 47. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2, 5
Output hold from clock	t_{PCKHOX}	1	—	ns	2

13.2 Timers AC Timing Specifications

This table provides the timer input and output AC timing specifications.

Table 50. Timers Input AC Timing Specifications¹

Characteristic	Symbol ²	Typ	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

- Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
- Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

This figure provides the AC test load for the timers.

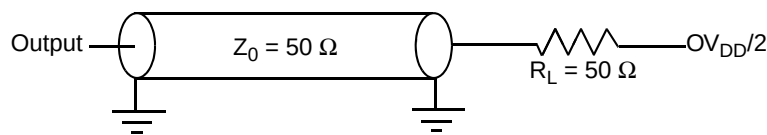


Figure 39. Timers AC Test Load

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8360E/58E.

14.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the device GPIO.

Table 51. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	$I_{OH} = -6.0 \text{ mA}$	2.4	—	V	1
Output low voltage	V_{OL}	$I_{OL} = 6.0 \text{ mA}$	—	0.5	V	1
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V	1
Input low voltage	V_{IL}	—	-0.3	0.8	V	—
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 10	μA	—

Note:

- This specification applies when operating from 3.3-V supply.

20.3 Pinout Listings

Refer to AN3097, “MPC8360/MPC8358E PowerQUICC Design Checklist,” for proper pin termination and usage.

This table shows the pin list of the MPC8360E TBGA package.

Table 66. MPC8360E TBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Primary DDR SDRAM Memory Controller Interface				
MEMC1_MDQ[0:31]	AJ34, AK33, AL33, AL35, AJ33, AK34, AK32, AM36, AN37, AN35, AR34, AT34, AP37, AP36, AR36, AT35, AP34, AR32, AP32, AM31, AN33, AM34, AM33, AM30, AP31, AM27, AR30, AT32, AN29, AP29, AN27, AR29	I/O	GV _{DD}	—
MEMC1_MDQ[32:63]/ MEMC2_MDQ[0:31]	AN8, AN7, AM8, AM6, AP9, AN9, AT7, AP7, AU6, AP6, AR4, AR3, AT6, AT5, AR5, AT3, AP4, AM5, AP3, AN3, AN5, AL5, AN4, AM2, AL2, AH5, AK3, AJ2, AJ3, AH4, AK4, AH3	I/O	GV _{DD}	—
MEMC1_MECC[0:4]/ MSRCID[0:4]	AP24, AN22, AM19, AN19, AM24	I/O	GV _{DD}	—
MEMC1_MECC[5]/ MDVAL	AM23	I/O	GV _{DD}	—
MEMC1_MECC[6:7]	AM22, AN18	I/O	GV _{DD}	—
MEMC1_MDM[0:3]	AL36, AN34, AP33, AN28	O	GV _{DD}	—
MEMC1_MDM[4:7]/ MEMC2_MDM[0:3]	AT9, AU4, AM3, AJ6	O	GV _{DD}	—
MEMC1_MDM[8]	AP27	O	GV _{DD}	—
MEMC1_MDQS[0:3]	AK35, AP35, AN31, AM26	I/O	GV _{DD}	—
MEMC1_MDQS[4:7]/ MEMC2_MDQS[0:3]	AT8, AU3, AL4, AJ5	I/O	GV _{DD}	—
MEMC1_MDQS[8]	AP26	I/O	GV _{DD}	—
MEMC1_MBA[0:1]	AU29, AU30	O	GV _{DD}	—
MEMC1_MBA[2]	AT30	O	GV _{DD}	—
MEMC1_MA[0:14]	AU21, AP22, AP21, AT21, AU25, AU26, AT23, AR26, AU24, AR23, AR28, AU23, AR22, AU20, AR18	O	GV _{DD}	—
MEMC1_MODT[0:1]	AG33, AJ36	O	GV _{DD}	6
MEMC1_MODT[2:3]/ MEMC2_MODT[0:1]	AT1, AK2	O	GV _{DD}	6
MEMC1_MWE	AT26	O	GV _{DD}	—
MEMC1_MRAS	AT29	O	GV _{DD}	—
MEMC1_MCAS	AT24	O	GV _{DD}	—
MEMC1_MCS[0:1]	AU27, AT27	O	GV _{DD}	—
MEMC1_MCS[2:3]/ MEMC2_MCS[0:1]	AU8, AU7	O	GV _{DD}	—

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_MODE	D36	I	OV _{DD}	—
M66EN/CE_PF[4]	B37	I/O	OV _{DD}	—
Local Bus Controller Interface				
LAD[0:31]	N32, N33, N35, N36, P37, P32, P34, R36, R35, R34, R33, T37, T35, T34, T33, U37, T32, U36, U34, V36, V35, W37, W35, V33, V32, W34, Y36, W32, AA37, Y33, AA35, AA34	I/O	OV _{DD}	—
LDP[0]/CKSTOP_OUT	AB37	I/O	OV _{DD}	—
LDP[1]/CKSTOP_IN	AB36	I/O	OV _{DD}	—
LDP[2]/LCS[6]	AB35	I/O	OV _{DD}	—
LDP[3]/LCS[7]	AA33	I/O	OV _{DD}	—
LA[27:31]	AC37, AA32, AC36, AC34, AD36	O	OV _{DD}	—
LCS[0:5]	AD33, AG37, AF34, AE33, AD32, AH37	O	OV _{DD}	—
LWE[0:3]/LSDDQM[0:3]/LBS[0:3]	AG35, AG34, AH36, AE32	O	OV _{DD}	—
LBCTL	AD35	O	OV _{DD}	—
LALE	M37	O	OV _{DD}	—
LGPL0/LSDA10/cfg_reset_source0	AB32	I/O	OV _{DD}	—
LGPL1/LSDWE/cfg_reset_source1	AE37	I/O	OV _{DD}	—
LGPL2/LSDRAS/LOE	AC33	O	OV _{DD}	—
LGPL3/LSDCAS/cfg_reset_source2	AD34	I/O	OV _{DD}	—
LGPL4/LGTA/LUPWAIT/LPBSE	AE35	I/O	OV _{DD}	—
LGPL5/cfg_clkin_div	AF36	I/O	OV _{DD}	—
LCKE	G36	O	OV _{DD}	—
LCLK[0]	J33	O	OV _{DD}	—
LCLK[1]/LCS[6]	J34	O	OV _{DD}	—
LCLK[2]/LCS[7]	G37	O	OV _{DD}	—
LSYNC_OUT	F34	O	OV _{DD}	—
LSYNC_IN	G35	I	OV _{DD}	—
Programmable Interrupt Controller				
MCP_OUT	E34	O	OV _{DD}	2
IRQ0/MCP_IN	C37	I	OV _{DD}	—
IRQ[1]/M1SRCID[4]/M2SRCID[4]/LSRCID[4]	F35	I/O	OV _{DD}	—
IRQ[2]/M1DVAL/M2DVAL/LDVAL	F36	I/O	OV _{DD}	—
IRQ[3]/CORE_SRESET	H34	I/O	OV _{DD}	—

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
No Connect				
NC	AM16, AM17, AM20, AN13, AN16, AN17, AP10, AP11, AP13, AP15, AP18, AR11, AR13, AR14, AR15, AR16, AR17, AR20, AT11, AT12, AT13, AT14, AT16, AT17, AT18, AU10, AU11, AU12, AU13, AU15, AU19	—	—	—

Notes:

1. This pin is an open drain signal. A weak pull-up resistor (1 k Ω) should be placed on this pin to OV_{DD}.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 k Ω) should be placed on this pin to OV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. These are On Die Termination pins, used to control DDR2 memories internal termination resistance.
7. This pin must always be tied to GND.
8. This pin must always be left not connected.
9. Refer to *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* section on “RGMII Pins,” for information about the two UCC2 Ethernet interface options.
10. This pin must always be tied to GV_{DD}.
11. It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor for DDR2.

This figure shows the internal distribution of clocks within the MPC8358E.

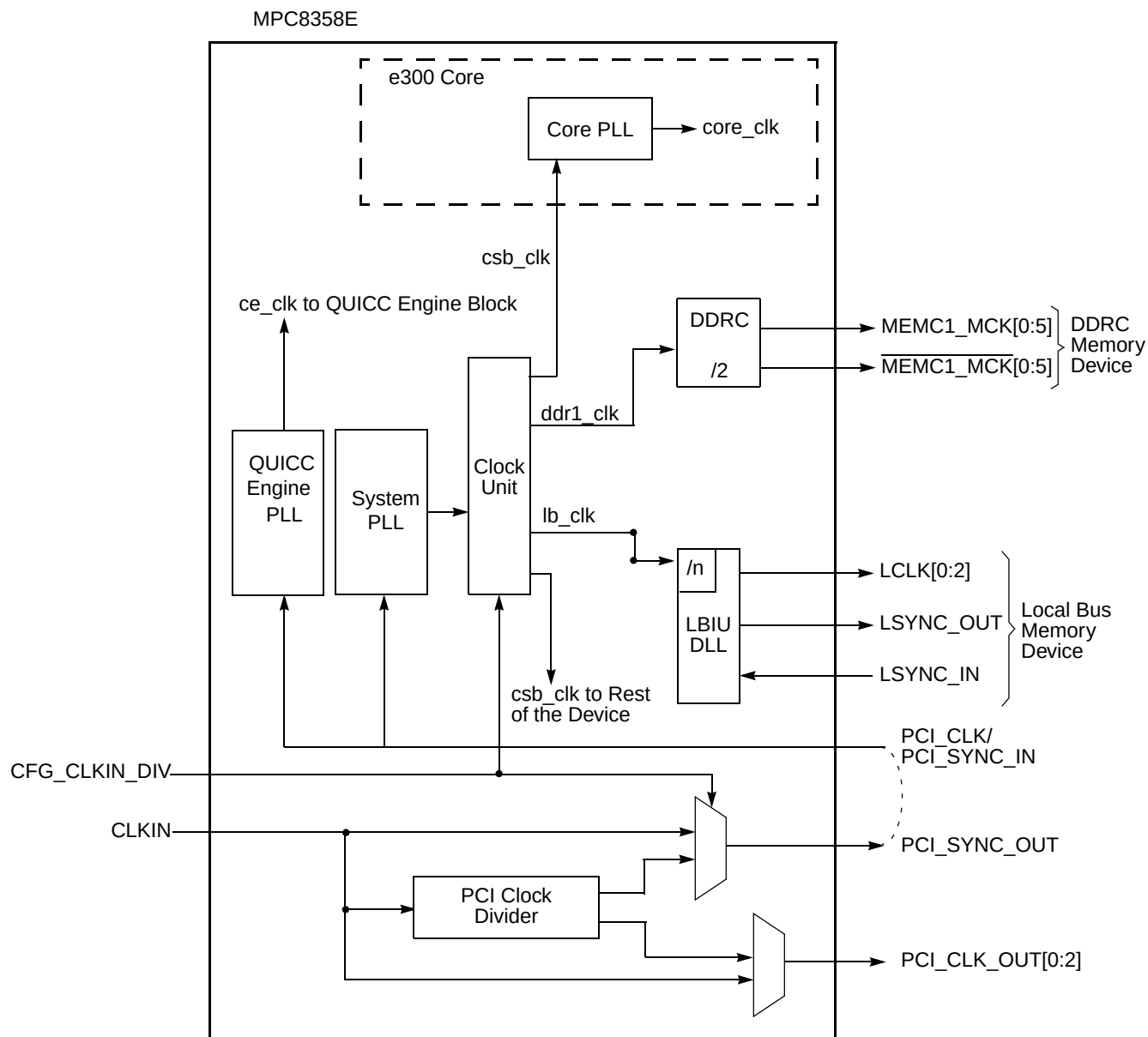


Figure 55. MPC8358E Clock Subsystem

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Note that in PCI host mode, the primary clock input also depends on whether PCI clock outputs are selected with RCWH[PCICKDRV]. When the device is configured as a PCI host device (RCWH[PCIHOST] = 1) and PCI clock output is selected (RCWH[PCICKDRV] = 1), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (+2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCIOEN_n] parameters enable the PCI_CLK_OUT_n, respectively.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input

Table 70. System PLL Multiplication Factors (continued)

RCWL[SPMF]	System PLL Multiplication Factor
1100	× 12
1101	× 13
1110	× 14
1111	× 15

The RCWL[SVCOD] denotes the system PLL VCO internal frequency as shown in this table.

Table 71. System PLL VCO Divider

RCWL[SVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider must be set properly so that the system VCO frequency is in the range of 600–1400 MHz.

The system VCO frequency is derived from the following equations:

- $csb_clk = \{PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)\} \times SPMF$
- System VCO Frequency = $csb_clk \times VCO\ divider$ (if both RCWL[DDRCM] and RCWL[LBCM] are cleared)
OR
- System VCO frequency = $2 \times csb_clk \times VCO\ divider$ (if either RCWL[DDRCM] or RCWL[LBCM] are set).

As described in [Section 21, “Clocking,”](#) the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (csb_clk). This table shows the expected frequency values for the CSB frequency for select csb_clk to CLKIN/PCI_SYNC_IN ratios.

Table 72. CSB Frequency Options

CFG_CLKIN_DIV at Reset ¹	SPMF	csb_clk : Input Clock Ratio ²	Input Clock Frequency (MHz) ²			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2:1				133
Low	0011	3:1				200
Low	0100	4:1				266
Low	0101	5:1				333

Table 74. QUICC Engine Block PLL Multiplication Factors (continued)

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = $\text{RCWL[CEPMF]} / (1 + \text{RCWL[CEPDF]})$
11101	0	× 29
11110	0	× 30
11111	0	× 31
00011	1	× 1.5
00101	1	× 2.5
00111	1	× 3.5
01001	1	× 4.5
01011	1	× 5.5
01101	1	× 6.5
01111	1	× 7.5
10001	1	× 8.5
10011	1	× 9.5
10101	1	× 10.5
10111	1	× 11.5
11001	1	× 12.5
11011	1	× 13.5
11101	1	× 14.5

Note:

1. Reserved modes are not listed.

The RCWL[CEVCOD] denotes the QUICC Engine Block PLL VCO internal frequency as shown in this table.

Table 75. QUICC Engine Block PLL VCO Divider

RCWL[CEVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine block VCO frequency is in the range of 600–1400 MHz. The QUICC Engine block frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine block frequencies should be selected according to the performance requirements.

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JA}$ = junction to board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

22.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

22.2.4 Heat Sinks and Junction-to-Ambient Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-millennium.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Interface material vendors include the following:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

22.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb force (4.5 kg force). If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

Table 81. SVR Settings (continued)

Device	Package	SVR (Rev. 2.0)	SVR (Rev. 2.1)
MPC8358E	TBGA	0x804A_0020	0x804A_0021
MPC8358	TBGA	0x804B_0020	0x804B_0021

25 Document Revision History

This table provides a revision history for this document.

Table 82. Revision History

Rev. Number	Date	Substantive Change(s)
5	09/2011	• Section 2.2.1, "Power-Up Sequencing", added the current limitation "3A to 5A" for the excessive current. • Section 2.1.2, "Power Supply Voltage Specification", Updated the Characteristic for TBGA (MPC8358 & MPC8360 Device) with specific frequency for Core and PLL voltages. • Added table footnote 3 to Table 2. • Applied table footnotes 1 and 2 to Table 10. • Removed table footnotes from Table 19. • Applied table footnote 8 to the last row of Table 40. • Applied table footnotes 8 and 9 to Table 41. • Applied table footnotes 2 and 3 to Table 45. • Removed table footnotes from Table 46. • Applied table footnote to last three rows of Table 65.
4	01/2011	• Updated references to the LCRR register throughout • Removed references to DDR DLL mode in Section 6.2.2, "DDR and DDR2 SDRAM Output AC Timing Specifications". • Changed "Junction-to-Case" to "Junction-to-Ambient" in Section 22.2.4, "Heat Sinks and Junction-to-Ambient Thermal Resistance", and Table 78, "Heat Sinks and Junction-to-Ambient Thermal Resistance of TBGA Package", titles.