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### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8358ezuagdg">https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8358ezuagdg</a>

- 10/100 Mbps Ethernet/IEEE Std. 802.3™ CDMA/CS interface through a media-independent interface (MII, RMII, RGMII)<sup>1</sup>
- 1000 Mbps Ethernet/IEEE 802.3 CDMA/CS interface through a media-independent interface (GMII, RGMII, TBI, RTBI) on UCC1 and UCC2
- 9.6-Kbyte jumbo frames
- ATM full-duplex SAR, up to 622 Mbps (OC-12/STM-4), AAL0, AAL1, and AAL5 in accordance ITU-T I.363.5
- ATM AAL2 CPS, SSSAR, and SSTED up to 155 Mbps (OC-3/STM-1) Mbps full duplex (with 4 CPS packets per cell) in accordance ITU-T I.366.1 and I.363.2
- ATM traffic shaping for CBR, VBR, UBR, and GFR traffic types compatible with ATM forum TM4.1 for up to 64-Kbyte simultaneous ATM channels
- ATM AAL1 structured and unstructured circuit emulation service (CES 2.0) in accordance with ITU-T I.163.1 and ATM Forum af-vtoa-00-0078.000
- IMA (Inverse Multiplexing over ATM) for up to 31 IMA links over 8 IMA groups in accordance with the ATM forum AF-PHY-0086.000 (Version 1.0) and AF-PHY-0086.001 (Version 1.1)
- ATM Transmission Convergence layer support in accordance with ITU-T I.432
- ATM OAM handling features compatible with ITU-T I.610
- PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686, and 3153
- IP support for IPv4 packets including TOS, TTL, and header checksum processing
- Ethernet over first mile IEEE 802.3ah
- Shim header
- Ethernet-to-Ethernet/AAL5/AAL2 inter-working
- L2 Ethernet switching using MAC address or IEEE Std. 802.1P/Q™ VLAN tags
- ATM (AAL2/AAL5) to Ethernet (IP) interworking in accordance with RFC2684 including bridging of ATM ports to Ethernet ports
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- AAL2 protocol rate up to 4 CPS at OC-3/STM-1 rate
- Packet over Sonet (POS) up to 622-Mbps full-duplex 124 MultiPHY
- POS hardware; microcode must be loaded as an IRAM package
- Transparent up to 70-Mbps full-duplex
- HDLC up to 70-Mbps full-duplex
- HDLC BUS up to 10 Mbps
- Asynchronous HDLC
- UART
- BISYNC up to 2 Mbps
- User-programmable Virtual FIFO size
- QUICC multichannel controller (QMC) for 64 TDM channels
- One multichannel communication controller (MCC) only on the MPC8360E supporting the following:
  - 256 HDLC or transparent channels
  - 128 SS7 channels
  - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces
- Two UTOPIA/POS interfaces on the MPC8360E supporting 124 MultiPHY each (optional 2\*128 MultiPHY with extended address) and one UTOPIA/POS interface on the MPC8358E supporting 31/124 MultiPHY
- Two serial peripheral interfaces (SPI); SPI2 is dedicated to Ethernet PHY management

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<sup>1</sup>.SMII or SGMII media-independent interface is not currently supported.

**Table 4. MPC8360E TBGA Core Power Dissipation<sup>1</sup> (continued)**

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
667	333	500	6.1	6.8	W	2, 3, 5, 9

**Notes:**

1. The values do not include I/O supply power ( $OV_{DD}$ ,  $LV_{DD}$ ,  $GV_{DD}$ ) or  $AV_{DD}$ . For I/O power values, see [Table 6](#).
2. Typical power is based on a voltage of  $V_{DD} = 1.2$  V or 1.3 V, a junction temperature of  $T_J = 105^\circ\text{C}$ , and a Dhrystone benchmark application.
3. Thermal solutions need to design to a value higher than typical power on the end application,  $T_A$  target, and I/O power.
4. Maximum power is based on a voltage of  $V_{DD} = 1.2$  V, WC process, a junction  $T_J = 105^\circ\text{C}$ , and an artificial smoke test.
5. Maximum power is based on a voltage of  $V_{DD} = 1.3$  V for applications that use 667 MHz (CPU)/500 (QE) with WC process, a junction  $T_J = 105^\circ\text{C}$ , and an artificial smoke test.
6. Typical power is based on a voltage of  $V_{DD} = 1.3$  V, a junction temperature of  $T_J = 70^\circ\text{C}$ , and a Dhrystone benchmark application.
7. Maximum power is based on a voltage of  $V_{DD} = 1.3$  V for applications that use 667 MHz (CPU) or 500 (QE) with WC process, a junction  $T_J = 70^\circ\text{C}$ , and an artificial smoke test.
8. This frequency combination is only available for rev. 2.0 silicon.
9. This frequency combination is not available for rev. 2.0 silicon.

**Table 5. MPC8358E TBGA Core Power Dissipation<sup>1</sup>**

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	300	4.1	4.5	W	2, 3, 4
400	266	400	4.5	5.0	W	2, 3, 4

**Notes:**

1. The values do not include I/O supply power ( $OV_{DD}$ ,  $LV_{DD}$ ,  $GV_{DD}$ ) or  $AV_{DD}$ . For I/O power values, see [Table 6](#).
2. Typical power is based on a voltage of  $V_{DD} = 1.2$  V, a junction temperature of  $T_J = 105^\circ\text{C}$ , and a Dhrystone benchmark application.
3. Thermal solutions need to design to a value higher than typical power on the end application,  $T_A$  target, and I/O power.
4. Maximum power is based on a voltage of  $V_{DD} = 1.2$  V, WC process, a junction  $T_J = 105^\circ\text{C}$ , and an artificial smoke test.

## 5.2 RESET AC Electrical Characteristics

This section describes the AC electrical specifications for the reset initialization timing requirements of the device. This table provides the reset initialization AC timing specifications for the DDR SDRAM component(s).

**Table 11. RESET Initialization Timing Specifications**

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow	32	—	$t_{\text{PCI\_SYNC\_IN}}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the device is in PCI host mode	32	—	$t_{\text{CLKIN}}$	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the device is in PCI agent mode	32	—	$t_{\text{PCI\_SYNC\_IN}}$	1
$\overline{\text{HRESET}}/\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{\text{PCI\_SYNC\_IN}}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{\text{PCI\_SYNC\_IN}}$	1
Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode	4	—	$t_{\text{CLKIN}}$	2
Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode	4	—	$t_{\text{PCI\_SYNC\_IN}}$	1
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the device to turn off POR config signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the device to turn on POR config signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{\text{PCI\_SYNC\_IN}}$	1, 3

**Notes:**

1.  $t_{\text{PCI\_SYNC\_IN}}$  is the clock period of the input clock applied to PCI\_SYNC\_IN. When the device is in PCI host mode the primary clock is applied to the CLKIN input, and PCI\_SYNC\_IN period depends on the value of CFG\_CLKIN\_DIV. Refer *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
2.  $t_{\text{CLKIN}}$  is the clock period of the input clock applied to CLKIN. It is only valid when the device is in PCI host mode. Refer *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
3. POR config signals consists of CFG\_RESET\_SOURCE[0:2] and CFG\_CLKIN\_DIV.

This table provides the PLL and DLL lock times.

**Table 12. PLL and DLL Lock Times**

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	$\mu\text{s}$	—
DLL lock times	7680	122,880	csb_clk cycles	1, 2

**Notes:**

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb\_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The csb\_clk is determined by the CLKIN and system PLL ratio. See [Section 21, "Clocking,"](#) for more information.

## 6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 21 and Table 22 provide the output AC timing specifications and measurement conditions for the DDR and DDR2 SDRAM interface.

**Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode**

At recommended operating conditions with  $GV_{DD}$  of (1.8 V or 2.5 V)  $\pm$  5%.

Parameter <sup>8</sup>	Symbol <sup>1</sup>	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/ $\overline{MCK[n]}$ crossing)	$t_{MCK}$	6	10	ns	2
Skew between any MCK to ADDR/CMD 333 MHz 266 MHz 200 MHz	$t_{AOSKEW}$	-1.0 -1.1 -1.2	0.2 0.3 0.4	ns	3
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz 200 MHz	$t_{DDKHAS}$	2.1 2.8 3.5	—	ns	4
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz—DDR1 266 MHz—DDR2 200 MHz	$t_{DDKHAX}$	2.0 2.7 2.8 3.5	—	ns	4
$\overline{MCS}(n)$ output setup with respect to MCK 333 MHz 266 MHz 200 MHz	$t_{DDKHCS}$	2.1 2.8 3.5	—	ns	4
$\overline{MCS}(n)$ output hold with respect to MCK 333 MHz 266 MHz 200 MHz	$t_{DDKHCSX}$	2.0 2.7 3.5	—	ns	4
MCK to MDQS	$t_{DDKMH}$	-0.8	0.7	ns	5, 9
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	$t_{DDKHDS},$ $t_{DDKLDS}$	0.7 1.0 1.2	—	ns	6
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	$t_{DDKHDX},$ $t_{DDKLDX}$	0.7 1.0 1.2	—	ns	6
MDQS preamble start	$t_{DDKHMP}$	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	7

## 8.2.1.2 GMII Receive AC Timing Specifications

This table provides the GMII receive AC timing specifications.

**Table 28. GMII Receive AC Timing Specifications**

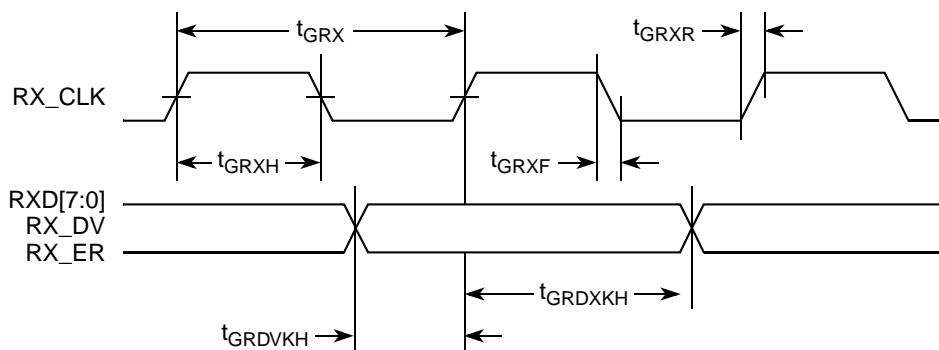
At recommended operating conditions with  $V_{DD}/OV_{DD}$  of  $3.3\text{ V} \pm 10\%$ .

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit	Notes
RX_CLK clock period	$t_{GRX}$	—	8.0	—	ns	—
RX_CLK duty cycle	$t_{GRXH}/t_{GRX}$	40	—	60	%	—
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	$t_{GRDVKH}$	2.0	—	—	ns	—
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	$t_{GRDXKH}$	0.2	—	—	ns	2
RX_CLK clock rise time, (20% to 80%)	$t_{GRXR}$	—	—	1.0	ns	—
RX_CLK clock fall time, (80% to 20%)	$t_{GRXF}$	—	—	1.0	ns	—

**Notes:**

- The symbols used for timing specifications follow the pattern of  $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$  for inputs and  $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{GRDVKH}$  symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the  $t_{RX}$  clock reference (K) going to the high state (H) or setup time. Also,  $t_{GRDXKL}$  symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the  $t_{GRX}$  clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of  $t_{GRX}$  represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- In rev. 2.0 silicon, due to errata,  $t_{GRDXKH}$  minimum is 0.5 which is not compliant with the standard. Refer to Errata *QE\_ENET18* in *Chip Errata for the MPC8360E, Rev. 1*.

This figure shows the GMII receive AC timing diagram.



**Figure 11. GMII Receive AC Timing Diagram**

## 8.2.5 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

**Table 35. RGMII and RTBI AC Timing Specifications**

At recommended operating conditions with  $V_{DD}$  of 2.5 V  $\pm$  5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	$t_{SKRGTKHDX}$ $t_{SKRGTKHDV}$	−0.5 —	—	— 0.5	ns	7
Data to clock input skew (at receiver)	$t_{SKRGDXKH}$ $t_{SKRGDVKH}$	1.0 —	—	— 2.6	ns	2
Clock cycle duration	$t_{RGT}$	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	$t_{RGTH}/t_{RGT}$	45	50	55	%	4, 5
Duty cycle for 10BASE-T and 100BASE-TX	$t_{RGTH}/t_{RGT}$	40	50	60	%	3, 5
Rise time (20–80%)	$t_{RGTR}$	—	—	0.75	ns	—
Fall time (20–80%)	$t_{RGTF}$	—	—	0.75	ns	—
GTX_CLK125 reference clock period	$t_{G125}$	—	8.0	—	ns	6
GTX_CLK125 reference clock duty cycle	$t_{G125H}/t_{G125}$	47	—	53	%	—

**Notes:**

- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of  $t_{RGT}$  represents the TBI (T) receive (Rx) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns can be added to the associated clock signal.
- For 10 and 100 Mbps,  $t_{RGT}$  scales to 400 ns  $\pm$  40 ns and 40 ns  $\pm$  4 ns, respectively.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three  $t_{RGT}$  of the lowest speed transitioned between.
- Duty cycle reference is  $V_{DD}/2$ .
- This symbol is used to represent the external GTX\_CLK125 and does not follow the original symbol naming convention.
- In rev. 2.0 silicon, due to errata,  $t_{SKRGTKHDX}$  minimum is −2.3 ns and  $t_{SKRGTKHDV}$  maximum is 1 ns for UCC1, 1.2 ns for UCC2 option 1, and 1.8 ns for UCC2 option 2. In rev. 2.1 silicon, due to errata,  $t_{SKRGTKHDX}$  minimum is −0.65 ns for UCC2 option 1 and −0.9 for UCC2 option 2, and  $t_{SKRGTKHDV}$  maximum is 0.75 ns for UCC1 and UCC2 option 1 and 0.85 for UCC2 option 2. Refer to Errata QE\_ENET10 in *Chip Errata for the MPC8360E, Rev. 1*. UCC1 does meet  $t_{SKRGTKHDX}$  minimum for rev. 2.1 silicon.

### 8.3.3 IEEE 1588 Timer AC Specifications

This table provides the IEEE 1588 timer AC specifications.

**Table 38. IEEE 1588 Timer AC Specifications**

Parameter	Symbol	Min	Max	Unit	Notes
Timer clock frequency	$t_{TMRCK}$	0	70	MHz	1
Input setup to timer clock	$t_{TMRCKS}$	—	—	—	2, 3
Input hold from timer clock	$t_{TMRCKH}$	—	—	—	2, 3
Output clock to output valid	$t_{GCLKNV}$	0	6	ns	—
Timer alarm to output valid	$t_{TMRAL}$	—	—	—	2

**Notes:**

1. The timer can operate on `rtc_clock` or `tmr_clock`. These clocks get muxed and any one of them can be selected. The minimum and maximum requirement for both `rtc_clock` and `tmr_clock` are the same.
2. These are asynchronous signals.
3. Inputs need to be stable at least one TMR clock.

## 9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8360E/58E.

### 9.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface.

**Table 39. Local Bus DC Electrical Characteristics**

Parameter	Symbol	Min	Max	Unit
High-level input voltage	$V_{IH}$	2	$OV_{DD} + 0.3$	V
Low-level input voltage	$V_{IL}$	-0.3	0.8	V
High-level output voltage, $I_{OH} = -100 \mu A$	$V_{OH}$	$OV_{DD} - 0.4$	—	V
Low-level output voltage, $I_{OL} = 100 \mu A$	$V_{OL}$	—	0.2	V
Input current	$I_{IN}$	—	$\pm 10$	$\mu A$

### 9.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface of the device.

**Table 40. Local Bus General Timing Parameters—DLL Enabled**

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Local bus cycle time	$t_{LBK}$	7.5	—	ns	2
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	1.7	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.9	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4



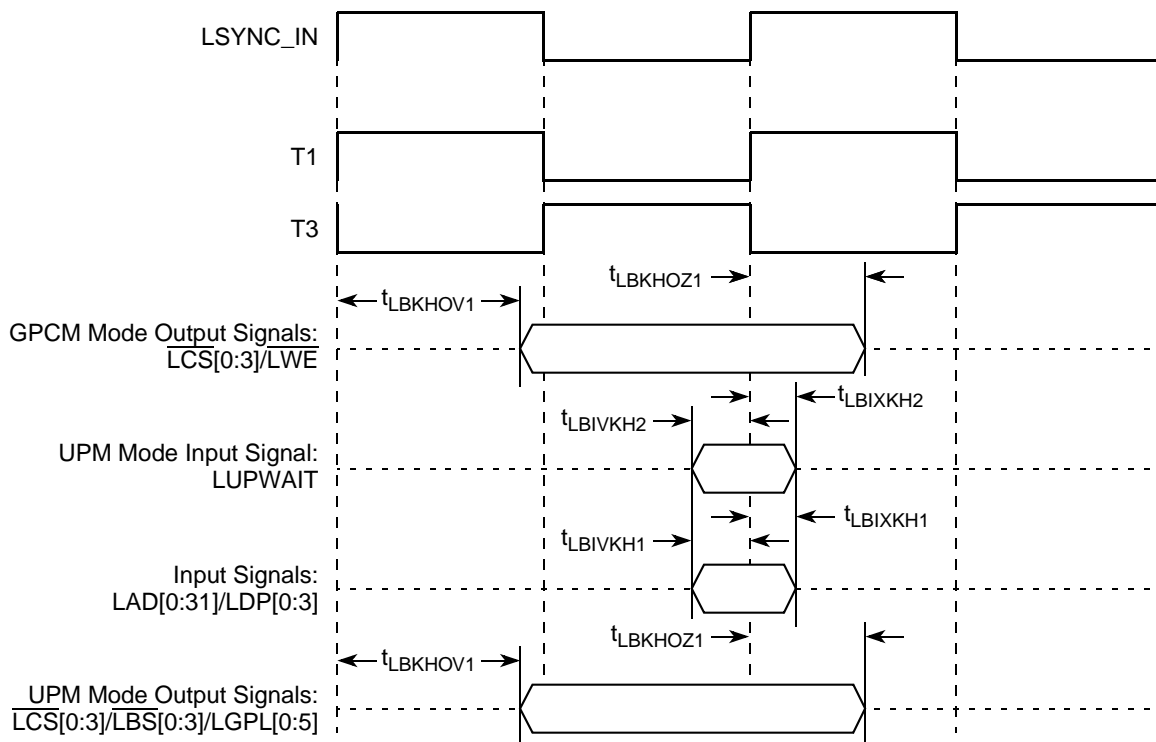


Figure 25. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Enabled)

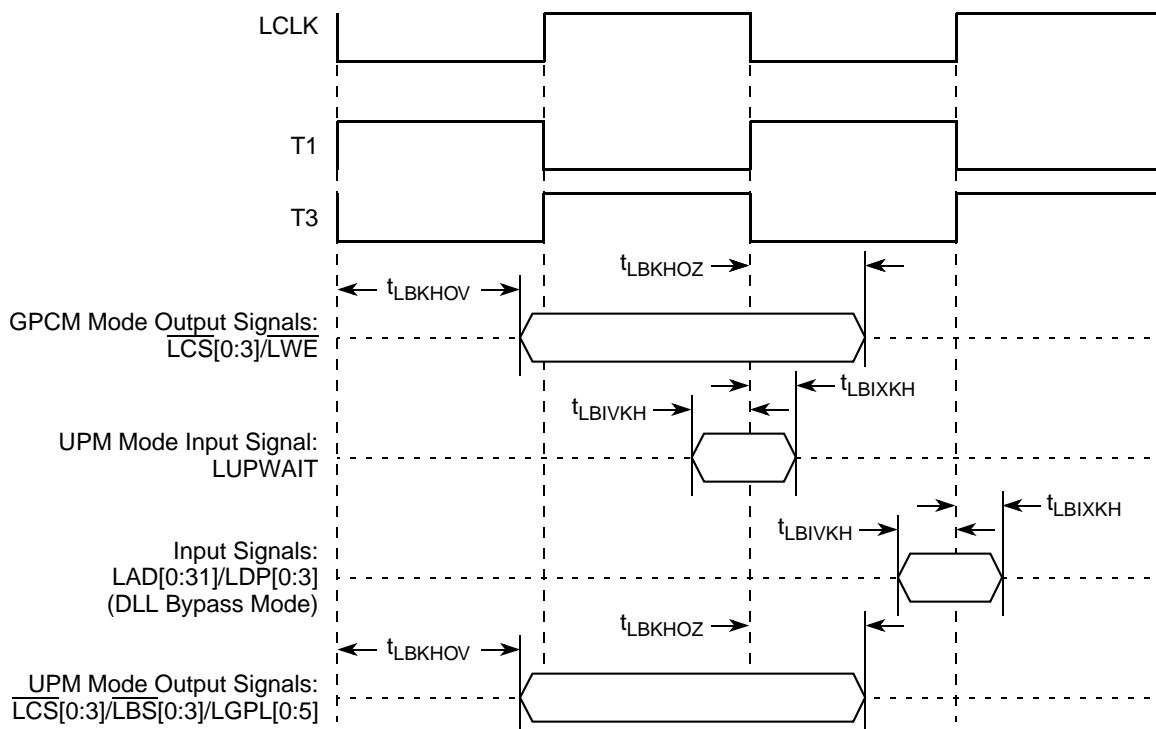


Figure 26. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Bypass Mode)

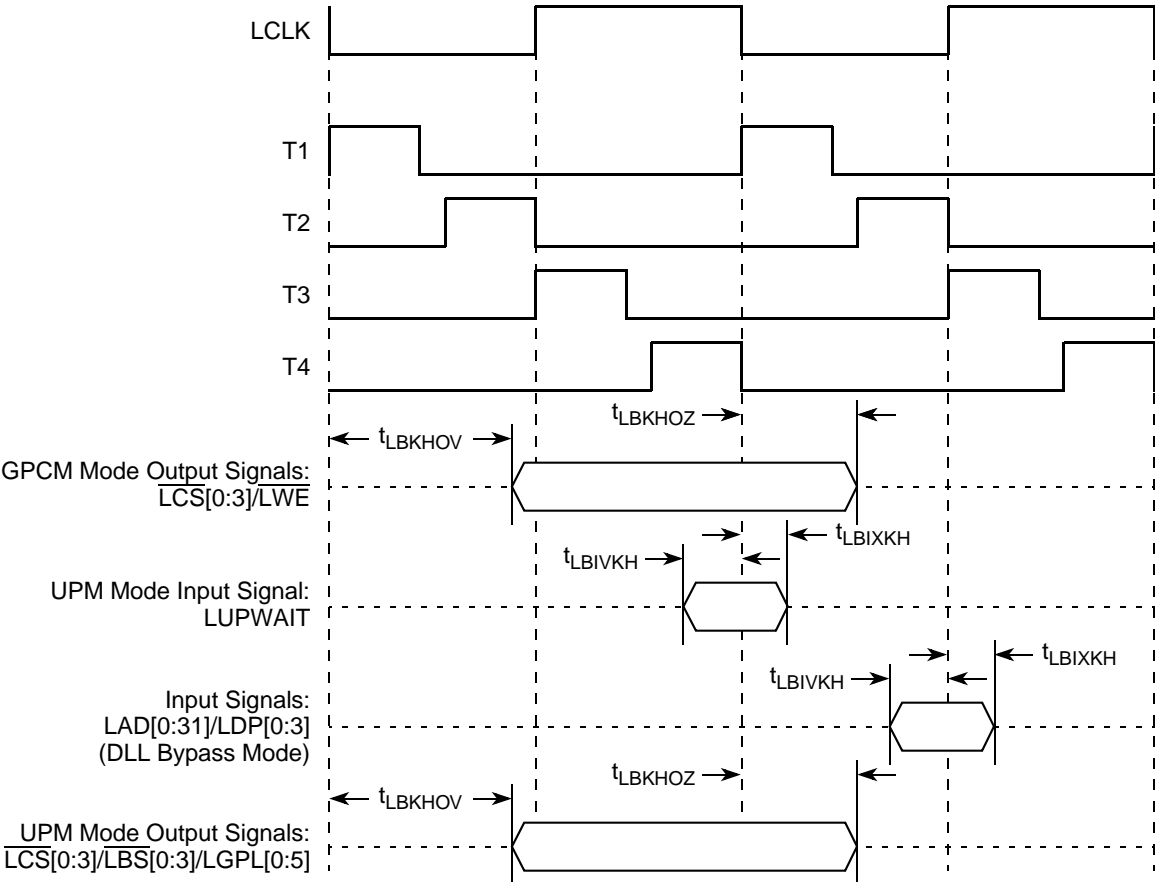


Figure 27. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (DLL Bypass Mode)

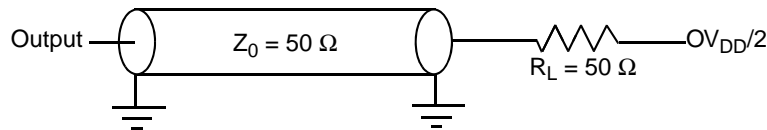
**Table 56. SPI AC Timing Specifications<sup>1</sup>**

Characteristic	Symbol <sup>2</sup>	Min	Max	Unit
SPI inputs—Slave mode (external clock) input hold time	$t_{NEIXKH}$	2	—	ns

**Notes:**

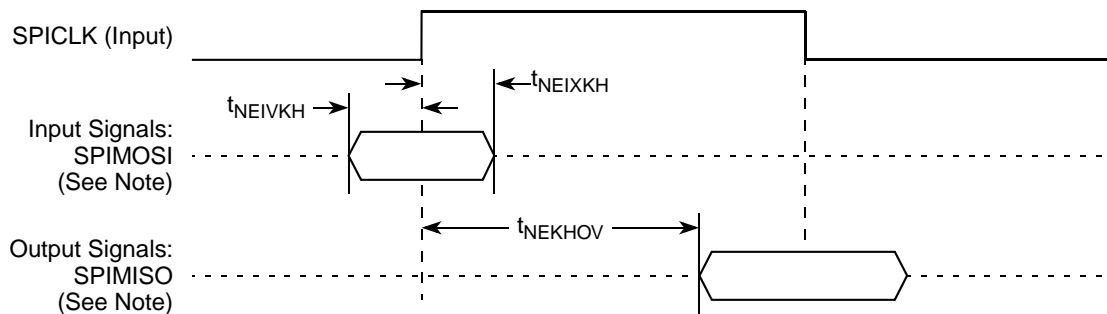
- Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of  $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$  for inputs and  $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{NIKH OV}$  symbolizes the NMSI outputs internal timing (NI) for the time  $t_{SPI}$  memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

This figure provides the AC test load for the SPI.


**Figure 41. SPI AC Test Load**

These figures represent the AC timing from Table 56. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

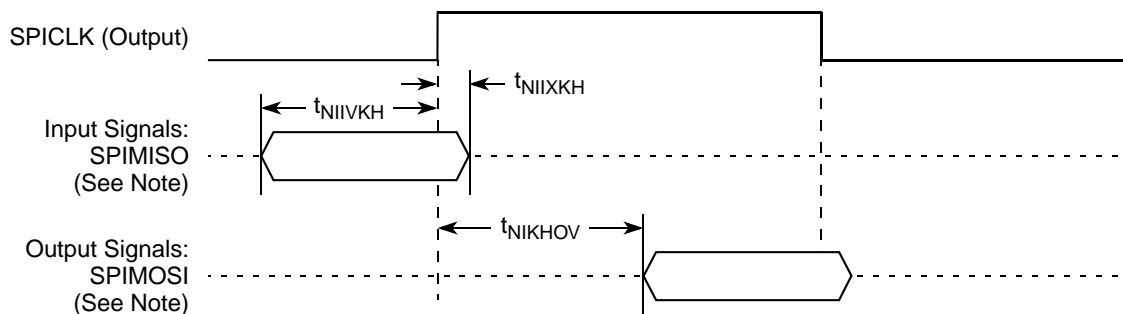
This figure shows the SPI timing in slave mode (external clock).



**Note:** The clock edge is selectable on SPI.

**Figure 42. SPI AC Timing in Slave Mode (External Clock) Diagram**

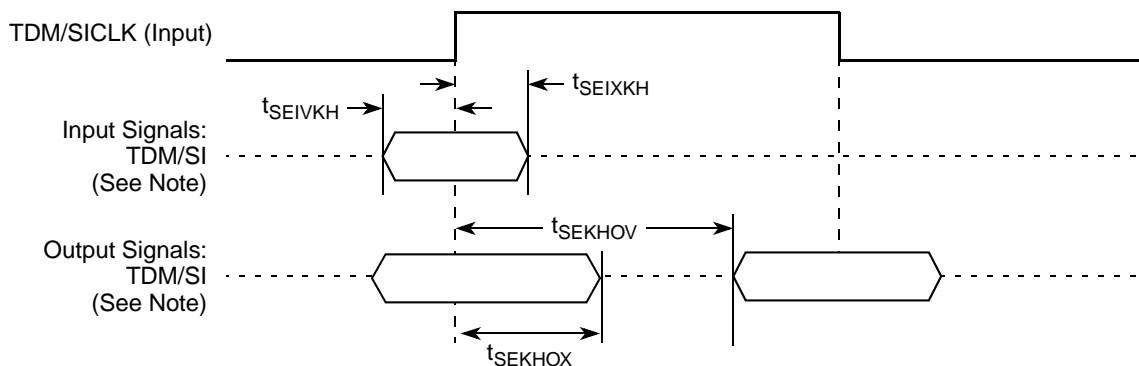
This figure shows the SPI timing in Master mode (internal clock).



**Note:** The clock edge is selectable on SPI.

**Figure 43. SPI AC Timing in Master Mode (Internal Clock) Diagram**

This figure shows the TDM/SI timing with external clock.



**Note:** The clock edge is selectable on TDM/SI

**Figure 45. TDM/SI AC Timing (External Clock) Diagram**

## 17.3 UTOPIA/POS

This section describes the DC and AC electrical specifications for the UTOPIA/POS of the MPC8360E/58E.

## 17.4 UTOPIA/POS DC Electrical Characteristics

This table provides the DC electrical characteristics for the device UTOPIA.

**Table 59. UTOPIA DC Electrical Characteristics**

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	$V_{OH}$	$I_{OH} = -8.0 \text{ mA}$	2.4	—	V
Output low voltage	$V_{OL}$	$I_{OL} = 8.0 \text{ mA}$	—	0.5	V
Input high voltage	$V_{IH}$	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	$V_{IL}$	—	-0.3	0.8	V
Input current	$I_{IN}$	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	$\pm 10$	$\mu\text{A}$

## 17.5 UTOPIA/POS AC Timing Specifications

This table provides the UTOPIA input and output AC timing specifications.

**Table 60. UTOPIA AC Timing Specifications<sup>1</sup>**

Characteristic	Symbol <sup>2</sup>	Min	Max	Unit	Notes
UTOPIA outputs—Internal clock delay	$t_{UIKHOV}$	0	11.5	ns	—
UTOPIA outputs—External clock delay	$t_{UEKHOV}$	1	11.6	ns	—
UTOPIA outputs—Internal clock high impedance	$t_{UIKHOX}$	0	8.0	ns	—
UTOPIA outputs—External clock high impedance	$t_{UEKHOX}$	1	10.0	ns	—
UTOPIA inputs—Internal clock input setup time	$t_{UIIVKH}$	6	—	ns	—
UTOPIA inputs—External clock input setup time	$t_{UEIVKH}$	4	—	ns	3

This figure shows the UTOPIA timing with internal clock.

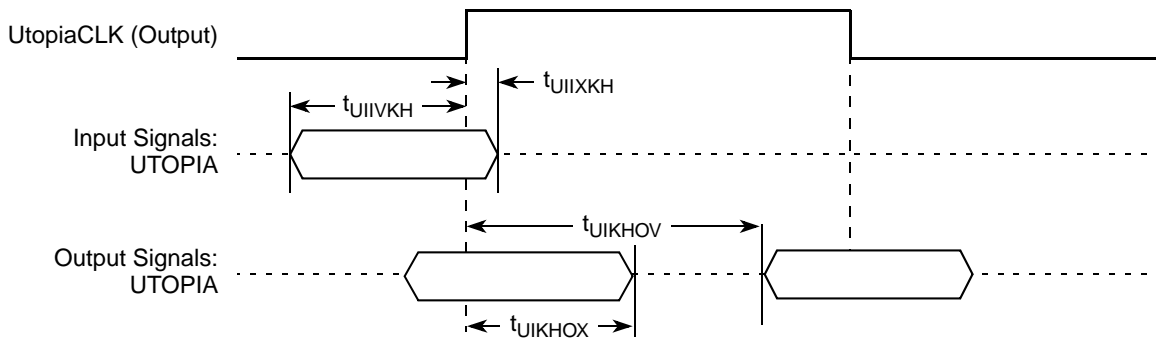


Figure 48. UTOPIA AC Timing (Internal Clock) Diagram

## 18 HDLC, BISYNC, Transparent, and Synchronous UART

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent, and synchronous UART protocols of the MPC8360E/58E.

### 18.1 HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

This table provides the DC electrical characteristics for the device HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 61. HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	$V_{OH}$	$I_{OH} = -2.0 \text{ mA}$	2.4	—	V
Output low voltage	$V_{OL}$	$I_{OL} = 3.2 \text{ mA}$	—	0.5	V
Input high voltage	$V_{IH}$	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	$V_{IL}$	—	-0.3	0.8	V
Input current	$I_{IN}$	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	$\pm 10$	$\mu\text{A}$

### 18.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

These tables provide the input and output AC timing specifications for HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 62. HDLC, BISYNC, and Transparent AC Timing Specifications<sup>1</sup>

Characteristic	Symbol <sup>2</sup>	Min	Max	Unit
Outputs—Internal clock delay	$t_{HIKHOV}$	0	11.2	ns
Outputs—External clock delay	$t_{HEKHOV}$	1	10.8	ns

# 20.2 Mechanical Dimensions of the TBGA Package

This figure depicts the mechanical dimensions and bottom surface nomenclature of the device, 740-TBGA package.

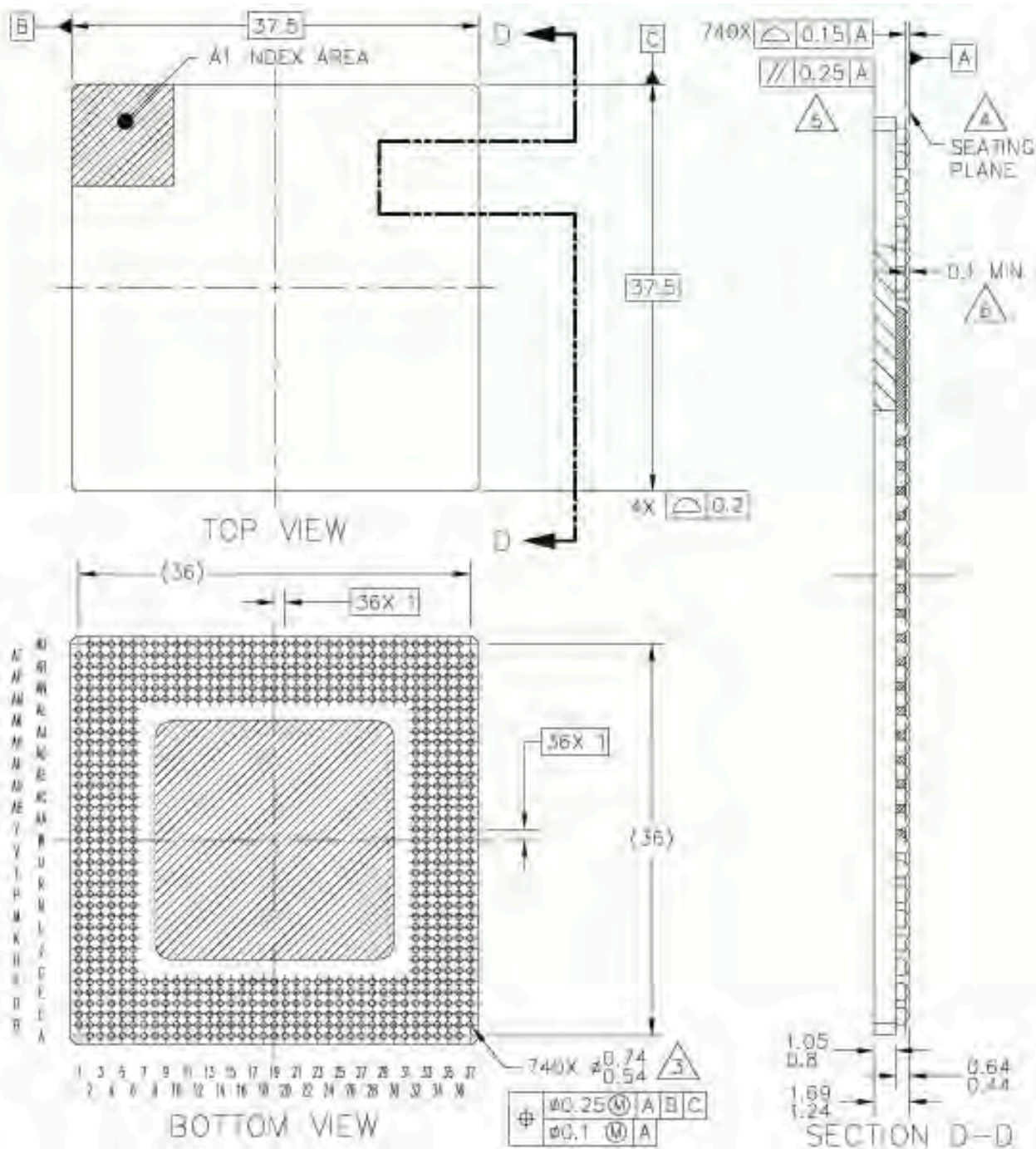


Figure 53. Mechanical Dimensions and Bottom Surface Nomenclature of the TBGA Package

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
<b>PMC</b>				
$\overline{\text{QUIESCE}}$	B36	O	$\text{OV}_{\text{DD}}$	—
<b>System Control</b>				
$\overline{\text{PORESET}}$	L37	I	$\text{OV}_{\text{DD}}$	—
$\overline{\text{HRESET}}$	L36	I/O	$\text{OV}_{\text{DD}}$	1
$\overline{\text{SRESET}}$	M33	I/O	$\text{OV}_{\text{DD}}$	2
<b>Thermal Management</b>				
THERM0	AP19	I	$\text{GV}_{\text{DD}}$	—
THERM1	AT31	I	$\text{GV}_{\text{DD}}$	—
<b>Power and Ground Signals</b>				
$\text{AV}_{\text{DD}1}$	K35	Power for LBIU DLL (1.2 V)	$\text{AV}_{\text{DD}1}$	—
$\text{AV}_{\text{DD}2}$	K36	Power for CE PLL (1.2 V)	$\text{AV}_{\text{DD}2}$	—
$\text{AV}_{\text{DD}5}$	AM29	Power for e300 PLL (1.2 V)	$\text{AV}_{\text{DD}5}$	—
$\text{AV}_{\text{DD}6}$	K37	Power for system PLL (1.2 V)	$\text{AV}_{\text{DD}6}$	—
GND	A2, A8, A13, A19, A22, A25, A31, A33, A36, B7, B12, B24, B27, B30, C4, C6, C9, C15, C26, C32, D3, D8, D11, D14, D17, D19, D23, D27, E7, E13, E25, E30, E36, F4, F37, G34, H1, H5, H32, H33, J4, J32, J37, K1, L3, L5, L33, L34, M1, M34, M35, N37, P2, P5, P35, P36, R4, T3, U1, U5, U35, V37, W1, W4, W33, W36, Y34, AA3, AA5, AC3, AC32, AC35, AD1, AD37, AE4, AE34, AE36, AF33, AG4, AG6, AG32, AH35, AJ1, AJ4, AJ32, AJ35, AJ37, AK36, AL3, AL34, AM4, AN6, AN23, AN30, AP8, AP12, AP14, AP16, AP17, AP20, AP25, AR6, AR8, AR9, AR19, AR24, AR31, AR35, AR37, AT4, AT10, AT19, AT20, AT25, AU14, AU22, AU28, AU35	—	—	—
$\text{GV}_{\text{DD}}$	AD4, AE3, AF1, AF5, AF35, AF37, AG2, AG36, AH33, AH34, AK5, AM1, AM35, AM37, AN2, AN10, AN11, AN12, AN14, AN32, AN36, AP5, AP23, AP28, AR1, AR7, AR10, AR12, AR21, AR25, AR27, AR33, AT15, AT22, AT28, AT33, AU2, AU5, AU16, AU31, AU36	Power for DDR DRAM I/O voltage (2.5 or 1.8 V)	$\text{GV}_{\text{DD}}$	—

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{IRQ}}[4:5]$	G33, G32	I/O	$\text{OV}_{\text{DD}}$	—
$\overline{\text{IRQ}}[6]/\overline{\text{LCS}}[6]/\overline{\text{CKSTOP\_OUT}}$	E35	I/O	$\text{OV}_{\text{DD}}$	—
$\overline{\text{IRQ}}[7]/\overline{\text{LCS}}[7]/\overline{\text{CKSTOP\_IN}}$	H36	I/O	$\text{OV}_{\text{DD}}$	—
<b>DUART</b>				
UART1_SOUT/M1SRCID[0]/M2SRCID[0]/LSRCID[0]	E32	O	$\text{OV}_{\text{DD}}$	—
UART1_SIN/M1SRCID[1]/M2SRCID[1]/LSRCID[1]	B34	I/O	$\text{OV}_{\text{DD}}$	—
$\overline{\text{UART1\_CTS}}$ /M1SRCID[2]/M2SRCID[2]/LSRCID[2]	C34	I/O	$\text{OV}_{\text{DD}}$	—
$\overline{\text{UART1\_RTS}}$ /M1SRCID[3]/M2SRCID[3]/LSRCID[3]	A35	O	$\text{OV}_{\text{DD}}$	—
<b>I<sup>2</sup>C Interface</b>				
IIC1_SDA	D34	I/O	$\text{OV}_{\text{DD}}$	2
IIC1_SCL	B35	I/O	$\text{OV}_{\text{DD}}$	2
IIC2_SDA	E33	I/O	$\text{OV}_{\text{DD}}$	2
IIC2_SCL	C35	I/O	$\text{OV}_{\text{DD}}$	2
<b>QUICC Engine</b>				
CE_PA[0]	F8	I/O	$\text{LV}_{\text{DD0}}$	—
CE_PA[1:2]	AH1, AG5	I/O	$\text{OV}_{\text{DD}}$	—
CE_PA[3:7]	F6, D4, C3, E5, A3	I/O	$\text{LV}_{\text{DD0}}$	—
CE_PA[8]	AG3	I/O	$\text{OV}_{\text{DD}}$	—
CE_PA[9:12]	F7, B3, E6, B4	I/O	$\text{LV}_{\text{DD0}}$	—
CE_PA[13:14]	AG1, AF6	I/O	$\text{OV}_{\text{DD}}$	—
CE_PA[15]	B2	I/O	$\text{LV}_{\text{DD0}}$	—
CE_PA[16]	AF4	I/O	$\text{OV}_{\text{DD}}$	—
CE_PA[17:21]	B16, A16, E17, A17, B17	I/O	$\text{LV}_{\text{DD1}}$	—
CE_PA[22]	AF3	I/O	$\text{OV}_{\text{DD}}$	—
CE_PA[23:26]	C18, D18, E18, A18	I/O	$\text{LV}_{\text{DD1}}$	—
CE_PA[27:28]	AF2, AE6	I/O	$\text{OV}_{\text{DD}}$	—
CE_PA[29]	B19	I/O	$\text{LV}_{\text{DD1}}$	—
CE_PA[30]	AE5	I/O	$\text{OV}_{\text{DD}}$	—
CE_PA[31]	F16	I/O	$\text{LV}_{\text{DD1}}$	—



Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
CE_PB[0:27]	AE2, AE1, AD5, AD3, AD2, AC6, AC5, AC4, AC2, AC1, AB5, AB4, AB3, AB1, AA6, AA4, AA2, Y6, Y4, Y3, Y2, Y1, W6, W5, W2, V5, V3, V2	I/O	OV <sub>DD</sub>	—
CE_PC[0:1]	V1, U6	I/O	OV <sub>DD</sub>	
CE_PC[2:3]	C16, A15	I/O	LV <sub>DD</sub> 1	—
CE_PC[4:6]	U4, U3, T6	I/O	OV <sub>DD</sub>	—
CE_PC[7]	C19	I/O	LV <sub>DD</sub> 2	—
CE_PC[8:9]	A4, C5	I/O	LV <sub>DD</sub> 0	—
CE_PC[10:30]	T5, T4, T2, T1, R5, R3, R1, C11, D12, F13, B10, C10, E12, A9, B8, D10, A14, E15, B14, D15, AH2	I/O	OV <sub>DD</sub>	—
CE_PD[0:27]	E11, D9, C8, F11, A7, E9, C7, A6, F10, B6, D7, E8, B5, A5, C2, E4, F5, B1, D2, G5, D1, E2, H6, F3, E1, F2, G3, H4	I/O	OV <sub>DD</sub>	—
CE_PE[0:31]	K3, J2, F1, G2, J5, H3, G1, H2, K6, J3, K5, K4, L6, P6, P4, P3, P1, N4, N5, N2, N1, M2, M3, M5, M6, L1, L2, L4, E14, C13, C14, B13	I/O	OV <sub>DD</sub>	—
CE_PF[0:3]	F14, D13, A12, A11	I/O	OV <sub>DD</sub>	—
<b>Clocks</b>				
PCI_CLK_OUT[0]/CE_PF[26]	B22	I/O	LV <sub>DD</sub> 2	—
PCI_CLK_OUT[1:2]/CE_PF[27:28]	D22, A23	I/O	OV <sub>DD</sub>	—
CLKIN	E37	I	OV <sub>DD</sub>	—
PCI_CLOCK/PCI_SYNC_IN	M36	I	OV <sub>DD</sub>	—
PCI_SYNC_OUT/CE_PF[29]	D37	I/O	OV <sub>DD</sub>	3
<b>JTAG</b>				
TCK	K33	I	OV <sub>DD</sub>	—
TDI	K34	I	OV <sub>DD</sub>	4
TDO	H37	O	OV <sub>DD</sub>	3
TMS	J36	I	OV <sub>DD</sub>	4
TRST	L32	I	OV <sub>DD</sub>	4
<b>Test</b>				
TEST	L35	I	OV <sub>DD</sub>	7
TEST_SEL	AU34	I	GV <sub>DD</sub>	10
<b>PMC</b>				
QUIESCE	B36	O	OV <sub>DD</sub>	—
<b>System Control</b>				

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PORESET	L37	I	OV <sub>DD</sub>	—
HRESET	L36	I/O	OV <sub>DD</sub>	1
SRESET	M33	I/O	OV <sub>DD</sub>	2
Thermal Management				
THERM0	AP19	I	GV <sub>DD</sub>	—
THERM1	AT31	I	GV <sub>DD</sub>	—
Power and Ground Signals				
AV <sub>DD</sub> 1	K35	Power for LBIU DLL (1.2 V)	AV <sub>DD</sub> 1	—
AV <sub>DD</sub> 2	K36	Power for CE PLL (1.2 V)	AV <sub>DD</sub> 2	—
AV <sub>DD</sub> 5	AM29	Power for e300 PLL (1.2 V)	AV <sub>DD</sub> 5	—
AV <sub>DD</sub> 6	K37	Power for system PLL (1.2 V)	AV <sub>DD</sub> 6	—
GND	A2, A8, A13, A19, A22, A25, A31, A33, A36, B7, B12, B24, B27, B30, C4, C6, C9, C15, C26, C32, D3, D8, D11, D14, D17, D19, D23, D27, E7, E13, E25, E30, E36, F4, F37, G34, H1, H5, H32, H33, J4, J32, J37, K1, L3, L5, L33, L34, M1, M34, M35, N37, P2, P5, P35, P36, R4, T3, U1, U5, U35, V37, W1, W4, W33, W36, Y34, AA3, AA5, AC3, AC32, AC35, AD1, AD37, AE4, AE34, AE36, AF33, AG4, AG6, AG32, AH35, AJ1, AJ4, AJ32, AJ35, AJ37, AK36, AL3, AL34, AM4, AN6, AN23, AN30, AP8, AP12, AP14, AP16, AP17, AP20, AP25, AR6, AR8, AR9, AR19, AR24, AR31, AR35, AR37, AT4, AT10, AT19, AT20, AT25, AU14, AU22, AU28, AU35	—	—	—
GV <sub>DD</sub>	AD4, AE3, AF1, AF5, AF35, AF37, AG2, AG36, AH33, AH34, AK5, AM1, AM35, AM37, AN2, AN10, AN11, AN12, AN14, AN32, AN36, AP5, AP23, AP28, AR1, AR7, AR10, AR12, AR21, AR25, AR27, AR33, AT15, AT22, AT28, AT33, AU2, AU5, AU16, AU31, AU36	Power for DDR DRAM I/O voltage (2.5 or 1.8 V)	GV <sub>DD</sub>	—
LV <sub>DD</sub> 0	D5, D6	Power for UCC1 Ethernet interface (2.5 V, 3.3 V)	LV <sub>DD</sub> 0	—

### Example 1. Sample Table Use

Index	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
A	1000	0000011	01001	0	33	266	400	300	∞	∞	∞
B	0100	0000100	00110	0	66	266	533	400	∞	∞	∞

- **Example A.** To configure the device with CSB clock rate of 266 MHz, core rate of 400 MHz, and QUICC Engine clock rate 300 MHz while the input clock rate is 33 MHz. Conf No. 's10' and 'c1' are selected from [Table 76](#). SPMF is 1000, CORPLL is 0000011, CEPMPF is 01001, and CEPDF is 0.
- **Example B.** To configure the device with CSBCSB clock rate of 266 MHz, core rate of 533 MHz and QUICC Engine clock rate 400 MHz while the input clock rate is 66 MHz. Conf No. 's5h' and 'c2h' are selected from [Table 76](#). SPMF is 0100, CORPLL is 0000100, CEPMPF is 00110, and CEPDF is 0.

## 22 Thermal

This section describes the thermal specifications of the MPC8360E/58E.

### 22.1 Thermal Characteristics

This table provides the package thermal characteristics for the 37.5 mm × 37.5 mm 740-TBGA package.

**Table 77. Package Thermal Characteristics for the TBGA Package**

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection on single-layer board (1s)	$R_{\theta JA}$	15	°C/W	1, 2
Junction-to-ambient natural convection on four-layer board (2s2p)	$R_{\theta JA}$	11	°C/W	1, 3
Junction-to-ambient (@ 1 m/s) on single-layer board (1s)	$R_{\theta JMA}$	10	°C/W	1, 3
Junction-to-ambient (@ 1 m/s) on four-layer board (2s2p)	$R_{\theta JMA}$	8	°C/W	1, 3
Junction-to-ambient (@ 2 m/s) on single-layer board (1s)	$R_{\theta JMA}$	9	°C/W	1, 3
Junction-to-ambient (@ 2 m/s) on four-layer board (2s2p)	$R_{\theta JMA}$	7	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	4.5	°C/W	4
Junction-to-case thermal	$R_{\theta JC}$	1.1	°C/W	5

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

$T_J$  = junction temperature (°C)

$T_B$  = board temperature at the package perimeter (°C)

$R_{\theta JA}$  = junction to board thermal resistance (°C/W) per JESD51-8

$P_D$  = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

## 22.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter ( $\Psi_{JT}$ ) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$T_J$  = junction temperature (°C)

$T_T$  = thermocouple temperature on top of package (°C)

$\Psi_{JT}$  = junction-to-ambient thermal resistance (°C/W)

$P_D$  = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## 22.2.4 Heat Sinks and Junction-to-Ambient Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

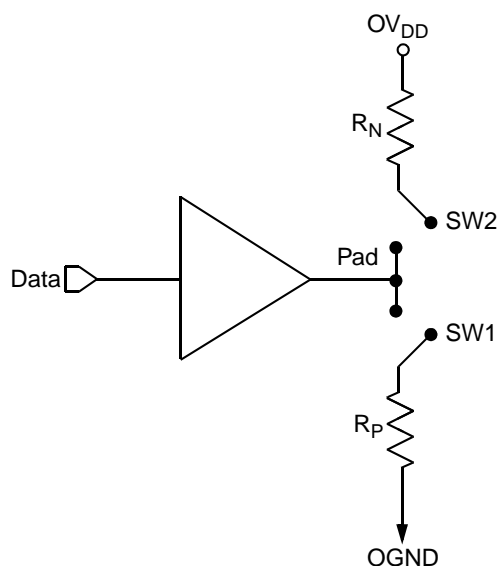
$R_{\theta JA}$  = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$  = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$  = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$  is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance,  $R_{\theta CA}$ . For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.



**Figure 57. Driver Impedance Measurement**

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is  $V_1 = R_{\text{source}} \times I_{\text{source}}$ . Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value  $R_{\text{term}}$ . The measured voltage is  $V_2 = 1/(1/R_1 + 1/R_2) \times I_{\text{source}}$ . Solving for the output impedance gives  $R_{\text{source}} = R_{\text{term}} \times (V_1/V_2 - 1)$ . The drive current is then  $I_{\text{source}} = V_1/R_{\text{source}}$ .

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum  $V_{DD}$ , nominal  $OV_{DD}$ , 105°C.

**Table 79. Impedance Characteristics**

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
$R_N$	42 Target	25 Target	20 Target	$Z_0$	W
$R_P$	42 Target	25 Target	20 Target	$Z_0$	W
Differential	NA	NA	NA	$Z_{\text{DIFF}}$	W

**Note:** Nominal supply voltages. See Table 1,  $T_J = 105^\circ\text{C}$ .

## 23.6 Configuration Pin Muxing

The device provides the user with power-on configuration options that can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While  $\overline{\text{HRESET}}$  is asserted however, these pins are treated as inputs. The value presented on these pins while  $\overline{\text{HRESET}}$  is asserted, is latched when  $\overline{\text{HRESET}}$  deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.