# E·XFL

#### NXP USA Inc. - MPC8358ZUADDEA Datasheet



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#### **Understanding Embedded - Microprocessors**

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8358zuaddea

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



This figure shows the MPC8358E block diagram.



Figure 2. MPC8358E Block Diagram

Major features of the MPC8360E/58E are as follows:

- e300 PowerPC processor core (enhanced version of the MPC603e core)
  - Operates at up to 667 MHz (for the MPC8360E) and 400 MHz (for the MPC8358E)
  - High-performance, superscalar processor core
  - Floating-point, integer, load/store, system register, and branch processing units
  - 32-Kbyte instruction cache, 32-Kbyte data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - Software-compatible with the Freescale processor families implementing the Power Architecture<sup>™</sup> technology
- QUICC Engine unit
  - Two 32-bit RISC controllers for flexible support of the communications peripherals, each operating up to 500 MHz (for the MPC8360E) and 400 MHz (for the MPC8358E)
  - Serial DMA channel for receive and transmit on all serial channels
  - QUICC Engine module peripheral request interface (for SEC, PCI, IEEE Std. 1588<sup>TM</sup>)
  - Eight universal communication controllers (UCCs) on the MPC8360E and six UCCs on the MPC8358E supporting the following protocols and interfaces (not all of them simultaneously):
    - IEEE 1588 protocol supported



- DRAM chip configurations from 64 Mbits to 1 Gigabit with  $\times 8/\times 16$  data ports
- Full ECC support (when the MPC8360E is configured as 2×32-bit DDR memory controllers, both support ECC)
- Page mode support (up to 16 simultaneous open pages for DDR1, up to 32 simultaneous open pages for DDR2)
- Contiguous or discontiguous memory mapping
- Read-modify-write support
- Sleep mode support for self refresh SDRAM
- Supports auto refreshing
- Supports source clock mode
- On-the-fly power management using CKE
- Registered DIMM support
- 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
- External driver impedance calibration
- On-die termination (ODT)
- PCI interface
  - PCI Specification Revision 2.3 compatible
  - Data bus widths:
    - Single 32-bit data PCI interface that operates at up to 66 MHz
  - PCI 3.3-V compatible (not 5-V compatible)
  - PCI host bridge capabilities on both interfaces
  - PCI agent mode supported on PCI interface
  - Support for PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses and support for delayed read transactions
  - Support for posting of processor-to-PCI and PCI-to-memory writes
  - On-chip arbitration, supporting five masters on PCI
  - Support for accesses to all PCI address spaces
  - Parity support
  - Selectable hardware-enforced coherency
  - Address translation units for address mapping between host and peripheral
  - Dual address cycle supported when the device is the target
  - Internal configuration registers accessible from PCI
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 133 MHz
  - Eight chip selects support eight external slaves
  - Up to eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
  - Three protocol engines available on a per chip select basis:
    - General-purpose chip select machine (GPCM)
      - Three user programmable machines (UPMs)
      - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
  - Functional and programming compatibility with the MPC8260 interrupt controller
  - Support for 8 external and 35 internal discrete interrupt sources
  - Support for one external (optional) and seven internal machine checkstop interrupt sources



- Programmable highest priority request
- Four groups of interrupts with programmable priority
- External and internal interrupts directed to communication processor
- Redirects interrupts to external INTA pin when in core disable mode
- Unique vector number for each interrupt source
- Dual industry-standard I<sup>2</sup>C interfaces
  - Two-wire interface
  - Multiple master support
  - Master or slave I<sup>2</sup>C mode support
  - On-chip digital filtering rejects spikes on the bus
  - System initialization data is optionally loaded from I<sup>2</sup>C-1 EPROM by boot sequencer embedded hardware
- DMA controller
  - Four independent virtual channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - All channels accessible by local core and remote PCI masters
  - Misaligned transfer capability
  - Data chaining and direct mode
  - Interrupt on completed segment and chain
  - DMA external handshake signals: DMA\_DREQ[0:3]/DMA\_DACK[0:3]/DMA\_DONE[0:3]. There is one set for each DMA channel. The pins are multiplexed to the parallel IO pins with other QE functions.
- DUART
  - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- System timers
  - Periodic interrupt timer
  - Real-time clock
  - Software watchdog timer
  - Eight general-purpose timers
- IEEE Std. 1149.1<sup>™</sup>-compliant, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

## 2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8360E/58E. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.



Table 1.	Absolute	Maximum	Ratings <sup>1</sup>	(continued)
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Characteristic	Symbol	Max Value	Unit	Notes
Storage temperature range	T <sub>STG</sub>	-55 to 150	°C	_

Notes:

- 1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- 2. Caution: MV<sub>IN</sub> must not exceed GV<sub>DD</sub> by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
- 3. Caution: OV<sub>IN</sub> must not exceed OV<sub>DD</sub> by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
- 4. **Caution:** LV<sub>IN</sub> must not exceed LV<sub>DD</sub> by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
- 5. (M,L,O)V<sub>IN</sub> and MV<sub>REF</sub> may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 3.
- 6. OV<sub>IN</sub> on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 4.

## 2.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for the device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2.	Recommended	Operating	Conditions
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Characteristic	Symbol	Recommended Value	Unit	Notes
Core and PLL supply voltage for	V <sub>DD</sub> & AV <sub>DD</sub>	1.2 V ± 60 mV	V	1, 3
MPC8358 Device Part Number with Processor Frequency label of AD=266MHz and AG=400MHz & QUICC Engine Frequency label of E=300MHz & G=400MHz				
MPC8360 Device Part Number with Processor Frequency label of AG=400MHz and AJ=533MHz & QUICC Engine Frequency label of G=400MHz				
Core and PLL supply voltage for	V <sub>DD</sub> & AV <sub>DD</sub>	1.3 V ± 50 mV	V	1, 3
MPC8360 Device Part Number with Processor Frequency label of AL=667MHz and QUICC Engine Frequency label of H=500MHz				
DDR and DDR2 DRAM I/O supply voltage DDR DDR2	GV <sub>DD</sub>	2.5 V ± 125 mV 1.8 V ± 90 mV	V	_
Three-speed Ethernet I/O supply voltage	LV <sub>DD</sub> 0	3.3 V ± 330 mV 2.5 V ± 125 mV	V	_
Three-speed Ethernet I/O supply voltage	LV <sub>DD</sub> 1	3.3 V ± 330 mV 2.5 V ± 125 mV	V	_
Three-speed Ethernet I/O supply voltage	LV <sub>DD</sub> 2	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—



Power Sequencing

## 2.2.1 Power-Up Sequencing

MPC8360E/58E does not require the core supply voltage ( $V_{DD}$  and  $AV_{DD}$ ) and I/O supply voltages ( $GV_{DD}$ ,  $LV_{DD}$ , and  $OV_{DD}$ ) to be applied in any particular order. During the power ramp up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there may be a period of time that all input and output pins are actively be driven and cause contention and excessive current from 3A to 5A. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage ( $V_{DD}$ ) before the I/O voltage ( $GV_{DD}$ ,  $LV_{DD}$ , and  $OV_{DD}$ ) and assert PORESET before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V, see this figure.



Figure 5. Power Sequencing Example

I/O voltage supplies (GV<sub>DD</sub>, LV<sub>DD</sub>, and OV<sub>DD</sub>) do not have any ordering requirements with respect to one another.

### 2.2.2 Power-Down Sequencing

The MPC8360E/58E does not require the core supply voltage and I/O supply voltages to be powered down in any particular order.

## **3 Power Characteristics**

The estimated typical power dissipation values are shown in these tables.

Table 4. MPC8360E TBGA	<b>Core Power</b>	Dissipation <sup>1</sup>
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Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	500	5.0	5.6	W	2, 3, 5
400	266	400	4.5	5.0	W	2, 3, 4
533	266	400	4.8	5.3	W	2, 3, 4
667	333	400	5.8	6.3	W	3, 6, 7, 8
500	333	500	5.9	6.4	W	3, 6, 7, 8



#### **Power Sequencing**

This table shows the estimated typical I/O power dissipation for the device.

Interface	Parameter	GV <sub>DD</sub> (1.8 V)	GV <sub>DD</sub> (2.5 V)	OV <sub>DD</sub> (3.3 V)	LV <sub>DD</sub> (3.3 V)	LV <sub>DD</sub> (2.5 V)	Unit	Comments
DDR I/O	200 MHz, 1 $\times$ 32 bits	0.3	0.46	_	_	—	W	—
65% utilization $R_c = 20 \Omega$	200 MHz, 1 $\times$ 64 bits	0.4	0.58			—	W	—
$R_t = 50 \Omega$	200 MHz, $2 \times 32$ bits	0.6	0.92	_	_	—	W	_
	266 MHz, 1 $\times$ 32 bits	0.35	0.56	_	_	—	W	_
	266 MHz, 1 $\times$ 64 bits	0.46	0.7	_	_	—	W	_
	266 MHz, $2 \times 32$ bits	0.7	1.11		—	—	W	_
	333 MHz, 1 $\times$ 32 bits	0.4	0.65	_	_	—	W	_
	333 MHz, 1 $\times$ 64 bits	0.53	0.82		—	—	W	_
	333 MHz, $2 \times 32$ bits	0.81	1.3		—	—	W	_
Local Bus I/O	133 MHz, 32 bits	—	—	0.22	_	_	W	_
3 pairs of clocks	83 MHz, 32 bits	—	—	0.14	—	—	W	—
	66 MHz, 32 bits	—	—	0.12	—	—	W	_
	50 MHz, 32 bits	—	—	0.09	—	—	W	_
PCI I/O	33 MHz, 32 bits	—	—	0.05	—	—	W	_
Load = 30 pF	66 MHz, 32 bits	—	—	0.07	—	—	W	—
10/100/1000	MII or RMII	—	—	_	0.01	—	W	Multiply by
Load = 20 pF	GMII or TBI	—	—	_	0.04	—	W	interfaces used.
	RGMII or RTBI	—	—	—	—	0.04	W	
Other I/O	_	—	_	0.1	—	—	W	_

Table 6. Estimated Typical I/O Power Dissipation

## 4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8360E/58E.

### NOTE

The rise/fall time on QUICC Engine block input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of  $V_{DD}$ ; fall time refers to transitions from 90% to 10% of  $V_{DD}$ .



#### **RESET DC Electrical Characteristics**

#### Table 9. GTX\_CLK125 AC Timing Specifications

#### At recommended operating conditions with $LV_{DD}$ = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV (continued)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
GTX_CLK rise and fall time $\label{eq:VDD} \begin{array}{l} \text{LV}_{\text{DD}} = 2.5 \text{ V} \\ \text{LV}_{\text{DD}} = 3.3 \text{ V} \end{array}$	t <sub>G125R</sub> /t <sub>G125F</sub>	—	_	0.75 1.0	ns	1
GTX_CLK125 duty cycle GMII & TBI 1000Base-T for RGMII & RTBI	t <sub>G125H</sub> /t <sub>G125</sub>	45 47	—	55 53	%	2
GTX_CLK125 jitter	—	—	—	±150	ps	2

#### Notes:

- 1. Rise and fall times for GTX\_CLK125 are measured from 0.5 and 2.0 V for  $LV_{DD}$  = 2.5 V and from 0.6 and 2.7 V for  $LV_{DD}$  = 3.3 V.
- GTX\_CLK125 is used to generate the GTX clock for the UCC Ethernet transmitter with 2% degradation. The GTX\_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by GTX\_CLK. See Section 8.2.2, "MII AC Timing Specifications," Section 8.2.3, "RMII AC Timing Specifications," and Section 8.2.5, "RGMII and RTBI AC Timing Specifications" for the duty cycle for 10Base-T and 100Base-T reference clock.

## 5 **RESET Initialization**

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8360E/58E.

### 5.1 **RESET DC Electrical Characteristics**

This table provides the DC electrical characteristics for the RESET pins of the device.

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V <sub>IH</sub>	_	2.0	OV <sub>DD</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	_	-0.3	0.8	V
Input current	I <sub>IN</sub>	_	_	±10	μA
Output high voltage	V <sub>OH</sub> <sup>2</sup>	I <sub>OH</sub> = -8.0 mA	2.4	—	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0 mA	_	0.5	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA	_	0.4	V

#### Table 10. RESET Pins DC Electrical Characteristics <sup>1</sup>

Notes:

1. This table applies for pins PORESET, HRESET, SRESET, and QUIESCE.

2. HRESET and SRESET are open drain pins, thus  $V_{OH}$  is not relevant for those pins.



**QUICC Engine Block Operating Frequency Limitations** 

## 5.3 QUICC Engine Block Operating Frequency Limitations

This section specify the limits of the AC electrical characteristics for the operation of the QUICC Engine block's communication interfaces.

### NOTE

The settings listed below are required for correct hardware interface operation. Each protocol by itself requires a minimal QUICC Engine block operating frequency setting for meeting the performance target. Because the performance is a complex function of all the QUICC Engine block settings, the user should make use of the QUICC Engine block performance utility tool provided by Freescale to validate their system.

This table lists the maximal QUICC Engine block I/O frequencies and the minimal QUICC Engine block core frequency for each interface.

Interface	Interface Operating Frequency (MHz)	Max Interface Bit Rate (Mbps)	Min QUICC Engine Operating Frequency <sup>1</sup> (MHz)	Notes
Ethernet Management: MDC/MDIO	10 (max)	10	20	_
MII	25 (typ)	100	50	_
RMII	50 (typ)	100	50	_
GMII/RGMII/TBI/RTBI	125 (typ)	1000	250	_
SPI (master/slave)	10 (max)	10	20	_
UCC through TDM	50 (max)	70	8  imes F	2
MCC	25 (max)	16.67	16 × F	2, 4
UTOPIA L2	50 (max)	800	$2 \times F$	2
POS-PHY L2	50 (max)	800	$2 \times F$	2
HDLC bus	10 (max)	10	20	_
HDLC/transparent	50 (max)	50	8/3 × F	2, 3
UART/async HDLC	3.68 (max internal ref clock)	115 (Kbps)	20	—
BISYNC	2 (max)	2	20	
USB	48 (ref clock)	12	96	_

#### Table 13. QUICC Engine Block Operating Frequency Limitations

Notes:

1. The QUICC Engine module needs to run at a frequency higher than or equal to what is listed in this table.

2. 'F' is the actual interface operating frequency.\

3. The bit rate limit is independent of the data bus width (that is, the same for serial, nibble, or octal interfaces).

4. TDM in high-speed mode for serial data interface.

## 6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR and DDR2 SDRAM interface of the MPC8360E/58E.



### 8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

### 8.2.2.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

#### Table 29. MII Transmit AC Timing Specifications

At recommended operating conditions with  $LV_{DD}/OV_{DD}$  of 3.3 V ± 10%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit
TX_CLK clock period 10 Mbps	t <sub>MTX</sub>		400		ns
TX_CLK clock period 100 Mbps	t <sub>MTX</sub>	_	40	_	ns
TX_CLK duty cycle	t <sub>MTXH</sub> /t <sub>MTX</sub>	35	_	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t <sub>MTKHDX</sub> t <sub>MTKHDV</sub>	1	5	 15	ns
TX_CLK data clock rise time, (20% to 80%)	t <sub>MTXR</sub>	1.0	_	4.0	ns
TX_CLK data clock fall time, (80% to 20%)	t <sub>MTXF</sub>	1.0		4.0	ns

#### Note:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t<sub>MTKHDX</sub> symbolizes MII transmit timing (MT) for the time t<sub>MTX</sub> clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t<sub>MTX</sub> represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub></sub>

This figure shows the MII transmit AC timing diagram.



Figure 12. MII Transmit AC Timing Diagram



### 8.3.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

#### **Table 37. MII Management AC Timing Specifications**

At recommended operating conditions with  $LV_{DD}$  is 3.3 V ± 10%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Мах	Unit	Notes
MDC frequency	f <sub>MDC</sub>	—	2.5	—	MHz	2
MDC period	t <sub>MDC</sub>	—	400	—	ns	—
MDC clock pulse width high	t <sub>MDCH</sub>	32	—	—	ns	_
MDC to MDIO delay	<sup>t</sup> мрткнрх <sup>t</sup> мрткнрv	10 —	_	 110	ns	3
MDIO to MDC setup time	t <sub>MDRDVKH</sub>	10	—	—	ns	—
MDIO to MDC hold time	t <sub>MDRDXKH</sub>	0	—	—	ns	—
MDC rise time	t <sub>MDCR</sub>	—	—	10	ns	—
MDC fall time	t <sub>MDHF</sub>	_	_	10	ns	

#### Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)</sub>(reference)(state)(signal)(state) for outputs. For example, t<sub>MDKHDX</sub> symbolizes management data timing (MD) for the time t<sub>MDC</sub> from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t<sub>MDRDVKH</sub> symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t<sub>MDC</sub> clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
  </sub>
- This parameter is dependent on the csb\_clk speed (that is, for a csb\_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb\_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
- 3. This parameter is dependent on the ce\_clk speed (that is, for a ce\_clk of 200 MHz, the delay is 90 ns and for a ce\_clk of 300 MHz, the delay is 63 ns).

This figure shows the MII management AC timing diagram.



Figure 21. MII Management Interface Timing Diagram





Figure 27. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (DLL Bypass Mode)



## **10.2 JTAG AC Electrical Characteristics**

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device.

This table provides the JTAG AC timing specifications as defined in Figure 30 through Figure 33.

#### Table 43. JTAG AC Timing Specifications (Independent of CLKIN)<sup>1</sup>

At recommended operating conditions (see Table 2).

Parameter	Symbol <sup>2</sup>	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f <sub>JTG</sub>	0	33.3	MHz	—
JTAG external clock cycle time	t <sub>JTG</sub>	30	_	ns	_
JTAG external clock duty cycle	t <sub>JTKHKL</sub> /t <sub>JTG</sub>	45	55	%	—
JTAG external clock rise and fall times	t <sub>JTGR</sub> & t <sub>JTGF</sub>	0	2	ns	_
TRST assert time	t <sub>TRST</sub>	25	_	ns	3
Input setup times: Boundary-scan data TMS, TDI	t <sub>JTDVKH</sub> t <sub>JTIVKH</sub>	4 4		ns	4
Input hold times: Boundary-scan data TMS, TDI	t <sub>JTDXKH</sub> t <sub>JTIXKH</sub>	10 10		ns	4
Valid times: Boundary-scan data TDO	t <sub>JTKLDV</sub> t <sub>JTKLOV</sub>	2 2	11 11	ns	5
Output hold times: Boundary-scan data TDO	t <sub>jtkldx</sub> t <sub>jtklox</sub>	2 2		ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	t <sub>JTKLDZ</sub> t <sub>JTKLOZ</sub>	2 2	19 9	ns	5, 6

#### Notes:

- 2. The symbols used for timing specifications herein follow the pattern of t<sub>(first two letters of functional block)(signal)(state)</sub> (reference)(state) for inputs and t<sub>(first two letters of functional block)</sub>(reference)(state)(signal)(state) for outputs. For example, t<sub>JTDVKH</sub> symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t<sub>JTG</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>JTDXKH</sub> symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t<sub>JTG</sub> clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
- 4. Non-JTAG signal input timing with respect to t<sub>TCLK</sub>.
- 5. Non-JTAG signal output timing with respect to t<sub>TCLK</sub>.
- 6. Guaranteed by design and characterization.

All outputs are measured from the midpoint voltage of the falling/rising edge of t<sub>TCLK</sub> to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 22). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.



This figure provides the test access port timing diagram.



VM = Midpoint Voltage (OV<sub>DD</sub>/2)

Figure 33. Test Access Port Timing Diagram

## 11 I<sup>2</sup>C

This section describes the DC and AC electrical characteristics for the  $I^2C$  interface of the MPC8360E/58E.

## 11.1 I<sup>2</sup>C DC Electrical Characteristics

This table provides the DC electrical characteristics for the  $I^2C$  interface of the device.

#### Table 44. I<sup>2</sup>C DC Electrical Characteristics

At recommended operating conditions with  $OV_{DD}$  of 3.3 V ± 10%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V <sub>IH</sub>	$0.7  imes OV_{DD}$	OV <sub>DD</sub> + 0.3	V	—
Input low voltage level	V <sub>IL</sub>	-0.3	$0.3  imes OV_{DD}$	V	—
Low level output voltage	V <sub>OL</sub>	0	0.4	V	1
Output fall time from $V_{IH}(\text{min})$ to $V_{IL}(\text{max})$ with a bus capacitance from 10 to 400 pF	<sup>t</sup> I2KLKV	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t <sub>I2KHKL</sub>	0	50	ns	3
Capacitance for each I/O pin	CI	_	10	pF	—
Input current (0 V ≤V <sub>IN</sub> ≤OV <sub>DD</sub> )	I <sub>IN</sub>		±10	μA	4

#### Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.

- 2.  $C_B$  = capacitance of one bus line in pF.
- 3. Refer to the MPC8360E Integrated Communications Processor Reference Manual for information on the digital filter used.
- 4. I/O pins obstruct the SDA and SCL lines if OV<sub>DD</sub> is switched off.



#### **SPI AC Timing Specifications**

Table 56.	SPI AC	Timing	Specifications <sup>1</sup>
-----------	--------	--------	-----------------------------

Characteristic	Symbol <sup>2</sup>	Min	Мах	Unit
SPI inputs—Slave mode (external clock) input hold time	t <sub>NEIXKH</sub>	2	—	ns

Notes:

- 1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state)</sub> for inputs and t<sub>(first two letters of functional block)</sub>(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>NIKHOV</sub> symbolizes the NMSI outputs internal timing (NI) for the time t<sub>SPI</sub> memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

This figure provides the AC test load for the SPI.



Figure 41. SPI AC Test Load

These figures represent the AC timing from Table 56. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

#### Figure 42. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in Master mode (internal clock).







Mechanical Dimensions of the TBGA Package

## 20.2 Mechanical Dimensions of the TBGA Package

This figure depicts the mechanical dimensions and bottom surface nomenclature of the device, 740-TBGA package.



Figure 53. Mechanical Dimensions and Bottom Surface Nomenclature of the TBGA Package



#### Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_DEVSEL/CE_PF[16]	E26	I/O	OV <sub>DD</sub>	5
PCI_IDSEL/CE_PF[17]	F22	I/O	OV <sub>DD</sub>	
PCI_SERR/CE_PF[18]	B29	I/O	OV <sub>DD</sub>	5
PCI_PERR/CE_PF[19]	A29	I/O	OV <sub>DD</sub>	5
PCI_REQ[0]/CE_PF[20]	F19	I/O	LV <sub>DD</sub> 2	—
PCI_REQ[1]/CPCI_HS_ES/ CE_PF[21]	A21	I/O	LV <sub>DD</sub> 2	—
PCI_REQ[2]/CE_PF[22]	C21	I/O	LV <sub>DD</sub> 2	
PCI_GNT[0]/CE_PF[23]	E20	I/O	LV <sub>DD</sub> 2	
PCI_GNT[1]/CPCI1_HS_LED/ CE_PF[24]	B20	I/O	LV <sub>DD</sub> 2	
PCI_GNT[2]/CPCI1_HS_ENUM/ CE_PF[25]	C20	I/O	LV <sub>DD</sub> 2	
PCI_MODE	D36	I	OV <sub>DD</sub>	
M66EN/CE_PF[4]	B37	I/O	OV <sub>DD</sub>	—
	Local Bus Controller Interface			
LAD[0:31]	N32, N33, N35, N36, P37, P32, P34, R36, R35, R34, R33, T37, T35, T34, T33, U37, T32, U36, U34, V36, V35, W37, W35, V33, V32, W34, Y36, W32, AA37, Y33, AA35, AA34	I/O	OV <sub>DD</sub>	_
LDP[0]/CKSTOP_OUT	AB37	I/O	OV <sub>DD</sub>	
LDP[1]/CKSTOP_IN	AB36	I/O	OV <sub>DD</sub>	
LDP[2]/LCS[6]	AB35	I/O	OV <sub>DD</sub>	
LDP[3]/LCS[7]	AA33	I/O	OV <sub>DD</sub>	
LA[27:31]	AC37, AA32, AC36, AC34, AD36	0	OV <sub>DD</sub>	
LCS[0:5]	AD33, AG37, AF34, AE33, AD32, AH37	0	$OV_{DD}$	
LWE[0:3]/LSDDQM[0:3]/LBS[0:3]	AG35, AG34, AH36, AE32	0	$OV_{DD}$	
LBCTL	AD35	0	$OV_{DD}$	
LALE	M37	0	$OV_{DD}$	
LGPL0/LSDA10/cfg_reset_source0	AB32	I/O	$OV_{DD}$	
LGPL1/LSDWE/cfg_reset_source1	AE37	I/O	$OV_{DD}$	
LGPL2/LSDRAS/LOE	AC33	0	$OV_{DD}$	
LGPL3/LSDCAS/cfg_reset_source2	AD34	I/O	$OV_{DD}$	
LGPL4/LGTA/LUPWAIT/LPBSE	AE35	I/O	$OV_{DD}$	
LGPL5/cfg_clkin_div	AF36	I/O	$OV_{DD}$	
LCKE	G36	0	OV <sub>DD</sub>	_
LCLK[0]	J33	0	OV <sub>DD</sub>	—
LCLK[1]/LCS[6]	J34	0	OV <sub>DD</sub>	—



**Pinout Listings** 

## 21 Clocking

This figure shows the internal distribution of clocks within the MPC8360E.



Figure 54. MPC8360E Clock Subsystem



#### Table 77. Package Thermal Characteristics for the TBGA Package (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-package natural convection on top	ΨJT	1	° C/W	6

Notes

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
- 2. Per JEDEC JESD51-2 and SEMI G38-87 with the single layer board horizontal.
- 3. Per JEDEC JESD51-6 with the board horizontal. 1 m/sec is approximately equal to 200 linear feet per minute (LFM).
- 4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

## 22.2 Thermal Management Information

For the following sections,  $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$  where  $P_{I/O}$  is the power dissipation of the I/O drivers. See Table 6 for typical power dissipations values.

# 22.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T<sub>J</sub>, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

 $T_J$  = junction temperature (° C)

 $T_A$  = ambient temperature for the package (° C)

 $R_{\theta IA}$  = junction-to-ambient thermal resistance (° C/W)

 $P_D$  = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity  $T_J - T_A$ ) are possible.

### 22.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. Additionally, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device. At a known board temperature, the junction temperature is estimated using the following equation:

**Heat Sink Attachment** 



Millennium Electronic Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-mil	s (MEI) I Ilennium.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105- Internet: www.chipcoo	3668 lers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefie	ld.com	603-635-5102
Interface material vendors include Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-40 Internet: www.chomer	the following: 014 ics.com	781-935-4850
Dow-Corning Corpora Dow-Corning Electron 2200 W. Salzburg Rd. Midland, MI 48686-09 Internet: www.dowcord	tion ic Materials 197 ning.com	800-248-2481
Shin-Etsu MicroSi, Inc 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.	c. .com	888-642-7674
The Bergquist Compar 18930 West 78th St. Chanhassen, MN 5531 Internet: www.bergqui	ny 7 stcompany.com	800-347-4572

## 22.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb force (4.5 kg force). If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

Part Numbers Fully Addressed by this Document

Device	Package	SVR (Rev. 2.0)	SVR (Rev. 2.1)
MPC8358E	TBGA	0x804A_0020	0x804A_0021
MPC8358	TBGA	0x804B_0020	0x804B_0021

## 25 Document Revision History

This table provides a revision history for this document.

#### Table 82. Revision History

Rev. Number	Date	Substantive Change(s)
5	09/2011	<ul> <li>Section 2.2.1, "Power-Up Sequencing", added the current limitation "3A to 5A" for the excessive current.</li> <li>Section 2.1.2, "Power Supply Voltage Specification, Updated the Characteristic for TBGA (MPC8358 &amp; MPC8360 Device) with specific frequency for Core and PLL voltages.</li> <li>Added table footnote 3 to Table 2.</li> <li>Applied table footnotes 1 and 2 to Table 10.</li> <li>Removed table footnotes from Table 19.</li> <li>Applied table footnotes 8 and 9 to Table 40.</li> <li>Applied table footnotes 2 and 3 to Table 41.</li> <li>Applied table footnotes from Table 46.</li> <li>Applied table footnote to last three rows of Table 65.</li> </ul>
4	01/2011	<ul> <li>Updated references to the LCRR register throughout</li> <li>Removed references to DDR DLL mode in Section 6.2.2, "DDR and DDR2 SDRAM Output AC Timing Specifications."</li> <li>Changed "Junction-to-Case" to "Junction-to-Ambient" in Section 22.2.4, "Heat Sinks and Junction-to-Ambient Thermal Resistance," and Table 78, "Heat Sinks and Junction-to-Ambient Thermal Resistance of TBGA Package," titles.</li> </ul>