# E·XFL

## NXP USA Inc. - MPC8360CVVADDH Datasheet



#### Welcome to E-XFL.COM

#### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8360cvvaddh

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



- 10/100 Mbps Ethernet/IEEE Std. 802.3<sup>TM</sup> CDMA/CS interface through a media-independent interface (MII, RMII, RGMII)<sup>1</sup>
- 1000 Mbps Ethernet/IEEE 802.3 CDMA/CS interface through a media-independent interface (GMII, RGMII, TBI, RTBI) on UCC1 and UCC2
- 9.6-Kbyte jumbo frames
- ATM full-duplex SAR, up to 622 Mbps (OC-12/STM-4), AAL0, AAL1, and AAL5 in accordance ITU-T I.363.5
- ATM AAL2 CPS, SSSAR, and SSTED up to 155 Mbps (OC-3/STM-1) Mbps full duplex (with 4 CPS packets per cell) in accordance ITU-T I.366.1 and I.363.2
- ATM traffic shaping for CBR, VBR, UBR, and GFR traffic types compatible with ATM forum TM4.1 for up to 64-Kbyte simultaneous ATM channels
- ATM AAL1 structured and unstructured circuit emulation service (CES 2.0) in accordance with ITU-T I.163.1 and ATM Forum af-vtoa-00-0078.000
- IMA (Inverse Multiplexing over ATM) for up to 31 IMA links over 8 IMA groups in accordance with the ATM forum AF-PHY-0086.000 (Version 1.0) and AF-PHY-0086.001 (Version 1.1)
- ATM Transmission Convergence layer support in accordance with ITU-T I.432
- ATM OAM handling features compatible with ITU-T I.610
- PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686, and 3153
- IP support for IPv4 packets including TOS, TTL, and header checksum processing
- Ethernet over first mile IEEE 802.3ah
- Shim header
- Ethernet-to-Ethernet/AAL5/AAL2 inter-working
- L2 Ethernet switching using MAC address or IEEE Std. 802.1P/Q<sup>™</sup> VLAN tags
- ATM (AAL2/AAL5) to Ethernet (IP) interworking in accordance with RFC2684 including bridging of ATM ports to Ethernet ports
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- AAL2 protocol rate up to 4 CPS at OC-3/STM-1 rate
- Packet over Sonet (POS) up to 622-Mbps full-duplex 124 MultiPHY
- POS hardware; microcode must be loaded as an IRAM package
- Transparent up to 70-Mbps full-duplex
- HDLC up to 70-Mbps full-duplex
- HDLC BUS up to 10 Mbps
- Asynchronous HDLC
- UART
- BISYNC up to 2 Mbps
- User-programmable Virtual FIFO size
- QUICC multichannel controller (QMC) for 64 TDM channels
- One multichannel communication controller (MCC) only on the MPC8360E supporting the following:
  - 256 HDLC or transparent channels
  - 128 SS7 channels
  - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces
- Two UTOPIA/POS interfaces on the MPC8360E supporting 124 MultiPHY each (optional 2\*128 MultiPHY with extended address) and one UTOPIA/POS interface on the MPC8358E supporting 31/124 MultiPHY
- Two serial peripheral interfaces (SPI); SPI2 is dedicated to Ethernet PHY management

1.SMII or SGMII media-independent interface is not currently supported.



#### **Power Sequencing**

This figure shows the undershoot and overshoot voltage of the PCI interface of the device for the 3.3-V signals, respectively.



Figure 4. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

## 2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	OV <sub>DD</sub> = 3.3 V
PCI signals	25	
PCI output clocks (including PCI_SYNC_OUT)	42	
DDR signal	20 36 (half-strength mode) <sup>1</sup>	GV <sub>DD</sub> = 2.5 V
DDR2 signal	18 36 (half-strength mode) <sup>1</sup>	GV <sub>DD</sub> = 1.8 V
10/100/1000 Ethernet signals	42	LV <sub>DD</sub> = 2.5/3.3 V
DUART, system control, I <sup>2</sup> C, SPI, JTAG	42	OV <sub>DD</sub> = 3.3 V
GPIO signals	42	OV <sub>DD</sub> = 3.3 V LV <sub>DD</sub> = 2.5/3.3 V

Note:

1. DDR output impedance values for half strength mode are verified by design and not tested.

# 2.2 Power Sequencing

This section details the power sequencing considerations for the MPC8360E/58E.





Table 4. MPC8360E TBGA Core Power Dissipation <sup>1</sup>	(continued)
--	-------------

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
667	333	500	6.1	6.8	W	2, 3, 5, 9

#### Notes:

- 1. The values do not include I/O supply power (OV<sub>DD</sub>, LV<sub>DD</sub>, GV<sub>DD</sub>) or AV<sub>DD</sub>. For I/O power values, see Table 6.
- 2. Typical power is based on a voltage of V<sub>DD</sub> = 1.2 V or 1.3 V, a junction temperature of T<sub>J</sub> = 105°C, and a Dhrystone benchmark application.
- 3. Thermal solutions need to design to a value higher than typical power on the end application, T<sub>A</sub> target, and I/O power.
- 4. Maximum power is based on a voltage of V<sub>DD</sub> = 1.2 V, WC process, a junction T<sub>J</sub> = 105°C, and an artificial smoke test.
- Maximum power is based on a voltage of V<sub>DD</sub> = 1.3 V for applications that use 667 MHz (CPU)/500 (QE) with WC process, a junction T<sub>1</sub> = 105° C, and an artificial smoke test.
- 6. Typical power is based on a voltage of  $V_{DD}$  = 1.3 V, a junction temperature of  $T_J$  = 70° C, and a Dhrystone benchmark application.
- Maximum power is based on a voltage of V<sub>DD</sub> = 1.3 V for applications that use 667 MHz (CPU) or 500 (QE) with WC process, a junction T<sub>J</sub> = 70° C, and an artificial smoke test.
- 8. This frequency combination is only available for rev. 2.0 silicon.
- 9. This frequency combination is not available for rev. 2.0 silicon.

## Table 5. MPC8358E TBGA Core Power Dissipation<sup>1</sup>

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	300	4.1	4.5	W	2, 3, 4
400	266	400	4.5	5.0	W	2, 3, 4

#### Notes:

- 1. The values do not include I/O supply power (OV<sub>DD</sub>,  $LV_{DD}$ ,  $GV_{DD}$ ) or  $AV_{DD}$ . For I/O power values, see Table 6.
- Typical power is based on a voltage of V<sub>DD</sub> = 1.2 V, a junction temperature of T<sub>J</sub> = 105°C, and a Dhrystone benchmark application.
- 3. Thermal solutions need to design to a value higher than typical power on the end application, T<sub>A</sub> target, and I/O power.
- 4. Maximum power is based on a voltage of V<sub>DD</sub> = 1.2 V, WC process, a junction T<sub>J</sub> = 105°C, and an artificial smoke test.



#### **Power Sequencing**

This table shows the estimated typical I/O power dissipation for the device.

Interface	Parameter	GV <sub>DD</sub> (1.8 V)	GV <sub>DD</sub> (2.5 V)	OV <sub>DD</sub> (3.3 V)	LV <sub>DD</sub> (3.3 V)	LV <sub>DD</sub> (2.5 V)	Unit	Comments
DDR I/O	200 MHz, 1 $\times$ 32 bits	0.3	0.46	_	_	—	W	—
$R_s = 20 \Omega$	200 MHz, 1 $\times$ 64 bits	0.4	0.58		_	—	W	—
$R_t = 50 \Omega$	200 MHz, $2 \times 32$ bits	0.6	0.92	_	_	—	W	_
	266 MHz, 1 $\times$ 32 bits	0.35	0.56	_	_	—	W	_
	266 MHz, 1 $\times$ 64 bits	0.46	0.7	_	_	—	W	_
	266 MHz, $2 \times 32$ bits	0.7	1.11		—	—	W	_
	333 MHz, 1 $\times$ 32 bits	0.4	0.65	_	_	—	W	_
	333 MHz, 1 $\times$ 64 bits	0.53	0.82		—	—	W	_
	333 MHz, $2 \times 32$ bits	0.81	1.3		—	—	W	_
Local Bus I/O	133 MHz, 32 bits	—	—	0.22	_	_	W	_
3 pairs of clocks	83 MHz, 32 bits	—	—	0.14	—	—	W	—
	66 MHz, 32 bits	—	—	0.12	—	—	W	_
	50 MHz, 32 bits	—	—	0.09	—	—	W	_
PCI I/O	33 MHz, 32 bits	—	—	0.05	—	—	W	_
Load = 30 pF	66 MHz, 32 bits	—	—	0.07	—	—	W	—
10/100/1000	MII or RMII	—	—	_	0.01	—	W	Multiply by
Load = 20 pF	GMII or TBI	—	—	_	0.04	—	W	interfaces used.
	RGMII or RTBI	—	—	—	—	0.04	W	
Other I/O	_	—	_	0.1	—	—	W	_

Table 6. Estimated Typical I/O Power Dissipation

# 4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8360E/58E.

## NOTE

The rise/fall time on QUICC Engine block input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of  $V_{DD}$ ; fall time refers to transitions from 90% to 10% of  $V_{DD}$ .



**QUICC Engine Block Operating Frequency Limitations** 

# 5.3 QUICC Engine Block Operating Frequency Limitations

This section specify the limits of the AC electrical characteristics for the operation of the QUICC Engine block's communication interfaces.

## NOTE

The settings listed below are required for correct hardware interface operation. Each protocol by itself requires a minimal QUICC Engine block operating frequency setting for meeting the performance target. Because the performance is a complex function of all the QUICC Engine block settings, the user should make use of the QUICC Engine block performance utility tool provided by Freescale to validate their system.

This table lists the maximal QUICC Engine block I/O frequencies and the minimal QUICC Engine block core frequency for each interface.

Interface	Interface Operating Frequency (MHz)	Max Interface Bit Rate (Mbps)	Min QUICC Engine Operating Frequency <sup>1</sup> (MHz)	Notes
Ethernet Management: MDC/MDIO	10 (max)	10	20	_
MII	25 (typ)	100	50	_
RMII	50 (typ)	100	50	_
GMII/RGMII/TBI/RTBI	125 (typ)	1000	250	_
SPI (master/slave)	10 (max)	10	20	_
UCC through TDM	50 (max)	70	8  imes F	2
MCC	25 (max)	16.67	16 × F	2, 4
UTOPIA L2	50 (max)	800	$2 \times F$	2
POS-PHY L2	50 (max)	800	$2 \times F$	2
HDLC bus	10 (max)	10	20	_
HDLC/transparent	50 (max)	50	8/3 × F	2, 3
UART/async HDLC	3.68 (max internal ref clock)	115 (Kbps)	20	_
BISYNC	2 (max)	2	20	
USB	48 (ref clock)	12	96	_

## Table 13. QUICC Engine Block Operating Frequency Limitations

Notes:

1. The QUICC Engine module needs to run at a frequency higher than or equal to what is listed in this table.

2. 'F' is the actual interface operating frequency.\

3. The bit rate limit is independent of the data bus width (that is, the same for serial, nibble, or octal interfaces).

4. TDM in high-speed mode for serial data interface.

# 6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR and DDR2 SDRAM interface of the MPC8360E/58E.



#### **DDR and DDR2 SDRAM AC Electrical Characteristics**

This table provides the input AC timing specifications for the DDR SDRAM interface when  $GV_{DD}(typ) = 2.5 \text{ V}$ .

#### Table 19. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with  $GV_{DD}$  of 2.5 V ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V <sub>IL</sub>	—	MV <sub>REF</sub> – 0.31	V	—
AC input high voltage	V <sub>IH</sub>	MV <sub>REF</sub> + 0.31	_	V	_

### Table 20. DDR and DDR2 SDRAM Input AC Timing Specifications Mode

At recommended operating conditions with  $GV_{DD}$  of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
MDQS—MDQ/MECC input skew per byte 333 MHz 266 MHz 200 MHz	t <sub>DISKEW</sub>	-750 -1125 -1250	750 1125 1250	ps	1, 2

#### Notes:

1. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.

Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 ≤n ≤7) or ECC (MECC[{0...7}] if n = 8).

This figure shows the input timing diagram for the DDR controller.



Figure 6. DDR Input Timing Diagram



# Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with  $GV_{DD}$  of (1.8 V or 2.5 V) ± 5%.

Parameter <sup>8</sup>	Symbol <sup>1</sup>	Min	Мах	Unit	Notes
MDQS epilogue end	t <sub>DDKHME</sub>	-0.6	0.9	ns	7

#### Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)</sub>(reference)(state)(signal)(state) for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t<sub>DDKHAS</sub> symbolizes DDR timing (DD) for the time t<sub>MCK</sub> memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t<sub>DDKLDX</sub> symbolizes DDR timing (DD) for the time t<sub>MCK</sub> memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
  </sub>
- 2. All MCK/ $\overline{MCK}$  referenced measurements are made from the crossing of the two signals ±0.1 V.
- In the source synchronous mode, MCK/MCK can be shifted in ¼ applied cycle increments through the clock control register. For the skew measurements referenced for t<sub>AOSKEW</sub> it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
- ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.
- 5. Note that t<sub>DDKHMH</sub> follows the symbol conventions described in note 1. For example, t<sub>DDKHMH</sub> describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t<sub>DDKHMH</sub> can be modified through control of the DQSS override bits in the TIMING\_CFG\_2 register. In source synchronous mode, this is typically set to the same delay as the clock adjust in the CLK\_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. Refer MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the device.
- All outputs are referenced to the rising edge of MCK(n) at the pins of the device. Note that t<sub>DDKHMP</sub> follows the symbol conventions described in note 1.
- 8. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.
- 9. In rev. 2.0 silicon, t<sub>DDKHMH</sub> maximum meets the specification of 0.6 ns. In rev. 2.0 silicon, due to errata, t<sub>DDKHMH</sub> minimum is –0.9 ns. Refer to Errata DDR18 in *Chip Errata for the MPC8360E, Rev. 1*.

This figure shows the DDR SDRAM output timing for address skew with respect to any MCK.







## 8.2.1.1 GMII Transmit AC Timing Specifications

This table provides the GMII transmit AC timing specifications.

### Table 27. GMII Transmit AC Timing Specifications

At recommended operating conditions with  $LV_{DD}/OV_{DD}$  of 3.3 V ± 10%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit	Notes
GTX_CLK clock period	t <sub>GTX</sub>	_	8.0		ns	_
GTX_CLK duty cycle	t <sub>GTXH/tGTX</sub>	40	_	60	%	—
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	<sup>t</sup> GTKHDX <sup>t</sup> GTKHDV	0.5	_	 5.0	ns	3
GTX_CLK clock rise time, (20% to 80%)	t <sub>GTXR</sub>	_	_	1.0	ns	_
GTX_CLK clock fall time, (80% to 20%)	t <sub>GTXF</sub>	_	_	1.0	ns	—
GTX_CLK125 clock period	t <sub>G125</sub>	_	8.0	_	ns	2
GTX_CLK125 reference clock duty cycle measured at $LV_{DD/2}$	t <sub>G125H</sub> /t <sub>G125</sub>	45		55	%	2

Notes:

- 1. The symbols used for timing specifications follow the pattern t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>GTKHDV</sub> symbolizes GMII transmit timing (GT) with respect to the t<sub>GTX</sub> clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t<sub>GTKHDX</sub> symbolizes GMII transmit timing (GT) with respect to the t<sub>ignx</sub> clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t<sub>GTX</sub> represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).</sub>
- 2. This symbol is used to represent the external GTX\_CLK125 signal and does not follow the original symbol naming convention.
- In rev. 2.0 silicon, due to errata, t<sub>GTKHDX</sub> minimum and t<sub>GTKHDV</sub> maximum are not supported when the GTX\_CLK is selected. Refer to Errata QE\_ENET18 in Chip Errata for the MPC8360E, Rev. 1.

This figure shows the GMII transmit AC timing diagram.



Figure 10. GMII Transmit AC Timing Diagram



## 8.2.4.1 TBI Transmit AC Timing Specifications

This table provides the TBI transmit AC timing specifications.

### Table 33. TBI Transmit AC Timing Specifications

At recommended operating conditions with  $LV_{DD}/OV_{DD}$  of 3.3 V ± 10%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit	Notes
GTX_CLK clock period	t <sub>TTX</sub>	_	8.0	_	ns	—
GTX_CLK duty cycle	t <sub>TTXH</sub> /t <sub>TTX</sub>	40	—	60	%	—
GTX_CLK to TBI data TCG[9:0] delay	t <sub>TTKHDX</sub> t <sub>TTKHDV</sub>	1.0	—	 5.0	ns	3
GTX_CLK clock rise time, (20% to 80%)	t <sub>TTXR</sub>	_	—	1.0	ns	—
GTX_CLK clock fall time, (80% to 20%)	t <sub>TTXF</sub>	_	_	1.0	ns	—
GTX_CLK125 reference clock period	t <sub>G125</sub>	_	8.0	_	ns	2
GTX_CLK125 reference clock duty cycle	t <sub>G125H</sub> /t <sub>G125</sub>	45	—	55	ns	—

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)</sub> (reference)(state) for inputs and t<sub>(first two letters of functional block)</sub>(reference)(state)(signal)(state) for outputs. For example, t<sub>TTKHDV</sub> symbolizes the TBI transmit timing (TT) with respect to the time from t<sub>TTX</sub> (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t<sub>TTKHDX</sub> symbolizes the TBI transmit timing (TT) with respect to the time from t<sub>TTX</sub> (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t<sub>TTKHDX</sub> symbolizes the TBI transmit timing (TT) with respect to the time from t<sub>TTX</sub> (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t<sub>TTX</sub> represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 2. This symbol is used to represent the external GTX\_CLK125 and does not follow the original symbol naming convention.
- 3. In rev. 2.0 silicon, due to errata, t<sub>TTKHDX</sub> minimum is 0.7 ns for UCC1. Refer to Errata QE\_ENET19 in Chip Errata for the MPC8360E, Rev. 1.

This figure shows the TBI transmit AC timing diagram.



Figure 18. TBI Transmit AC Timing Diagram



This figure provides the AC test load for the  $I^2C$ .



Figure 34. I<sup>2</sup>C AC Test Load

This figure shows the AC timing diagram for the  $I^2C$  bus.



# 12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8360E/58E.

# 12.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface of the device.

### **Table 46. PCI DC Electrical Characteristics**

Parameter	Symbol	Test Condition	Min	Мах	Unit
High-level input voltage	V <sub>IH</sub>	$V_{OUT} \ge V_{OH}$ (min) or	$0.5\times\text{OV}_\text{DD}$	OV <sub>DD</sub> + 0.5	V
Low-level input voltage	V <sub>IL</sub>	V <sub>OUT</sub> ≤V <sub>OL</sub> (max)	-0.5	$0.3  imes OV_{DD}$	V
High-level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -500 μA	$0.9  imes OV_{DD}$	—	V
Low-level output voltage	V <sub>OL</sub>	l <sub>OL</sub> = 1500 μA	—	$0.1  imes OV_{DD}$	V
Input current	I <sub>IN</sub>	0 V ≤V <sub>IN</sub> <sup>1</sup> ≤OV <sub>DD</sub>	—	±10	μA

# 12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the device. Note that the PCI\_CLK or PCI\_SYNC\_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. This table provides the PCI AC timing specifications at 66 MHz.

Parameter	Symbol <sup>1</sup>	Min	Мах	Unit	Notes
Clock to output valid	t <sub>PCKHOV</sub>	_	6.0	ns	2, 5
Output hold from clock	t <sub>PCKHOX</sub>	1	—	ns	2

## Table 47. PCI AC Timing Specifications at 66 MHz



# 18.3 AC Test Load

These figures represent the AC timing from Table 62 and Table 63. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the timing with external clock.



Figure 50. AC Timing (External Clock) Diagram

This figure shows the timing with internal clock.



Figure 51. AC Timing (Internal Clock) Diagram



**USB DC Electrical Characteristics** 

# 19 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8360E/58E.

# **19.1 USB DC Electrical Characteristics**

This table provides the DC electrical characteristics for the USB interface.

### **Table 64. USB DC Electrical Characteristics**

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V <sub>IH</sub>	2	OV <sub>DD</sub> + 0.3	V
Low-level input voltage	V <sub>IL</sub>	-0.3	0.8	V
High-level output voltage, $I_{OH} = -100 \ \mu A$	V <sub>OH</sub>	OV <sub>DD</sub> - 0.4	—	V
Low-level output voltage, I <sub>OL</sub> = 100 μA	V <sub>OL</sub>	—	0.2	V
Input current	I <sub>IN</sub>	—	±10	μA

# **19.2 USB AC Electrical Specifications**

This table describes the general timing parameters of the USB interface of the device.

Table 65. USB General Timing Parameters

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes	Note
USB clock cycle time	t <sub>USCK</sub>	20.83		ns	Full speed 48 MHz	_
USB clock cycle time	t <sub>USCK</sub>	166.67		ns	Low speed 6 MHz	_
Skew between TXP and TXN	t <sub>USTSPN</sub>	_	5	ns	—	2
Skew among RXP, RXN, and RXD	t <sub>USRSPND</sub>	_	10	ns	Full speed transitions	2
Skew among RXP, RXN, and RXD	t <sub>USRPND</sub>		100	ns	Low speed transitions	2

#### Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(state)(signal)</sub> for receive signals and t<sub>(first two letters of functional block)(state)(signal)</sub> for transmit signals. For example, t<sub>USRSPND</sub> symbolizes USB timing (US) for the USB receive signals skew (RS) among RXP, RXN, and RXD (PND). Also, t<sub>USTSPN</sub> symbolizes USB timing (US) for the USB transmit signals skew (TS) between TXP and TXN (PN).

2. Skew measurements are done at  $OV_{DD}/2$  of the rising or falling edge of the signals.

This figure provide the AC test load for the USB.



Figure 52. USB AC Test Load



**Pinout Listings** 

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC1_MCKE[0:1]	AL32, AU33	0	GV <sub>DD</sub>	3
MEMC1_MCK[0:1]	AK37, AT37	0	GV <sub>DD</sub>	
MEMC1_MCK[2:3]/ MEMC2_MCK[0:1]	AN1, AR2	0	GV <sub>DD</sub>	_
MEMC1_MCK[4:5]/ MEMC2_MCKE[0:1]	AN25, AK1	0	GV <sub>DD</sub>	_
MEMC1_MCK[0:1]	AL37, AT36	0	GV <sub>DD</sub>	_
MEMC1_MCK[2:3]/ MEMC2_MCK[0:1]	AP2, AT2	0	GV <sub>DD</sub>	_
MEMC1_MCK[4]/ MEMC2_MDM[8]	AN24	0	GV <sub>DD</sub>	
MEMC1_MCK[5]/ MEMC2_MDQS[8]	AL1	0	GV <sub>DD</sub>	_
MDIC[0:1]	АН6, АР30	I/O	GV <sub>DD</sub>	10
Sec	ondary DDR SDRAM Memory Controller Interface			
MEMC2_MECC[0:7]	AN16, AP18, AM16, AM17, AN17, AP13, AP15, AN13	I/O	GV <sub>DD</sub>	_
MEMC2_MBA[0:2]	AU12, AU15, AU13	0	GV <sub>DD</sub>	_
MEMC2_MA[0:14]	AT12, AP11, AT13, AT14, AR13, AR15, AR16, AT16, AT18, AT17, AP10, AR20, AR17, AR14, AR11	0	GV <sub>DD</sub>	_
MEMC2_MWE	AU10	0	GV <sub>DD</sub>	_
MEMC2_MRAS	AT11	0	GV <sub>DD</sub>	_
MEMC2_MCAS	AU11	0	GV <sub>DD</sub>	
	PCI			
PCI_INTA/IRQ_OUT/CE_PF[5]	A20	I/O	LV <sub>DD</sub> 2	2
PCI_RESET_OUT/CE_PF[6]	E19	I/O	LV <sub>DD</sub> 2	_
PCI_AD[31:30]/CE_PG[31:30]	D20, D21	I/O	LV <sub>DD</sub> 2	
PCI_AD[29:25]/CE_PG[29:25]	A24, B23, C23, E23, A26	I/O	OV <sub>DD</sub>	
PCI_AD[24]/CE_PG[24]	B21	I/O	LV <sub>DD</sub> 2	_
PCI_AD[23:0]/CE_PG[23:0]	C24, C25, D25, B25, E24, F24, A27, A28, F27, A30, C30, D30, E29, B31, C31, D31, D32, A32, C33, B33, F30, E31, A34, D33	I/O	OV <sub>DD</sub>	
PCI_C/BE[3:0]/CE_PF[10:7]	E22, B26, E28, F28	I/O	OV <sub>DD</sub>	
PCI_PAR/CE_PF[11]	D28	I/O	OV <sub>DD</sub>	
PCI_FRAME/CE_PF[12]	D26	I/O	OV <sub>DD</sub>	5
PCI_TRDY/CE_PF[13]	C27	I/O	OV <sub>DD</sub>	5
PCI_IRDY/CE_PF[14]	C28	I/O	OV <sub>DD</sub>	5
PCI_STOP/CE_PF[15]	B28	I/O	OV <sub>DD</sub>	5



## Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
IRQ[4:5]	G33, G32	I/O	OV <sub>DD</sub>	—
IRQ[6]/LCS[6]/CKSTOP_OUT	E35	I/O	OV <sub>DD</sub>	—
IRQ[7]/LCS[7]/CKSTOP_IN	H36	I/O	OV <sub>DD</sub>	—
	DUART			
UART1_SOUT/M1SRCID[0]/ M2SRCID[0]/LSRCID[0]	E32	0	OV <sub>DD</sub>	_
UART1_SIN/M1SRCID[1]/ M2SRCID[1]/LSRCID[1]	B34	I/O	OV <sub>DD</sub>	
UART1_CTS/M1SRCID[2]/ M2SRCID[2]/LSRCID[2]	C34	I/O	OV <sub>DD</sub>	
UART1_RTS/M1SRCID[3]/ M2SRCID[3]/LSRCID[3]	A35	0	OV <sub>DD</sub>	_
	I <sup>2</sup> C Interface			<u> </u>
IIC1_SDA	D34	I/O	OV <sub>DD</sub>	2
IIC1_SCL	B35	I/O	OV <sub>DD</sub>	2
IIC2_SDA	E33	I/O	OV <sub>DD</sub>	2
IIC2_SCL	C35	I/O	OV <sub>DD</sub>	2
	QUICC Engine			
CE_PA[0]	F8	I/O	LV <sub>DD0</sub>	—
CE_PA[1:2]	AH1, AG5	I/O	OV <sub>DD</sub>	—
CE_PA[3:7]	F6, D4, C3, E5, A3	I/O	LV <sub>DD</sub> 0	—
CE_PA[8]	AG3	I/O	OV <sub>DD</sub>	—
CE_PA[9:12]	F7, B3, E6, B4	I/O	LV <sub>DD</sub> 0	—
CE_PA[13:14]	AG1, AF6	I/O	OV <sub>DD</sub>	—
CE_PA[15]	B2	I/O	LV <sub>DD</sub> 0	—
CE_PA[16]	AF4	I/O	OV <sub>DD</sub>	—
CE_PA[17:21]	B16, A16, E17, A17, B17	I/O	LV <sub>DD</sub> 1	—
CE_PA[22]	AF3	I/O	OV <sub>DD</sub>	—
CE_PA[23:26]	C18, D18, E18, A18	I/O	LV <sub>DD</sub> 1	—
CE_PA[27:28]	AF2, AE6	I/O	OV <sub>DD</sub>	—
CE_PA[29]	B19	I/O	LV <sub>DD</sub> 1	—
CE_PA[30]	AE5	I/O	$OV_{DD}$	—
CE_PA[31]	F16	I/O	LV <sub>DD</sub> 1	—



**Pinout Listings** 

Signal	Package Pin Number	Pin Type	Power Supply	Notes					
CE_PB[0:27]	AE2, AE1, AD5, AD3, AD2, AC6, AC5, AC4, AC2, AC1, AB5, AB4, AB3, AB1, AA6, AA4, AA2, Y6, Y4, Y3, Y2, Y1, W6, W5, W2, V5, V3, V2	I/O	OV <sub>DD</sub>	_					
CE_PC[0:1]	V1, U6	I/O	OV <sub>DD</sub>						
CE_PC[2:3]	C16, A15	I/O	LV <sub>DD</sub> 1	—					
CE_PC[4:6]	U4, U3, T6	I/O	OV <sub>DD</sub>	—					
CE_PC[7]	C19	I/O	LV <sub>DD</sub> 2	—					
CE_PC[8:9]	A4, C5	I/O	LV <sub>DD</sub> 0	—					
CE_PC[10:30]	T5, T4, T2, T1, R5, R3, R1, C11, D12, F13, B10, C10, E12, A9, B8, D10, A14, E15, B14, D15, AH2	I/O	OV <sub>DD</sub>	—					
CE_PD[0:27]	E11, D9, C8, F11, A7, E9, C7, A6, F10, B6, D7, E8, B5, A5, C2, E4, F5, B1, D2, G5, D1, E2, H6, F3, E1, F2, G3, H4	I/O	OV <sub>DD</sub>	—					
CE_PE[0:31]	K3, J2, F1, G2, J5, H3, G1, H2, K6, J3, K5, K4, L6, P6, P4, P3, P1, N4, N5, N2, N1, M2, M3, M5, M6, L1, L2, L4, E14, C13, C14, B13	I/O	OV <sub>DD</sub>	—					
CE_PF[0:3]	F14, D13, A12, A11	I/O	OV <sub>DD</sub>	—					
	Clocks								
PCI_CLK_OUT[0]/CE_PF[26]	B22	I/O	LV <sub>DD</sub> 2	—					
PCI_CLK_OUT[1:2]/CE_PF[27:28]	D22, A23	I/O	OV <sub>DD</sub>	—					
CLKIN	E37	I	OV <sub>DD</sub>	—					
PCI_CLOCK/PCI_SYNC_IN	M36	I	OV <sub>DD</sub>	—					
PCI_SYNC_OUT/CE_PF[29]	D37	I/O	OV <sub>DD</sub>	3					
	JTAG								
ТСК	К33	I	OV <sub>DD</sub>	_					
TDI	K34	I	OV <sub>DD</sub>	4					
TDO	H37	0	OV <sub>DD</sub>	3					
TMS	J36	I	OV <sub>DD</sub>	4					
TRST	L32	I	OV <sub>DD</sub>	4					
	Test								
TEST	L35	I	OV <sub>DD</sub>	7					
TEST_SEL	AU34	I	GV <sub>DD</sub>	10					
	РМС								
QUIESCE	B36	0	OV <sub>DD</sub>	—					
System Control									

## Table 67. MPC8358E TBGA Pinout Listing (continued)



Core PLL Configuration

# 21.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb\_clk*) and the e300 core clock (*core\_clk*). This table shows the encodings for RCWL[COREPLL]. COREPLL values not listed in this table should be considered reserved.

RCWL[COREPLL]		core_clk:csb_clk	VCO divider		
0–1	2–5	6	Ratio		
nn	0000	n	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)	
00	0001	0	1:1	÷2	
01	0001	0	1:1	÷4	
10	0001	0	1:1	÷8	
11	0001	0	1:1	÷8	
00	0001	1	1.5:1	÷2	
01	0001	1	1.5:1	÷4	
10	0001	1	1.5:1	÷8	
11	0001	1	1.5:1	÷8	
00	0010	0	2:1	÷2	
01	0010	0	2:1	÷4	
10	0010	0	2:1	÷8	
11	0010	0	2:1	÷8	
00	0010	1	2.5:1	÷2	
01	0010	1	2.5:1	÷4	
10	0010	1	2.5:1	÷8	
11	0010	1	2.5:1	÷8	
00	0011	0	3:1	÷2	
01	0011	0	3:1	÷4	
10	0011	0	3:1	÷8	
11	0011	0	3:1	÷8	

## Table 73. e300 Core PLL Configuration

## NOTE

Core VCO frequency = Core frequency  $\times$  VCO divider. The VCO divider (RCWL[COREPLL[0:1]]) must be set properly so that the core VCO frequency is in the range of 800–1800 MHz. Having a core frequency below the CSB frequency is not a possible option because the core frequency must be equal to or greater than the CSB frequency.



The QUICC Engine block VCO frequency is derived from the following equations:

 $ce_clk = (primary clock input \times CEPMF) \div (1 + CEPDF)$ 

QE VCO Frequency =  $ce_clk \times VCO$  divider  $\times (1 + CEPDF)$ 

# 21.4 Suggested PLL Configurations

To simplify the PLL configurations, the device might be separated into two clock domains. The first domain contains the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb\_clk as its input clock. The second clock domain has the QUICC Engine block PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. This table shows suggested PLL configurations for 33 and 66 MHz input clocks and illustrates each of the clock domains separately. Any combination of clock domains setting with same input clock are valid. Refer to Section 21, "Clocking," for the appropriate operating frequencies for your device.

Conf No. <sup>1</sup>	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock Freq (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)		
	33 MHz CLKIN/PCI_SYNC_IN Options												
s1	0100	0000100	æ	æ	33	133	266	—	8	8	8		
s2	0100	0000101	æ	æ	33	133	333	_	8	8	8		
s3	0101	0000100	æ	æ	33	166	333	_	8	8	8		
s4	0101	0000101	æ	æ	33	166	416			8	8		
s5	0110	0000100	æ	æ	33	200	400		8	8	8		
s6	0110	0000110	æ	æ	33	200	600			—	8		
s7	0111	0000011	æ	æ	33	233	350		8	8	8		
s8	0111	0000100	æ	æ	33	233	466			8	8		
s9	0111	0000101	æ	æ	33	233	583			_	8		
s10	1000	0000011	æ	æ	33	266	400		8	8	8		
s11	1000	0000100	æ	æ	33	266	533			8	8		
s12	1000	0000101	æ	æ	33	266	667			_	8		
s13	1001	0000010	æ	æ	33	300	300		8	8	8		
s14	1001	0000011	æ	æ	33	300	450	_		8	8		
s15	1001	0000100	æ	æ	33	300	600	_		—	8		
s16	1010	0000010	æ	æ	33	333	333	_	8	8	8		
s17	1010	0000011	æ	æ	33	333	500	_		8	8		
s18	1010	0000100	æ	æ	33	333	667	_		—	8		
c1	æ	æ	01001	0	33			300	8	8	8		
c2	æ	æ	01100	0	33	_	_	400	8	8	8		
c3	æ	æ	01110	0	33	_	_	466	_	8	8		
c4	æ	æ	01111	0	33			500	_	8	8		

Table 76. Suggested PLL Configurations



**Configuration Pin Muxing** 



Figure 57. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is  $V_1 = R_{source} \times I_{source}$ . Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value  $R_{term}$ . The measured voltage is  $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$ . Solving for the output impedance gives  $R_{source} = R_{term} \times (V_1/V_2 - 1)$ . The drive current is then  $I_{source} = V_1/R_{source}$ .

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum  $V_{DD}$ , nominal  $OV_{DD}$ , 105° C.

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R <sub>N</sub>	42 Target	25 Target	20 Target	Z <sub>0</sub>	W
R <sub>P</sub>	42 Target	25 Target	20 Target	Z <sub>0</sub>	W
Differential	NA	NA	NA	Z <sub>DIFF</sub>	W

**Table 79. Impedance Characteristics** 

**Note:** Nominal supply voltages. See Table 1,  $T_J = 105^{\circ}$  C.

# 23.6 Configuration Pin Muxing

The device provides the user with power-on configuration options that can be set through the use of external pull-up or pull-down resistors of 4.7 k $\Omega$ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While HRESET is asserted however, these pins are treated as inputs. The value presented on these pins while HRESET is asserted, is latched when HRESET deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.



# 23.7 Pull-Up Resistor Requirements

The device requires high resistance pull-up resistors (10 k $\Omega$  is recommended) on open drain type pins including I<sup>2</sup>C pins, Ethernet Management MDIO pin, and EPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, see *MPC8360E/MPC8358E PowerQUICC Design Checklist* (AN3097).

# 24 Ordering Information

# 24.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the MPC8360E/58E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. Additionally to the processor frequency, the part numbering scheme also includes an application modifier, which may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number.

MPC	nnnn	е	t	рр	aa	а	а	Α
Product Code	Part Identifier	Encryption Acceleration	Temperature Range	Package <sup>2</sup>	Processor Frequency <sup>3</sup>	Platform Frequency	QUICC Engine Frequency	Die Revision
MPC	8358	Blank = not included E = included	$Blank = 0^{\circ} C$ $T_A \text{ to } 105^{\circ} C$ $T_J$ $C = -40^{\circ} C T_A$ $to \; 105^{\circ} C T_J$	ZU = TBGA VV = TBGA (no lead)	e300 core speed AD = 266 MHz AG = 400 MHz	D = 266 MHz	E = 300 MHz G = 400 MHz	A = rev. 2.1 silicon
	8360				e300 core speed AG = 400 MHz AJ = 533 MHz AL = 667 MHz	D = 266 MHz F = 333 MHz	G = 400 MHz H = 500 MHz	A = rev. 2.1 silicon
MPC (rev. 2.0 silicon only)	8360	Blank = not included E = included	0° C T <sub>A</sub> to 70° C T <sub>J</sub>	ZU = TBGA VV = TBGA (no lead)	e300 core speed AH = 500 MHz AL = 667 MHz	F = 333 MHz	G = 400 MHz H = 500 MHz	_

## Table 80. Part Numbering Nomenclature<sup>1</sup>

#### Notes:

1. Not all processor, platform, and QUICC Engine block frequency combinations are supported. For available frequency combinations, contact your local Freescale sales office or authorized distributor.

2. See Section 20, "Package and Pin Listings," for more information on available package types.

Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this
specification support all core frequencies. Additionally, parts addressed by part number specifications may support other
maximum core frequencies.

This table shows the SVR settings by device and package type.

Table 81.	SVR	Settings
-----------	-----	----------

Device	Package	SVR (Rev. 2.0)	SVR (Rev. 2.1)
MPC8360E	TBGA	0x8048_0020	0x8048_0021
MPC8360	TBGA	0x8049_0020	0x8049_0021

#### How to Reach Us:

Home Page: www.freescale.com

Web Support: http://www.freescale.com/support

#### **USA/Europe or Locations Not Listed:**

Freescale Semiconductor, Inc. Technical Information Center, EL516 2100 East Elliot Road Tempe, Arizona 85284 1-800-521-6274 or +1-480-768-2130 www.freescale.com/support

#### Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH Technical Information Center Schatzbogen 7 81829 Muenchen, Germany +44 1296 380 456 (English) +46 8 52200080 (English) +49 89 92103 559 (German) +33 1 69 35 48 48 (French) www.freescale.com/support

#### Japan:

Freescale Semiconductor Japan Ltd. Headquarters ARCO Tower 15F 1-8-1, Shimo-Meguro, Meguro-ku Tokyo 153-0064 Japan 0120 191014 or +81 3 5437 9125 support.japan@freescale.com

#### Asia/Pacific:

Freescale Semiconductor China Ltd. Exchange Building 23F No. 118 Jianguo Road Chaoyang District Beijing 100022 China +86 10 5879 8000 support.asia@freescale.com

#### For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center 1-800 441-2447 or +1-303-675-2140 Fax: +1-303-675-2150 LDCForFreescaleSemiconductor @hibbertgroup.com Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale, the Freescale logo, and PowerQUICC are trademarks of Freescale Semiconductor, Inc. Reg. U.S. Pat. & Tm. Off. QUICC Engine is a trademark of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org. © 2011 Freescale Semiconductor, Inc.

Document Number: MPC8360EEC Rev. 5 09/2011



