NXP USA Inc. - MPC8360CVVAJDG Datasheet





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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8360cvvajdg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



- Eight TDM interfaces on the MPC8360E and four TDM interfaces on the MPC8358E with 1-bit mode for E3/T3 rates in clear channel
- Sixteen independent baud rate generators and 30 input clock pins for supplying clocks to UCC and MCC serial channels (MCC is only available on the MPC8360E)
- Four independent 16-bit timers that can be interconnected as four 32-bit timers
- Interworking functionality:
 - Layer 2 10/100-Base T Ethernet switch
 - ATM-to-ATM switching (AAL0, 2, 5)
 - Ethernet-to-ATM switching with L3/L4 support
 - PPP interworking
- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, 802.11i®, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs).
 - Public key execution unit (PKEU) supporting the following:
 - RSA and Diffie-Hellman
 - Programmable field size up to 2048 bits
 - Elliptic curve cryptography
 - F2m and F(p) modes
 - Programmable field size up to 511 bits
 - Data encryption standard execution unit (DEU)
 - DES, 3DES
 - Two key (K1, K2) or three key (K1, K2, K3)
 - ECB and CBC modes for both DES and 3DES
 - Advanced encryption standard unit (AESU)
 - Implements the Rinjdael symmetric key cipher
 - Key lengths of 128, 192, and 256 bits, two key
 - ECB, CBC, CCM, and counter modes
 - ARC four execution unit (AFEU)
 - Implements a stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
 - Message digest execution unit (MDEU)
 - SHA with 160-, 224-, or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either SHA or MD5 algorithm
 - Random number generator (RNG)
 - Four crypto-channels, each supporting multi-command descriptor chains
 - Static and/or dynamic assignment of crypto-execution units via an integrated controller
 - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
 - Storage/NAS XOR parity generation accelerator for RAID applications
- Dual DDR SDRAM memory controllers on the MPC8360E and a single DDR SDRAM memory controller on the MPC8358E
 - Programmable timing supporting both DDR1 and DDR2 SDRAM
 - On the MPC8360E, the DDR buses can be configured as two 32-bit buses or one 64-bit bus; on the MPC8358E, the DDR bus can be configured as a 32- or 64-bit bus
 - 32- or 64-bit data interface, up to 333 MHz (for the MPC8360E) and 266 MHz (for the MPC8358E) data rate
 - Four banks of memory, each up to 1 Gbyte



Table 1.	Absolute	Maximum	Ratings ¹	(continued)
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Characteristic	Symbol	Max Value	Unit	Notes
Storage temperature range	T _{STG}	-55 to 150	°C	_

Notes:

- 1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- 2. Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
- 3. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
- 4. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 100 ms during power-on reset and power-down sequences.
- 5. (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 3.
- 6. OV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 4.

2.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for the device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2.	Recommended	Operating	Conditions
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Characteristic	Symbol	Recommended Value	Unit	Notes
Core and PLL supply voltage for	V _{DD} & AV _{DD}	1.2 V ± 60 mV	V	1, 3
MPC8358 Device Part Number with Processor Frequency label of AD=266MHz and AG=400MHz & QUICC Engine Frequency label of E=300MHz & G=400MHz				
MPC8360 Device Part Number with Processor Frequency label of AG=400MHz and AJ=533MHz & QUICC Engine Frequency label of G=400MHz				
Core and PLL supply voltage for	V _{DD} & AV _{DD}	1.3 V ± 50 mV	V	1, 3
MPC8360 Device Part Number with Processor Frequency label of AL=667MHz and QUICC Engine Frequency label of H=500MHz				
DDR and DDR2 DRAM I/O supply voltage DDR DDR2	GV _{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	_
Three-speed Ethernet I/O supply voltage	LV _{DD} 0	3.3 V ± 330 mV 2.5 V ± 125 mV	V	_
Three-speed Ethernet I/O supply voltage	LV _{DD} 1	3.3 V ± 330 mV 2.5 V ± 125 mV	V	_
Three-speed Ethernet I/O supply voltage	LV _{DD} 2	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—





Table 4. MPC8360E TBGA Core Power Dissipation ¹	(continued)
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Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
667	333	500	6.1	6.8	W	2, 3, 5, 9

Notes:

- 1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 6.
- 2. Typical power is based on a voltage of V_{DD} = 1.2 V or 1.3 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.
- 3. Thermal solutions need to design to a value higher than typical power on the end application, T_A target, and I/O power.
- 4. Maximum power is based on a voltage of V_{DD} = 1.2 V, WC process, a junction T_J = 105°C, and an artificial smoke test.
- Maximum power is based on a voltage of V_{DD} = 1.3 V for applications that use 667 MHz (CPU)/500 (QE) with WC process, a junction T₁ = 105° C, and an artificial smoke test.
- 6. Typical power is based on a voltage of V_{DD} = 1.3 V, a junction temperature of T_J = 70° C, and a Dhrystone benchmark application.
- Maximum power is based on a voltage of V_{DD} = 1.3 V for applications that use 667 MHz (CPU) or 500 (QE) with WC process, a junction T_J = 70° C, and an artificial smoke test.
- 8. This frequency combination is only available for rev. 2.0 silicon.
- 9. This frequency combination is not available for rev. 2.0 silicon.

Table 5. MPC8358E TBGA Core Power Dissipation¹

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	300	4.1	4.5	W	2, 3, 4
400	266	400	4.5	5.0	W	2, 3, 4

Notes:

- 1. The values do not include I/O supply power (OV_{DD}, LV_{DD} , GV_{DD}) or AV_{DD} . For I/O power values, see Table 6.
- Typical power is based on a voltage of V_{DD} = 1.2 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.
- 3. Thermal solutions need to design to a value higher than typical power on the end application, T_A target, and I/O power.
- 4. Maximum power is based on a voltage of V_{DD} = 1.2 V, WC process, a junction T_J = 105°C, and an artificial smoke test.



Power Sequencing

This table shows the estimated typical I/O power dissipation for the device.

Interface	Parameter	GV _{DD} (1.8 V)	GV _{DD} (2.5 V)	OV _{DD} (3.3 V)	LV _{DD} (3.3 V)	LV _{DD} (2.5 V)	Unit	Comments
DDR I/O	200 MHz, 1 \times 32 bits	0.3	0.46	_	_	—	W	—
$R_s = 20 \Omega$	200 MHz, 1 \times 64 bits	0.4	0.58			—	W	—
$R_t = 50 \Omega$	200 MHz, 2×32 bits	0.6	0.92	_	_	—	W	_
	266 MHz, 1 \times 32 bits	0.35	0.56	_	_	—	W	_
	266 MHz, 1 \times 64 bits	0.46	0.7	_	_	—	W	_
	266 MHz, 2×32 bits	0.7	1.11		—	—	W	_
	333 MHz, 1 \times 32 bits	0.4	0.65	_	_	—	W	_
	333 MHz, 1 \times 64 bits	0.53	0.82		—	—	W	_
	333 MHz, 2×32 bits	0.81	1.3		—	—	W	_
Local Bus I/O	133 MHz, 32 bits	—	—	0.22	_	_	W	_
3 pairs of clocks	83 MHz, 32 bits	—	—	0.14	—	—	W	—
	66 MHz, 32 bits	—	—	0.12	—	—	W	_
	50 MHz, 32 bits	—	—	0.09	—	—	W	_
PCI I/O	33 MHz, 32 bits	—	—	0.05	—	—	W	_
Load = 30 pF	66 MHz, 32 bits	—	—	0.07	—	—	W	—
10/100/1000	MII or RMII	—	—	_	0.01	—	W	Multiply by
Load = 20 pF	GMII or TBI	—	—	_	0.04	—	W	interfaces used.
	RGMII or RTBI	—	—	—	—	0.04	W	
Other I/O	_	—	_	0.1	—	—	W	_

Table 6. Estimated Typical I/O Power Dissipation

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8360E/58E.

NOTE

The rise/fall time on QUICC Engine block input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of V_{DD} ; fall time refers to transitions from 90% to 10% of V_{DD} .



6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the device when $GV_{DD}(typ) = 1.8 \text{ V}.$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV _{DD}	1.71	1.89	V	1
I/O reference voltage	MV _{REF}	$0.49 imes \text{GV}_{\text{DD}}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.125	GV _{DD} + 0.3	V	_
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.125	V	_
Output leakage current	I _{OZ}	_	±10	μA	4
Output high current (V _{OUT} = 1.420 V)	I _{OH}	-13.4	—	mA	-
Output low current (V _{OUT} = 0.280 V)	I _{OL}	13.4	—	mA	-
MV _{REF} input leakage current	I _{VREF}	_	±10	μA	-
Input current (0 V ≰⁄ _{IN} ≤OV _{DD})	I _{IN}	—	±10	μA	_

Table 14. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.

 MV_{REF} is expected to equal 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} cannot exceed ±2% of the DC value.

 V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to equal MV_{REF}. This rail should track variations in the DC level of MV_{REF}.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

This table provides the DDR2 capacitance when $GV_{DD}(typ) = 1.8$ V.

Table 15. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) of the device when $GV_{DD}(typ) = 2.5 \text{ V}.$

Table 16. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	GV _{DD}	2.375	2.625	V	1
I/O reference voltage	MV _{REF}	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} - 0.04	MV _{REF} + 0.04	V	3



DDR and DDR2 SDRAM AC Electrical Characteristics

This table provides the input AC timing specifications for the DDR SDRAM interface when $GV_{DD}(typ) = 2.5 \text{ V}$.

Table 19. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V _{IL}	—	MV _{REF} – 0.31	V	—
AC input high voltage	V _{IH}	MV _{REF} + 0.31	_	V	_

Table 20. DDR and DDR2 SDRAM Input AC Timing Specifications Mode

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
MDQS—MDQ/MECC input skew per byte 333 MHz 266 MHz 200 MHz	t _{DISKEW}	-750 -1125 -1250	750 1125 1250	ps	1, 2

Notes:

1. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.

Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 ≤n ≤7) or ECC (MECC[{0...7}] if n = 8).

This figure shows the input timing diagram for the DDR controller.



Figure 6. DDR Input Timing Diagram





This section describes the DC and AC electrical specifications for the DUART interface of the MPC8360E/58E.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface of the device.

Table 23. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit	Notes
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V	—
Low-level input voltage OV _{DD}	V _{IL}	-0.3	0.8	V	—
High-level output voltage, I _{OH} = −100 μA	V _{OH}	OV _{DD} - 0.4	—	V	—
Low-level output voltage, I _{OL} = 100 μA	V _{OL}	—	0.2	V	—
Input current (0 V ≰⁄ _{IN} ≤OV _{DD})	I _{IN}	—	±10	μA	1

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface of the device.

Table 24.	DUART	AC T	iming	Speci	ifications
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Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	_
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	_	2

Notes:

- 1. Actual attainable baud rate is limited by the latency of interrupt processing.
- 2. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

8 UCC Ethernet Controller: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

8.1 Three-Speed Ethernet Controller (10/100/1000 Mbps)— GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), MII (media independent interface), RMII (reduced media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The MII, RMII, GMII, and TBI interfaces are only defined for 3.3 V, while the RGMII and RTBI interfaces are only defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet



GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for the MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

8.1.1 10/100/1000 Ethernet DC Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), reduced media independent interface (RMII) signals, management data input/output (MDIO) and management data clock (MDC).

The MII and RMII interfaces are defined for 3.3 V, while the RGMII and RTBI interfaces can be operated at 2.5 V. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3*. The RMII interface follows the *RMII Consortium RMII Specification Version 1.2*.

Table 25. RGMII/RTBI, GMII, TBI, MII, and RMII DC Electrical Characteristics (when operating at 3.3 V)

Parameter	Symbol	Conditions		Min	Мах	Unit	Notes
Supply voltage 3.3 V	LV _{DD}	—		2.97	3.63	V	1
Output high voltage	V _{OH}	I _{OH} = -4.0 mA	$LV_{DD} = Min$	2.40	LV _{DD} + 0.3	V	—
Output low voltage	V _{OL}	I _{OL} = 4.0 mA	$LV_{DD} = Min$	GND	0.50	V	—
Input high voltage	V _{IH}	—	_	2.0	LV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	—	_	-0.3	0.90	V	—
Input current	I _{IN}	0 V ≤V _{IN} ≤LV _{DD}		—	±10	μA	—

Note:

1. GMII/MII pins that are not needed for RGMII, RMII, or RTBI operation are powered by the OV_{DD} supply.

Table 26. RGMII/RTBI DC Electrical Characteristics	(when o	perating	at 2.5 V)
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Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV _{DD}	-	_	2.37	2.63	V
Output high voltage	V _{OH}	I _{OH} = -1.0 mA	LV _{DD} = Min	2.00	LV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	$LV_{DD} = Min$	GND – 0.3	0.40	V
Input high voltage	V _{IH}	—	LV _{DD} = Min	1.7	LV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	$LV_{DD} = Min$	-0.3	0.70	V
Input current	I _{IN}	0 V ≤V _{IN} ≤LV _{DD}		—	±10	μA

8.2 GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII Timing Specifications

This sections describe the GMII transmit and receive AC timing specifications.



Ethernet Management Interface Electrical Characteristics

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.



Figure 20. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI, and RTBI are specified in Section 8.1, "Three-Speed Ethernet Controller (10/100/1000 Mbps)— GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage (3.3 V)	OV _{DD}	—		2.97	3.63	V
Output high voltage	V _{OH}	$I_{OH} = -1.0 \text{ mA}$	$OV_{DD} = Min$	2.10	OV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	$OV_{DD} = Min$	GND	0.50	V
Input high voltage	V _{IH}	—		2.00	—	V
Input low voltage	V _{IL}	—		—	0.80	V
Input current	I _{IN}	0 V ≤V _{IN}	₁≤OV _{DD}	—	±10	μA

Table 36. MII Management DC Electrica	I Characteristics When Powered at 3.3 V
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Local Bus AC Electrical Specifications

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to output valid	t _{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ}		4	ns	8

Table 41. Local Bus General Timing Parameters—DLL Bypass Mode⁹ (continued)

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the to the output (O) going invalid (X) or output hold time.
 </sub>
- 2. All timings are in reference to falling edge of LCLK0 (for all outputs and for LGTA and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
- 3. All signals are measured from OV_{DD}/2 of the rising/falling edge of LCLK0 to 0.4 × OV_{DD} of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. t_{LBOTOT1} should be used when RCWH[LALE] is not set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- t_{LBOTOT2} should be used when RCWH[LALE] is set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- 7. t_{LBOTOT3} should be used when RCWH[LALE] is set and when the load on LALE output pin equals to the load on LAD output pins.
- 8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 9. DLL bypass mode is not recommended for use at frequencies above 66 MHz.

This figure provides the AC test load for the local bus.



Figure 22. Local Bus C Test Load



These figures show the local bus signals.



Figure 24. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)

PCI AC Electrical Specifications

Table 47. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Clock to output high impedance	t _{PCKHOZ}	_	14	ns	2, 3
Input setup to clock	t _{PCIVKH}	3.0	_	ns	2, 4
Input hold from clock	t _{PCIXKH}	0.3	_	ns	2, 4, 6

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
 </sub>
- 2. See the timing measurement conditions in the PCI 2.2 Local Bus Specifications.
- 3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.
- 5. In rev. 2.0 silicon, due to errata, t_{PCIHOV} maximum is 6.6 ns. Refer to Errata PCI21 in Chip Errata for the MPC8360E, Rev. 1.
- 6. In rev. 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Refer to Errata PCI17 in Chip Errata for the MPC8360E, Rev. 1.

Table 48. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Clock to output valid	t _{PCKHOV}	_	11	ns	2
Output hold from clock	t _{PCKHOX}	2	—	ns	2
Clock to output high impedance	t _{PCKHOZ}	_	14	ns	2, 3
Input setup to clock	t _{PCIVKH}	7.0	—	ns	2, 2
Input hold from clock	t _{PCIXKH}	0.3	—	ns	2, 4, 5

Notes:

- The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
- 2. See the timing measurement conditions in the PCI 2.2 Local Bus Specifications.
- 3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.
- 5. In rev. 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Refer to Errata PCI17 in Chip Errata for the MPC8360E, Rev. 1.

This figure provides the AC test load for PCI.



Figure 36. PCI AC Test Load



This figure shows the TDM/SI timing with external clock.



Note: The clock edge is selectable on TDM/SI



17.3 UTOPIA/POS

This section describes the DC and AC electrical specifications for the UTOPIA/POS of the MPC8360E/58E.

17.4 UTOPIA/POS DC Electrical Characteristics

This table provides the DC electrical characteristics for the device UTOPIA.

 Table 59. UTOPIA DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	_	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	$0 V \leq V_{IN} \leq OV_{DD}$	—	±10	μA

17.5 UTOPIA/POS AC Timing Specifications

This table provides the UTOPIA input and output AC timing specifications.

Table 60. UTOPIA AC Timing Specifications¹

Characteristic	Symbol ²	Min	Мах	Unit	Notes
UTOPIA outputs—Internal clock delay	t _{UIKHOV}	0	11.5	ns	
UTOPIA outputs—External clock delay	t _{UEKHOV}	1	11.6	ns	_
UTOPIA outputs—Internal clock high impedance	t _{UIKHOX}	0	8.0	ns	_
UTOPIA outputs—External clock high impedance	t _{UEKHOX}	1	10.0	ns	_
UTOPIA inputs—Internal clock input setup time	t _{UIIVKH}	6	_	ns	_
UTOPIA inputs—External clock input setup time	t _{UEIVKH}	4	—	ns	3

Table 60. UTOPIA AC Timing Specifications¹ (continued)

Characteristic	Symbol ²	Min	Мах	Unit	Notes
UTOPIA inputs—Internal clock input hold time	t _{UIIXKH}	2.4	—	ns	
UTOPIA inputs—External clock input hold time	t _{UEIXKH}	1	—	ns	3

Notes:

- 1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{UIKHOX} symbolizes the UTOPIA outputs internal timing (UI) for the time t_{UTOPIA} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
 </sub>
- In rev. 2.0 silicon, due to errata, t_{UEIVKH} minimum is 4.3 ns and t_{UEIXKH} minimum is 1.4 ns under specific conditions. Refer to Errata QE_UPC3 in *Chip Errata for the MPC8360E, Rev. 1.*

This figure provides the AC test load for the UTOPIA.



Figure 46. UTOPIA AC Test Load

These figures represent the AC timing from Table 56. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the UTOPIA timing with external clock.



Figure 47. UTOPIA AC Timing (External Clock) Diagram



NP

20.3 Pinout Listings

Refer to AN3097, "MPC8360/MPC8358E PowerQUICC Design Checklist," for proper pin termination and usage.

This table shows the pin list of the MPC8360E TBGA package.

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Pri	mary DDR SDRAM Memory Controller Interface			
MEMC1_MDQ[0:31]	AJ34, AK33, AL33, AL35, AJ33, AK34, AK32, AM36, AN37, AN35, AR34, AT34, AP37, AP36, AR36, AT35, AP34, AR32, AP32, AM31, AN33, AM34, AM33, AM30, AP31, AM27, AR30, AT32, AN29, AP29, AN27, AR29	I/O	GV _{DD}	_
MEMC1_MDQ[32:63]/ MEMC2_MDQ[0:31]	AN8, AN7, AM8, AM6, AP9, AN9, AT7, AP7, AU6, AP6, AR4, AR3, AT6, AT5, AR5, AT3, AP4, AM5, AP3, AN3, AN5, AL5, AN4, AM2, AL2, AH5, AK3, AJ2, AJ3, AH4, AK4, AH3	I/O	GV _{DD}	_
MEMC1_MECC[0:4]/ MSRCID[0:4]	AP24, AN22, AM19, AN19, AM24	I/O	GV _{DD}	_
MEMC1_MECC[5]/ MDVAL	AM23	I/O	GV _{DD}	—
MEMC1_MECC[6:7]	AM22, AN18	I/O	GV _{DD}	—
MEMC1_MDM[0:3]	AL36, AN34, AP33, AN28	0	GV _{DD}	—
MEMC1_MDM[4:7]/ MEMC2_MDM[0:3]	AT9, AU4, AM3, AJ6	0	GV _{DD}	—
MEMC1_MDM[8]	AP27	0	GV _{DD}	—
MEMC1_MDQS[0:3]	AK35, AP35, AN31, AM26	I/O	GV _{DD}	—
MEMC1_MDQS[4:7]/ MEMC2_MDQS[0:3]	AT8, AU3, AL4, AJ5	I/O	GV _{DD}	—
MEMC1_MDQS[8]	AP26	I/O	GV _{DD}	—
MEMC1_MBA[0:1]	AU29, AU30	0	GV _{DD}	—
MEMC1_MBA[2]	AT30	0	GV _{DD}	_
MEMC1_MA[0:14]	AU21, AP22, AP21, AT21, AU25, AU26, AT23, AR26, AU24, AR23, AR28, AU23, AR22, AU20, AR18	0	GV _{DD}	-
MEMC1_MODT[0:1]	AG33, AJ36	0	GV _{DD}	6
MEMC1_MODT[2:3]/ MEMC2_MODT[0:1]	AT1, AK2	0	GV _{DD}	6
MEMC1_MWE	AT26	0	GV _{DD}	—
MEMC1_MRAS	AT29	0	GV _{DD}	—
MEMC1_MCAS	AT24	0	GV _{DD}	_
MEMC1_MCS[0:1]	AU27, AT27	0	GV _{DD}	_
MEMC1_MCS[2:3]/ MEMC2_MCS[0:1]	AU8, AU7	0	GV _{DD}	

Table 66. MPC8360E TBGA Pinout Listing



Pinout Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC1_MCKE[0:1]	AL32, AU33	0	GV _{DD}	3
MEMC1_MCK[0:1]	AK37, AT37	0	GV _{DD}	
MEMC1_MCK[2:3]/ MEMC2_MCK[0:1]	AN1, AR2	0	GV _{DD}	-
MEMC1_MCK[4:5]/ MEMC2_MCKE[0:1]	AN25, AK1	0	GV _{DD}	_
MEMC1_MCK[0:1]	AL37, AT36	0	GV _{DD}	_
MEMC1_MCK[2:3]/ MEMC2_MCK[0:1]	AP2, AT2	0	GV _{DD}	_
MEMC1_MCK[4]/ MEMC2_MDM[8]	AN24	0	GV _{DD}	
MEMC1_MCK[5]/ MEMC2_MDQS[8]	AL1	0	GV _{DD}	_
MDIC[0:1]	АН6, АР30	I/O	GV _{DD}	10
Sec	ondary DDR SDRAM Memory Controller Interface			
MEMC2_MECC[0:7]	AN16, AP18, AM16, AM17, AN17, AP13, AP15, AN13	I/O	GV _{DD}	_
MEMC2_MBA[0:2]	AU12, AU15, AU13	0	GV _{DD}	_
MEMC2_MA[0:14]	AT12, AP11, AT13, AT14, AR13, AR15, AR16, AT16, AT18, AT17, AP10, AR20, AR17, AR14, AR11	0	GV _{DD}	_
MEMC2_MWE	AU10	0	GV _{DD}	_
MEMC2_MRAS	AT11	0	GV _{DD}	_
MEMC2_MCAS	AU11	0	GV _{DD}	
	PCI			
PCI_INTA/IRQ_OUT/CE_PF[5]	A20	I/O	LV _{DD} 2	2
PCI_RESET_OUT/CE_PF[6]	E19	I/O	LV _{DD} 2	_
PCI_AD[31:30]/CE_PG[31:30]	D20, D21	I/O	LV _{DD} 2	
PCI_AD[29:25]/CE_PG[29:25]	A24, B23, C23, E23, A26	I/O	OV _{DD}	
PCI_AD[24]/CE_PG[24]	B21	I/O	LV _{DD} 2	_
PCI_AD[23:0]/CE_PG[23:0]	C24, C25, D25, B25, E24, F24, A27, A28, F27, A30, C30, D30, E29, B31, C31, D31, D32, A32, C33, B33, F30, E31, A34, D33	I/O	OV _{DD}	
PCI_C/BE[3:0]/CE_PF[10:7]	E22, B26, E28, F28	I/O	OV _{DD}	
PCI_PAR/CE_PF[11]	D28	I/O	OV _{DD}	
PCI_FRAME/CE_PF[12]	D26	I/O	OV _{DD}	5
PCI_TRDY/CE_PF[13]	C27	I/O	OV _{DD}	5
PCI_IRDY/CE_PF[14]	C28	I/O	OV _{DD}	5
PCI_STOP/CE_PF[15]	B28	I/O	OV _{DD}	5



Pinout Listings

21 Clocking

This figure shows the internal distribution of clocks within the MPC8360E.



Figure 54. MPC8360E Clock Subsystem



Pinout Listings

clock. When the device is configured as a PCI agent device the CLKIN and the CFG_CLKIN_DIV signals should be tied to GND.

When the device is configured as a PCI host device (RCWH[PCIHOST] = 1) and PCI clock output is disabled (RCWH[PCICKDRV] = 0), clock distribution and balancing done externally on the board. Therefore, PCI_SYNC_IN is the primary input clock.

As shown in Figure 54 and Figure 55, the primary clock input (frequency) is multiplied by the QUICC Engine block phase-locked loop (PLL), the system PLL, and the clock unit to create the QUICC Engine clock (ce_clk), the coherent system bus clock (csb_clk), the internal DDRC1 controller clock ($ddr1_clk$), and the internal clock for the local bus interface unit and DDR2 memory controller (lb_clk).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb_clk = \{PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)\} \times SPMF$$

In PCI host mode, PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV) is the CLKIN frequency; in PCI agent mode, CFG_CLKIN_DIV must be pulled down (low), so PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV) is the PCI_CLK frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, "Reset, Clocking, and Initialization," in the *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more information on the clock subsystem.

The *ce_clk* frequency is determined by the QUICC Engine PLL multiplication factor (RCWL[CEPMF) and the QUICC Engine PLL division factor (RCWL[CEPDF]) according to the following equation:

 $ce_clk = (primary clock input \times CEPMF) \div (1 + CEPDF)$

The internal *ddr1_clk* frequency is determined by the following equation:

 $ddr1_clk = csb_clk \times (1 + RCWL[DDR1CM])$

Note that the lb_clk clock frequency (for DDRC2) is determined by RCWL[LBCM]. The *internal ddr1_clk* frequency is not the external memory bus frequency; *ddr1_clk* passes through the DDRC1 clock divider (\div 2) to create the differential DDRC1 memory bus clock outputs (MEMC1_MCK and MEMC1_MCK). However, the data rate is the same frequency as *ddr1_clk*.

The internal *lb_clk* frequency is determined by the following equation:

 $lb_clk = csb_clk \times (1 + \text{RCWL[LBCM]})$

Note that *lb_clk* is not the external local bus or DDRC2 frequency; *lb_clk* passes through the a LB clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LB clock divider ratio is controlled by LCRR[CLKDIV].

Additionally, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. This table specifies which units have a configurable clock frequency.

Unit	Default Frequency	Options
Security core	csb_clk/3	Off, <i>csb_clk</i> ¹ , <i>csb_clk</i> /2, <i>csb_clk</i> /3
PCI and DMA complex	csb_clk	Off, <i>csb_clk</i>

Table 68	Configurable	Clock	Units
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¹ With limitation, only for slow csb_clk rates, up to 166 MHz.

This table provides the operating frequencies for the TBGA package under recommended operating conditions (see Table 2). All frequency combinations shown in the table below may not be available. Maximum operating frequencies depend on the part

System PLL Configuration

RCWL[SPMF]	System PLL Multiplication Factor
1100	× 12
1101	× 13
1110	× 14
1111	× 15

The RCWL[SVCOD] denotes the system PLL VCO internal frequency as shown in this table.

VCO Divider
4
8
2
Reserved

Table 71. System PLL VCO Divider

NOTE

The VCO divider must be set properly so that the system VCO frequency is in the range of 600-1400 MHz.

The system VCO frequency is derived from the following equations:

- $csb_clk = \{PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)\} \times SPMF$
- System VCO Frequency = *csb_clk* × VCO divider (if both RCWL[DDRCM] and RCWL[LBCM] are cleared) OR
- System VCO frequency = $2 \times csb_clk \times$ VCO divider (if either RCWL[DDRCM] or RCWL[LBCM] are set).

As described in Section 21, "Clocking," the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). This table shows the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

CFG_CLKIN_DIV at Reset ¹	SPMF	csb_clk: Input Clock Ratio ²	Input Clock Frequency (MHz) ²			
			16.67	25	33.33	66.67
			<i>csb_clk</i> Frequency (MHz)			
Low	0010	2:1				133
Low	0011	3:1			100	200
Low	0100	4:1		100	133	266
Low	0101	5:1		125	166	333

Table 72. CSB Frequency Options



QUICC Engine Block PLL Configuration

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF])
11101	0	× 29
11110	0	× 30
11111	0	× 31
00011	1	× 1.5
00101	1	× 2.5
00111	1	× 3.5
01001	1	× 4.5
01011	1	× 5.5
01101	1	× 6.5
01111	1	× 7.5
10001	1	× 8.5
10011	1	× 9.5
10101	1	× 10.5
10111	1	× 11.5
11001	1	× 12.5
11011	1	× 13.5
11101	1	× 14.5

Table 74. QUICC Engine Block PLL Multiplication Factors (continued)

Note:

1. Reserved modes are not listed.

The RCWL[CEVCOD] denotes the QUICC Engine Block PLL VCO internal frequency as shown in this table.

Table 75. QUICC Engine Block PLL VCO Divider

RCWL[CEVCOD]	VCO Divider		
00	4		
01	8		
10	2		
11	Reserved		

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine block VCO frequency is in the range of 600–1400 MHz. The QUICC Engine block frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine block frequencies should be selected according to the performance requirements.