



Welcome to E-XFL.COM

Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8360czuaddh

wide range of protocols including ATM, Ethernet, HDLC, and POS. The QUICC Engine module's enhanced interworking eases the transition and reduces investment costs from ATM to IP based systems. The other major features include a dual DDR SDRAM memory controller for the MPC8360E, which allows equipment providers to partition system parameters and data in an extremely efficient way, such as using one 32-bit DDR memory controller for control plane processing and the other for data plane processing. The MPC8358E has a single DDR SDRAM memory controller. The MPC8360E/58E also offers a 32-bit PCI controller, a flexible local bus, and a dedicated security engine.

This figure shows the MPC8360E block diagram.

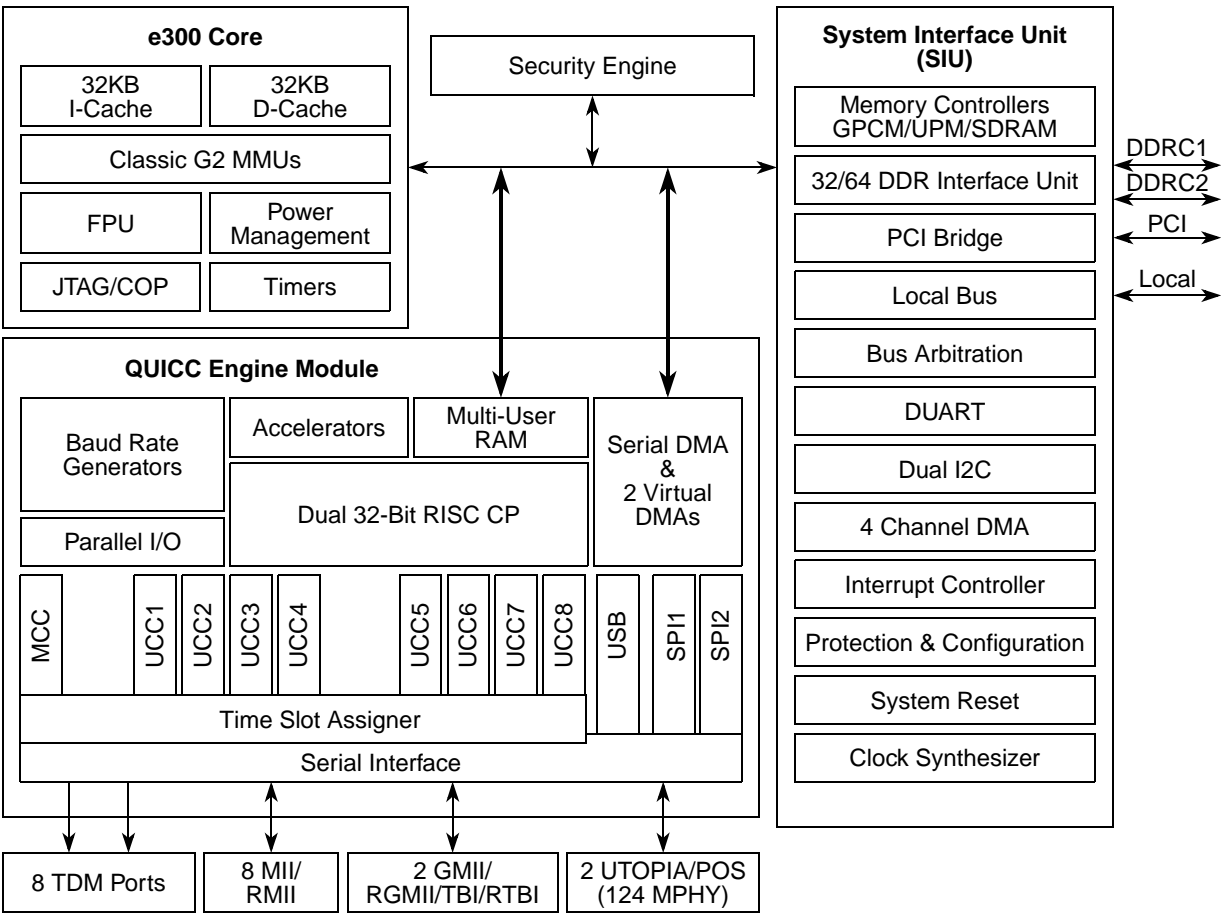


Figure 1. MPC8360E Block Diagram

This figure shows the undershoot and overshoot voltage of the PCI interface of the device for the 3.3-V signals, respectively.

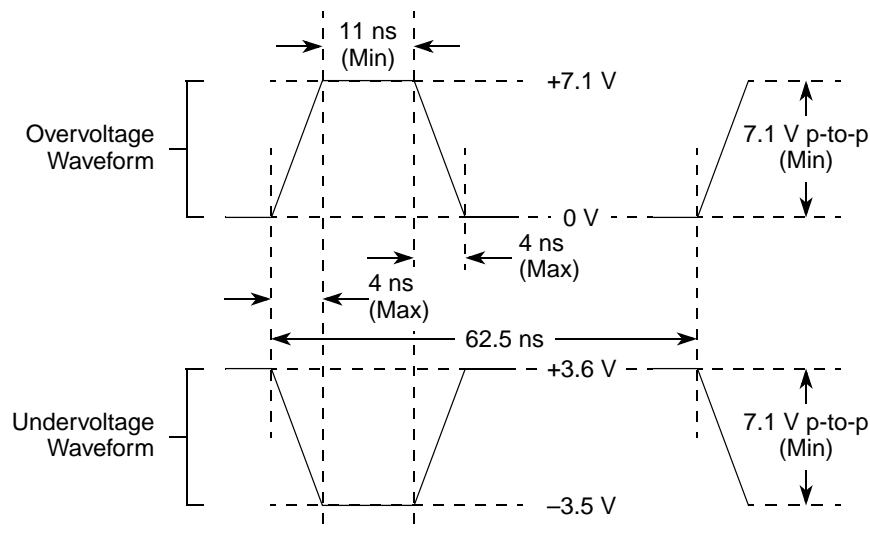


Figure 4. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	$OV_{DD} = 3.3\text{ V}$
PCI signals	25	
PCI output clocks (including PCI_SYNC_OUT)	42	
DDR signal	20 36 (half-strength mode) ¹	$GV_{DD} = 2.5\text{ V}$
DDR2 signal	18 36 (half-strength mode) ¹	$GV_{DD} = 1.8\text{ V}$
10/100/1000 Ethernet signals	42	$LV_{DD} = 2.5/3.3\text{ V}$
DUART, system control, I ² C, SPI, JTAG	42	$OV_{DD} = 3.3\text{ V}$
GPIO signals	42	$OV_{DD} = 3.3\text{ V}$ $LV_{DD} = 2.5/3.3\text{ V}$

Note:

1. DDR output impedance values for half strength mode are verified by design and not tested.

2.2 Power Sequencing

This section details the power sequencing considerations for the MPC8360E/58E.

Table 4. MPC8360E TBGA Core Power Dissipation¹ (continued)

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
667	333	500	6.1	6.8	W	2, 3, 5, 9

Notes:

1. The values do not include I/O supply power (OV_{DD} , LV_{DD} , GV_{DD}) or AV_{DD} . For I/O power values, see [Table 6](#).
2. Typical power is based on a voltage of $V_{DD} = 1.2$ V or 1.3 V, a junction temperature of $T_J = 105^\circ\text{C}$, and a Dhrystone benchmark application.
3. Thermal solutions need to design to a value higher than typical power on the end application, T_A target, and I/O power.
4. Maximum power is based on a voltage of $V_{DD} = 1.2$ V, WC process, a junction $T_J = 105^\circ\text{C}$, and an artificial smoke test.
5. Maximum power is based on a voltage of $V_{DD} = 1.3$ V for applications that use 667 MHz (CPU)/500 (QE) with WC process, a junction $T_J = 105^\circ\text{C}$, and an artificial smoke test.
6. Typical power is based on a voltage of $V_{DD} = 1.3$ V, a junction temperature of $T_J = 70^\circ\text{C}$, and a Dhrystone benchmark application.
7. Maximum power is based on a voltage of $V_{DD} = 1.3$ V for applications that use 667 MHz (CPU) or 500 (QE) with WC process, a junction $T_J = 70^\circ\text{C}$, and an artificial smoke test.
8. This frequency combination is only available for rev. 2.0 silicon.
9. This frequency combination is not available for rev. 2.0 silicon.

Table 5. MPC8358E TBGA Core Power Dissipation¹

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	300	4.1	4.5	W	2, 3, 4
400	266	400	4.5	5.0	W	2, 3, 4

Notes:

1. The values do not include I/O supply power (OV_{DD} , LV_{DD} , GV_{DD}) or AV_{DD} . For I/O power values, see [Table 6](#).
2. Typical power is based on a voltage of $V_{DD} = 1.2$ V, a junction temperature of $T_J = 105^\circ\text{C}$, and a Dhrystone benchmark application.
3. Thermal solutions need to design to a value higher than typical power on the end application, T_A target, and I/O power.
4. Maximum power is based on a voltage of $V_{DD} = 1.2$ V, WC process, a junction $T_J = 105^\circ\text{C}$, and an artificial smoke test.

5.3 QUICC Engine Block Operating Frequency Limitations

This section specifies the limits of the AC electrical characteristics for the operation of the QUICC Engine block's communication interfaces.

NOTE

The settings listed below are required for correct hardware interface operation. Each protocol by itself requires a minimal QUICC Engine block operating frequency setting for meeting the performance target. Because the performance is a complex function of all the QUICC Engine block settings, the user should make use of the QUICC Engine block performance utility tool provided by Freescale to validate their system.

This table lists the maximal QUICC Engine block I/O frequencies and the minimal QUICC Engine block core frequency for each interface.

Table 13. QUICC Engine Block Operating Frequency Limitations

Interface	Interface Operating Frequency (MHz)	Max Interface Bit Rate (Mbps)	Min QUICC Engine Operating Frequency ¹ (MHz)	Notes
Ethernet Management: MDC/MDIO	10 (max)	10	20	—
MII	25 (typ)	100	50	—
RMII	50 (typ)	100	50	—
GMII/RGMII/TBI/RTBI	125 (typ)	1000	250	—
SPI (master/slave)	10 (max)	10	20	—
UCC through TDM	50 (max)	70	$8 \times F$	2
MCC	25 (max)	16.67	$16 \times F$	2, 4
UTOPIA L2	50 (max)	800	$2 \times F$	2
POS-PHY L2	50 (max)	800	$2 \times F$	2
HDLC bus	10 (max)	10	20	—
HDLC/transparent	50 (max)	50	$8/3 \times F$	2, 3
UART/asynch HDLC	3.68 (max internal ref clock)	115 (Kbps)	20	—
BISYNC	2 (max)	2	20	—
USB	48 (ref clock)	12	96	—

Notes:

1. The QUICC Engine module needs to run at a frequency higher than or equal to what is listed in this table.
2. 'F' is the actual interface operating frequency.
3. The bit rate limit is independent of the data bus width (that is, the same for serial, nibble, or octal interfaces).
4. TDM in high-speed mode for serial data interface.

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR and DDR2 SDRAM interface of the MPC8360E/58E.

Table 16. DDR SDRAM DC Electrical Characteristics for $GV_{DD}(typ) = 2.5\text{ V}$ (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.18$	V	—
Output leakage current	I_{OZ}	—	± 10	μA	4
Output high current ($V_{OUT} = 1.95\text{ V}$)	I_{OH}	-15.2	—	mA	—
Output low current ($V_{OUT} = 0.35\text{ V}$)	I_{OL}	15.2	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	± 10	μA	—
Input current ($0\text{ V} \leq V_{IN} \leq OV_{DD}$)	I_{IN}	—	± 10	μA	—

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} . This rail should track variations in the DC level of MV_{REF} .
4. Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.

This table provides the DDR capacitance when $GV_{DD}(typ) = 2.5\text{ V}$.

Table 17. DDR SDRAM Capacitance for $GV_{DD}(typ) = 2.5\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 2.5\text{ V} \pm 0.125\text{ V}$, $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM interface when $GV_{DD}(typ) = 1.8\text{ V}$.

Table 18. DDR2 SDRAM Input AC Timing Specifications for $GV_{DD}(typ) = 1.8\text{ V}$

At recommended operating conditions with GV_{DD} of $1.8\text{ V} \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.25$	V	—
AC input high voltage	V_{IH}	$MV_{REF} + 0.25$	—	V	—

This table provides the input AC timing specifications for the DDR SDRAM interface when $GV_{DD}(typ) = 2.5\text{ V}$.

Table 19. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of $2.5\text{ V} \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.31$	V	—
AC input high voltage	V_{IH}	$MV_{REF} + 0.31$	—	V	—

Table 20. DDR and DDR2 SDRAM Input AC Timing Specifications Mode

At recommended operating conditions with GV_{DD} of $(1.8\text{ or }2.5\text{ V}) \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
MDQS—MDQ/MECC input skew per byte 333 MHz 266 MHz 200 MHz	t_{DISKEW}	−750 −1125 −1250	750 1125 1250	ps	1, 2

Notes:

1. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.
2. Maximum possible skew between a data strobe ($MDQS[n]$) and any corresponding bit of data ($MDQ[8n + \{0...7\}]$ if $0 \leq n \leq 7$) or ECC ($MECC[\{0...7\}]$ if $n = 8$).

This figure shows the input timing diagram for the DDR controller.

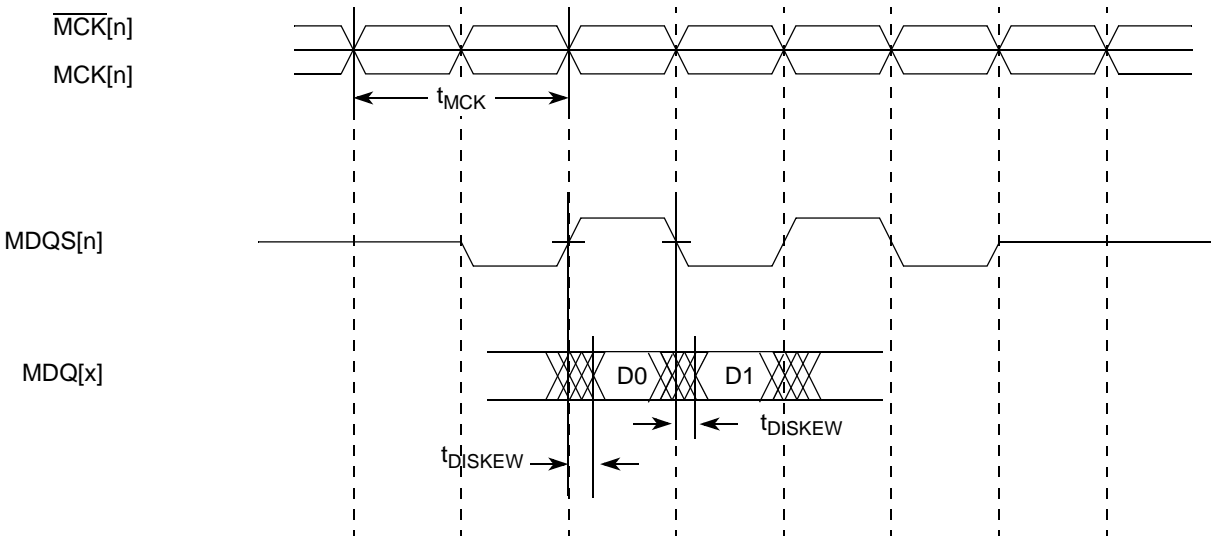


Figure 6. DDR Input Timing Diagram

Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for the MDIO and MDC are specified in [Section 8.3, “Ethernet Management Interface Electrical Characteristics.”](#)

8.1.1 10/100/1000 Ethernet DC Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), reduced media independent interface (RMII) signals, management data input/output (MDIO) and management data clock (MDC).

The MII and RMII interfaces are defined for 3.3 V, while the RGMII and RTBI interfaces can be operated at 2.5 V. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3*. The RMII interface follows the *RMII Consortium RMII Specification Version 1.2*.

Table 25. RGMII/RTBI, GMII, TBI, MII, and RMII DC Electrical Characteristics (when operating at 3.3 V)

Parameter	Symbol	Conditions		Min	Max	Unit	Notes
Supply voltage 3.3 V	V_{DD}	—		2.97	3.63	V	1
Output high voltage	V_{OH}	$I_{OH} = -4.0 \text{ mA}$	$V_{DD} = \text{Min}$	2.40	$V_{DD} + 0.3$	V	—
Output low voltage	V_{OL}	$I_{OL} = 4.0 \text{ mA}$	$V_{DD} = \text{Min}$	GND	0.50	V	—
Input high voltage	V_{IH}	—	—	2.0	$V_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	—	—	-0.3	0.90	V	—
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq V_{DD}$		—	± 10	μA	—

Note:

1. GMII/II pins that are not needed for RGMII, RMII, or RTBI operation are powered by the OV_{DD} supply.

Table 26. RGMII/RTBI DC Electrical Characteristics (when operating at 2.5 V)

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	V_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0 \text{ mA}$	$V_{DD} = \text{Min}$	2.00	$V_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0 \text{ mA}$	$V_{DD} = \text{Min}$	GND - 0.3	0.40	V
Input high voltage	V_{IH}	—	$V_{DD} = \text{Min}$	1.7	$V_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	$V_{DD} = \text{Min}$	-0.3	0.70	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq V_{DD}$		—	± 10	μA

8.2 GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII Timing Specifications

This sections describe the GMII transmit and receive AC timing specifications.

8.2.1.2 GMII Receive AC Timing Specifications

This table provides the GMII receive AC timing specifications.

Table 28. GMII Receive AC Timing Specifications

At recommended operating conditions with V_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
RX_CLK clock period	t_{GRX}	—	8.0	—	ns	—
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	%	—
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns	—
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.2	—	—	ns	2
RX_CLK clock rise time, (20% to 80%)	t_{GRXR}	—	—	1.0	ns	—
RX_CLK clock fall time, (80% to 20%)	t_{GRXF}	—	—	1.0	ns	—

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- In rev. 2.0 silicon, due to errata, t_{GRDXKH} minimum is 0.5 which is not compliant with the standard. Refer to Errata *QE_ENET18* in *Chip Errata for the MPC8360E, Rev. 1*.

This figure shows the GMII receive AC timing diagram.

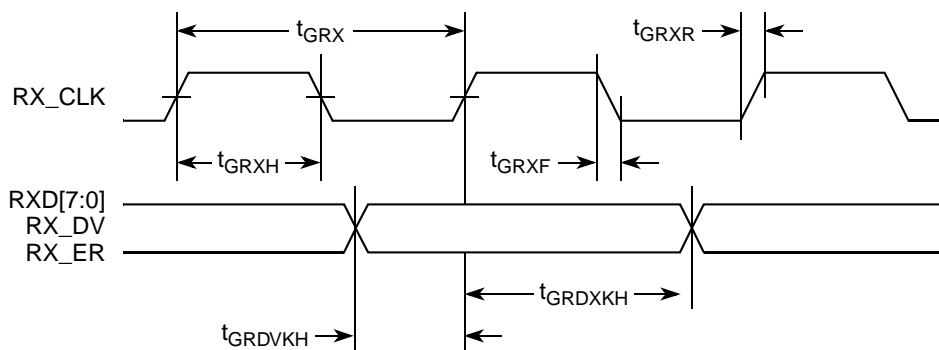


Figure 11. GMII Receive AC Timing Diagram

8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.2.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 29. MII Transmit AC Timing Specifications

At recommended operating conditions with V_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX} t_{MTKHDX}	1 —	5	— 15	ns
TX_CLK data clock rise time, (20% to 80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall time, (80% to 20%)	t_{MTXF}	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the MII transmit AC timing diagram.

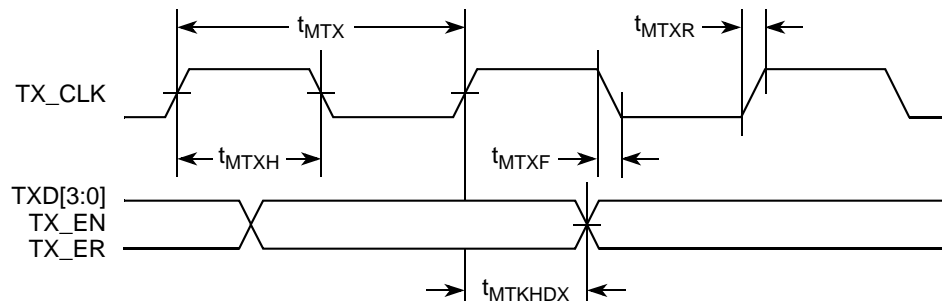


Figure 12. MII Transmit AC Timing Diagram

8.2.2.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 30. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise time, (20% to 80%)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time, (80% to 20%)	t_{MRXF}	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load.

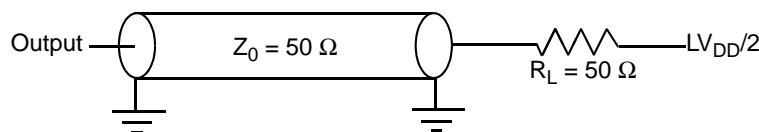


Figure 13. AC Test Load

This figure shows the MII receive AC timing diagram.

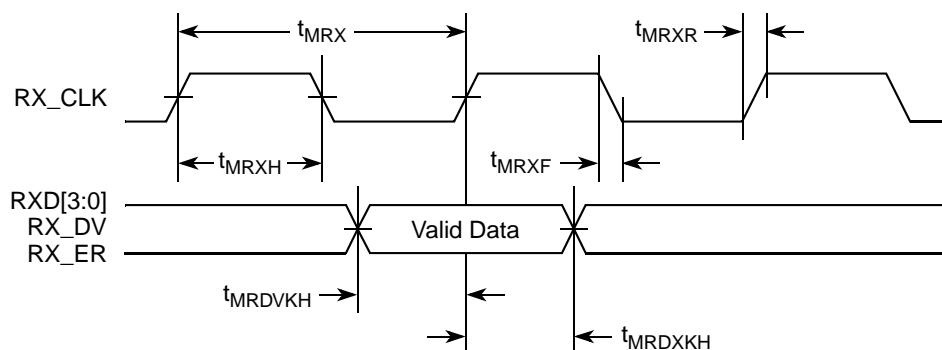


Figure 14. MII Receive AC Timing Diagram

8.2.5 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 35. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with V_{DD} of 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	$t_{SKRGTKHDX}$ $t_{SKRGTKHDV}$	−0.5 —	—	— 0.5	ns	7
Data to clock input skew (at receiver)	$t_{SKRGDXKH}$ $t_{SKRGDVKH}$	1.0 —	—	— 2.6	ns	2
Clock cycle duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	t_{RGTH}/t_{RGT}	45	50	55	%	4, 5
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 5
Rise time (20–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20–80%)	t_{RGTF}	—	—	0.75	ns	—
GTX_CLK125 reference clock period	t_{G125}	—	8.0	—	ns	6
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%	—

Notes:

- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (Rx) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns can be added to the associated clock signal.
- For 10 and 100 Mbps, t_{RGT} scales to 400 ns \pm 40 ns and 40 ns \pm 4 ns, respectively.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- Duty cycle reference is $V_{DD}/2$.
- This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
- In rev. 2.0 silicon, due to errata, $t_{SKRGTKHDX}$ minimum is −2.3 ns and $t_{SKRGTKHDV}$ maximum is 1 ns for UCC1, 1.2 ns for UCC2 option 1, and 1.8 ns for UCC2 option 2. In rev. 2.1 silicon, due to errata, $t_{SKRGTKHDX}$ minimum is −0.65 ns for UCC2 option 1 and −0.9 for UCC2 option 2, and $t_{SKRGTKHDV}$ maximum is 0.75 ns for UCC1 and UCC2 option 1 and 0.85 for UCC2 option 2. Refer to Errata QE_ENET10 in *Chip Errata for the MPC8360E, Rev. 1*. UCC1 does meet $t_{SKRGTKHDX}$ minimum for rev. 2.1 silicon.

Table 47. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0.3	—	ns	2, 4, 6

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
- See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
- For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- Input timings are measured at the pin.
- In rev. 2.0 silicon, due to errata, t_{PCIHOV} maximum is 6.6 ns. Refer to Errata PCI21 in *Chip Errata for the MPC8360E, Rev. 1*.
- In rev. 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Refer to Errata PCI17 in *Chip Errata for the MPC8360E, Rev. 1*.

Table 48. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	7.0	—	ns	2, 2
Input hold from clock	t_{PCIXKH}	0.3	—	ns	2, 4, 5

Notes:

- The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS} , reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
- See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
- For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- Input timings are measured at the pin.
- In rev. 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Refer to Errata PCI17 in *Chip Errata for the MPC8360E, Rev. 1*.

This figure provides the AC test load for PCI.

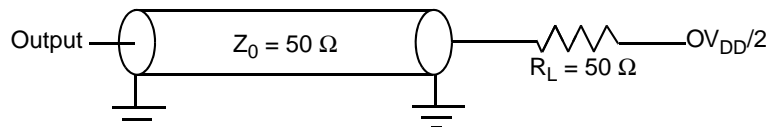


Figure 36. PCI AC Test Load

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC1_MCKE[0:1]	AL32, AU33	O	GV _{DD}	3
MEMC1_MCK[0:1]	AK37, AT37	O	GV _{DD}	—
MEMC1_MCK[2:3]/ MEMC2_MCK[0:1]	AN1, AR2	O	GV _{DD}	—
MEMC1_MCK[4:5]/ MEMC2_MCKE[0:1]	AN25, AK1	O	GV _{DD}	—
MEMC1_MCK[0:1]	AL37, AT36	O	GV _{DD}	—
MEMC1_MCK[2:3]/ MEMC2_MCK[0:1]	AP2, AT2	O	GV _{DD}	—
MEMC1_MCK[4]/ MEMC2_MDM[8]	AN24	O	GV _{DD}	—
MEMC1_MCK[5]/ MEMC2_MDQS[8]	AL1	O	GV _{DD}	—
MDIC[0:1]	AH6, AP30	I/O	GV _{DD}	10
Secondary DDR SDRAM Memory Controller Interface				
MEMC2_MECC[0:7]	AN16, AP18, AM16, AM17, AN17, AP13, AP15, AN13	I/O	GV _{DD}	—
MEMC2_MBA[0:2]	AU12, AU15, AU13	O	GV _{DD}	—
MEMC2_MA[0:14]	AT12, AP11, AT13, AT14, AR13, AR15, AR16, AT16, AT18, AT17, AP10, AR20, AR17, AR14, AR11	O	GV _{DD}	—
MEMC2_MWE	AU10	O	GV _{DD}	—
MEMC2_MRAS	AT11	O	GV _{DD}	—
MEMC2_MCAS	AU11	O	GV _{DD}	—
PCI				
PCI_INTA/IRQ_OUT/CE_PF[5]	A20	I/O	LV _{DD2}	2
PCI_RESET_OUT/CE_PF[6]	E19	I/O	LV _{DD2}	—
PCI_AD[31:30]/CE_PG[31:30]	D20, D21	I/O	LV _{DD2}	—
PCI_AD[29:25]/CE_PG[29:25]	A24, B23, C23, E23, A26	I/O	OV _{DD}	—
PCI_AD[24]/CE_PG[24]	B21	I/O	LV _{DD2}	—
PCI_AD[23:0]/CE_PG[23:0]	C24, C25, D25, B25, E24, F24, A27, A28, F27, A30, C30, D30, E29, B31, C31, D31, D32, A32, C33, B33, F30, E31, A34, D33	I/O	OV _{DD}	—
PCI_C/BE[3:0]/CE_PF[10:7]	E22, B26, E28, F28	I/O	OV _{DD}	—
PCI_PAR/CE_PF[11]	D28	I/O	OV _{DD}	—
PCI_FRAME/CE_PF[12]	D26	I/O	OV _{DD}	5
PCI_TRDY/CE_PF[13]	C27	I/O	OV _{DD}	5
PCI_IRDY/CE_PF[14]	C28	I/O	OV _{DD}	5
PCI_STOP/CE_PF[15]	B28	I/O	OV _{DD}	5

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LCLK[2]/LCS[7]	G37	O	OV _{DD}	—
LSYNC_OUT	F34	O	OV _{DD}	—
LSYNC_IN	G35	I	OV _{DD}	—
Programmable Interrupt Controller				
MCP_OUT	E34	O	OV _{DD}	2
IRQ0/MCP_IN	C37	I	OV _{DD}	—
IRQ[1]/M1SRCID[4]/M2SRCID[4]/LSRCID[4]	F35	I/O	OV _{DD}	—
IRQ[2]/M1DVAL/M2DVAL/LDVAL	F36	I/O	OV _{DD}	—
IRQ[3]/CORE_SRESET	H34	I/O	OV _{DD}	—
IRQ[4:5]	G33, G32	I/O	OV _{DD}	—
IRQ[6]/LCS[6]/CKSTOP_OUT	E35	I/O	OV _{DD}	—
IRQ[7]/LCS[7]/CKSTOP_IN	H36	I/O	OV _{DD}	—
DUART				
UART1_SOUT/M1SRCID[0]/M2SRCID[0]/LSRCID[0]	E32	O	OV _{DD}	—
UART1_SIN/M1SRCID[1]/M2SRCID[1]/LSRCID[1]	B34	I/O	OV _{DD}	—
UART1_CTS/M1SRCID[2]/M2SRCID[2]/LSRCID[2]	C34	I/O	OV _{DD}	—
UART1_RTS/M1SRCID[3]/M2SRCID[3]/LSRCID[3]	A35	O	OV _{DD}	—
I²C Interface				
IIC1_SDA	D34	I/O	OV _{DD}	2
IIC1_SCL	B35	I/O	OV _{DD}	2
IIC2_SDA	E33	I/O	OV _{DD}	2
IIC2_SCL	C35	I/O	OV _{DD}	2
QUICC Engine Block				
CE_PA[0]	F8	I/O	LV _{DD0}	—
CE_PA[1:2]	AH1, AG5	I/O	OV _{DD}	—
CE_PA[3:7]	F6, D4, C3, E5, A3	I/O	LV _{DD0}	—
CE_PA[8]	AG3	I/O	OV _{DD}	—
CE_PA[9:12]	F7, B3, E6, B4	I/O	LV _{DD0}	—
CE_PA[13:14]	AG1, AF6	I/O	OV _{DD}	—
CE_PA[15]	B2	I/O	LV _{DD0}	—
CE_PA[16]	AF4	I/O	OV _{DD}	—
CE_PA[17:21]	B16, A16, E17, A17, B17	I/O	LV _{DD1}	—

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MWE	AT26	O	GV _{DD}	—
MEMC_MRAS	AT29	O	GV _{DD}	—
MEMC_MCAS	AT24	O	GV _{DD}	—
MEMC_MCS[0:3]	AU27, AT27, AU8, AU7	O	GV _{DD}	—
MEMC_MCKE[0:1]	AL32, AU33	O	GV _{DD}	3
MEMC_MCK[0:5]	AK37, AT37, AN1, AR2, AN25, AK1	O	GV _{DD}	—
MEMC_MCK[0:5]	AL37, AT36, AP2, AT2, AN24, AL1	O	GV _{DD}	—
MDIC[0:1]	AH6, AP30	I/O	GV _{DD}	11
PCI				
PCI_INTA/IRQ_OUT/CE_PF[5]	A20	I/O	LV _{DD2}	2
PCI_RESET_OUT/CE_PF[6]	E19	I/O	LV _{DD2}	—
PCI_AD[31:30]/CE_PG[31:30]	D20, D21	I/O	LV _{DD2}	—
PCI_AD[29:25]/CE_PG[29:25]	A24, B23, C23, E23, A26	I/O	OV _{DD}	—
PCI_AD[24]/CE_PG[24]	B21	I/O	LV _{DD2}	—
PCI_AD[23:0]/CE_PG[23:0]	C24, C25, D25, B25, E24, F24, A27, A28, F27, A30, C30, D30, E29, B31, C31, D31, D32, A32, C33, B33, F30, E31, A34, D33	I/O	OV _{DD}	—
PCI_C/BE[3:0]/CE_PF[10:7]	E22, B26, E28, F28	I/O	OV _{DD}	—
PCI_PAR/CE_PF[11]	D28	I/O	OV _{DD}	—
PCI_FRAME/CE_PF[12]	D26	I/O	OV _{DD}	5
PCI_TRDY/CE_PF[13]	C27	I/O	OV _{DD}	5
PCI_IRDY/CE_PF[14]	C28	I/O	OV _{DD}	5
PCI_STOP/CE_PF[15]	B28	I/O	OV _{DD}	5
PCI_DEVSEL/CE_PF[16]	E26	I/O	OV _{DD}	5
PCI_IDSEL/CE_PF[17]	F22	I/O	OV _{DD}	—
PCI_SERR/CE_PF[18]	B29	I/O	OV _{DD}	5
PCI_PERR/CE_PF[19]	A29	I/O	OV _{DD}	5
PCI_REQ[0]/CE_PF[20]	F19	I/O	LV _{DD2}	—
PCI_REQ[1]/CPCI_HS_ES/ CE_PF[21]	A21	I/O	LV _{DD2}	—
PCI_REQ[2]/CE_PF[22]	C21	I/O	LV _{DD2}	—
PCI_GNT[0]/CE_PF[23]	E20	I/O	LV _{DD2}	—
PCI_GNT[1]/CPCI1_HS_LED/ CE_PF[24]	B20	I/O	LV _{DD2}	—
PCI_GNT[2]/CPCI1_HS_ENUM/ CE_PF[25]	C20	I/O	LV _{DD2}	—

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PORESET	L37	I	OV _{DD}	—
HRESET	L36	I/O	OV _{DD}	1
SRESET	M33	I/O	OV _{DD}	2
Thermal Management				
THERM0	AP19	I	GV _{DD}	—
THERM1	AT31	I	GV _{DD}	—
Power and Ground Signals				
AV _{DD} 1	K35	Power for LBIU DLL (1.2 V)	AV _{DD} 1	—
AV _{DD} 2	K36	Power for CE PLL (1.2 V)	AV _{DD} 2	—
AV _{DD} 5	AM29	Power for e300 PLL (1.2 V)	AV _{DD} 5	—
AV _{DD} 6	K37	Power for system PLL (1.2 V)	AV _{DD} 6	—
GND	A2, A8, A13, A19, A22, A25, A31, A33, A36, B7, B12, B24, B27, B30, C4, C6, C9, C15, C26, C32, D3, D8, D11, D14, D17, D19, D23, D27, E7, E13, E25, E30, E36, F4, F37, G34, H1, H5, H32, H33, J4, J32, J37, K1, L3, L5, L33, L34, M1, M34, M35, N37, P2, P5, P35, P36, R4, T3, U1, U5, U35, V37, W1, W4, W33, W36, Y34, AA3, AA5, AC3, AC32, AC35, AD1, AD37, AE4, AE34, AE36, AF33, AG4, AG6, AG32, AH35, AJ1, AJ4, AJ32, AJ35, AJ37, AK36, AL3, AL34, AM4, AN6, AN23, AN30, AP8, AP12, AP14, AP16, AP17, AP20, AP25, AR6, AR8, AR9, AR19, AR24, AR31, AR35, AR37, AT4, AT10, AT19, AT20, AT25, AU14, AU22, AU28, AU35	—	—	—
GV _{DD}	AD4, AE3, AF1, AF5, AF35, AF37, AG2, AG36, AH33, AH34, AK5, AM1, AM35, AM37, AN2, AN10, AN11, AN12, AN14, AN32, AN36, AP5, AP23, AP28, AR1, AR7, AR10, AR12, AR21, AR25, AR27, AR33, AT15, AT22, AT28, AT33, AU2, AU5, AU16, AU31, AU36	Power for DDR DRAM I/O voltage (2.5 or 1.8 V)	GV _{DD}	—
LV _{DD} 0	D5, D6	Power for UCC1 Ethernet interface (2.5 V, 3.3 V)	LV _{DD} 0	—

Table 70. System PLL Multiplication Factors (continued)

RCWL[SPMF]	System PLL Multiplication Factor
1100	× 12
1101	× 13
1110	× 14
1111	× 15

The RCWL[SVCOD] denotes the system PLL VCO internal frequency as shown in this table.

Table 71. System PLL VCO Divider

RCWL[SVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider must be set properly so that the system VCO frequency is in the range of 600–1400 MHz.

The system VCO frequency is derived from the following equations:

- $csb_clk = \{PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)\} \times SPMF$
- System VCO Frequency = $csb_clk \times VCO\ divider$ (if both RCWL[DDRCM] and RCWL[LBCM] are cleared)
OR
- System VCO frequency = $2 \times csb_clk \times VCO\ divider$ (if either RCWL[DDRCM] or RCWL[LBCM] are set).

As described in [Section 21, “Clocking,”](#) the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (csb_clk). This table shows the expected frequency values for the CSB frequency for select csb_clk to CLKIN/PCI_SYNC_IN ratios.

Table 72. CSB Frequency Options

CFG_CLKIN_DIV at Reset ¹	SPMF	csb_clk : Input Clock Ratio ²	Input Clock Frequency (MHz) ²			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2:1				133
Low	0011	3:1				200
Low	0100	4:1				266
Low	0101	5:1				333

21.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). This table shows the encodings for RCWL[COREPLL]. COREPLL values not listed in this table should be considered reserved.

Table 73. e300 Core PLL Configuration

RCWL[COREPLL]			<i>core_clk:csb_clk</i> Ratio	VCO divider
0–1	2–5	6		
nn	0000	n	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)
00	0001	0	1:1	÷2
01	0001	0	1:1	÷4
10	0001	0	1:1	÷8
11	0001	0	1:1	÷8
00	0001	1	1.5:1	÷2
01	0001	1	1.5:1	÷4
10	0001	1	1.5:1	÷8
11	0001	1	1.5:1	÷8
00	0010	0	2:1	÷2
01	0010	0	2:1	÷4
10	0010	0	2:1	÷8
11	0010	0	2:1	÷8
00	0010	1	2.5:1	÷2
01	0010	1	2.5:1	÷4
10	0010	1	2.5:1	÷8
11	0010	1	2.5:1	÷8
00	0011	0	3:1	÷2
01	0011	0	3:1	÷4
10	0011	0	3:1	÷8
11	0011	0	3:1	÷8

NOTE

Core VCO frequency = Core frequency × VCO divider. The VCO divider (RCWL[COREPLL[0:1]]) must be set properly so that the core VCO frequency is in the range of 800–1800 MHz. Having a core frequency below the CSB frequency is not a possible option because the core frequency must be equal to or greater than the CSB frequency.

The QUICC Engine block VCO frequency is derived from the following equations:

$$ce_clk = (\text{primary clock input} \times \text{CEPMF}) \div (1 + \text{CEPDF})$$

$$\text{QE VCO Frequency} = ce_clk \times \text{VCO divider} \times (1 + \text{CEPDF})$$

21.4 Suggested PLL Configurations

To simplify the PLL configurations, the device might be separated into two clock domains. The first domain contains the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the `csb_clk` as its input clock. The second clock domain has the QUICC Engine block PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. This table shows suggested PLL configurations for 33 and 66 MHz input clocks and illustrates each of the clock domains separately. Any combination of clock domains setting with same input clock are valid. Refer to [Section 21, “Clocking,”](#) for the appropriate operating frequencies for your device.

Table 76. Suggested PLL Configurations

Conf No. ¹	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock Freq (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
33 MHz CLKIN/PCI_SYNC_IN Options											
s1	0100	0000100	æ	æ	33	133	266	—	∞	∞	∞
s2	0100	0000101	æ	æ	33	133	333	—	∞	∞	∞
s3	0101	0000100	æ	æ	33	166	333	—	∞	∞	∞
s4	0101	0000101	æ	æ	33	166	416	—	—	∞	∞
s5	0110	0000100	æ	æ	33	200	400	—	∞	∞	∞
s6	0110	0000110	æ	æ	33	200	600	—	—	—	∞
s7	0111	0000011	æ	æ	33	233	350	—	∞	∞	∞
s8	0111	0000100	æ	æ	33	233	466	—	—	∞	∞
s9	0111	0000101	æ	æ	33	233	583	—	—	—	∞
s10	1000	0000011	æ	æ	33	266	400	—	∞	∞	∞
s11	1000	0000100	æ	æ	33	266	533	—	—	∞	∞
s12	1000	0000101	æ	æ	33	266	667	—	—	—	∞
s13	1001	0000010	æ	æ	33	300	300	—	∞	∞	∞
s14	1001	0000011	æ	æ	33	300	450	—	—	∞	∞
s15	1001	0000100	æ	æ	33	300	600	—	—	—	∞
s16	1010	0000010	æ	æ	33	333	333	—	∞	∞	∞
s17	1010	0000011	æ	æ	33	333	500	—	—	∞	∞
s18	1010	0000100	æ	æ	33	333	667	—	—	—	∞
c1	æ	æ	01001	0	33	—	—	300	∞	∞	∞
c2	æ	æ	01100	0	33	—	—	400	∞	∞	∞
c3	æ	æ	01110	0	33	—	—	466	—	∞	∞
c4	æ	æ	01111	0	33	—	—	500	—	∞	∞

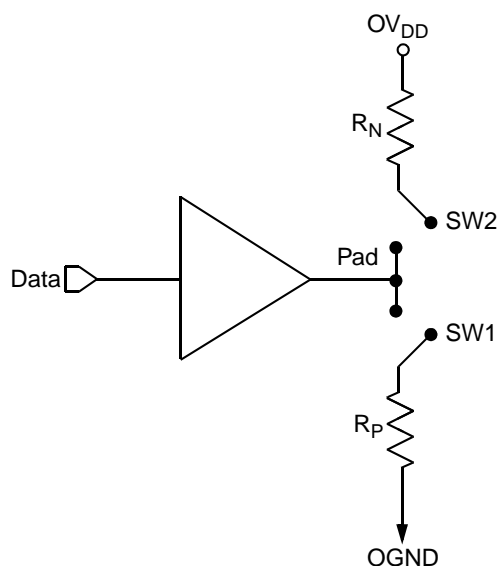


Figure 57. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{\text{source}} \times I_{\text{source}}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term} . The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2) \times I_{\text{source}}$. Solving for the output impedance gives $R_{\text{source}} = R_{\text{term}} \times (V_1/V_2 - 1)$. The drive current is then $I_{\text{source}} = V_1/R_{\text{source}}$.

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD} , nominal OV_{DD} , 105°C.

Table 79. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	20 Target	Z_0	W
R_P	42 Target	25 Target	20 Target	Z_0	W
Differential	NA	NA	NA	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, $T_J = 105^\circ\text{C}$.

23.6 Configuration Pin Muxing

The device provides the user with power-on configuration options that can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.