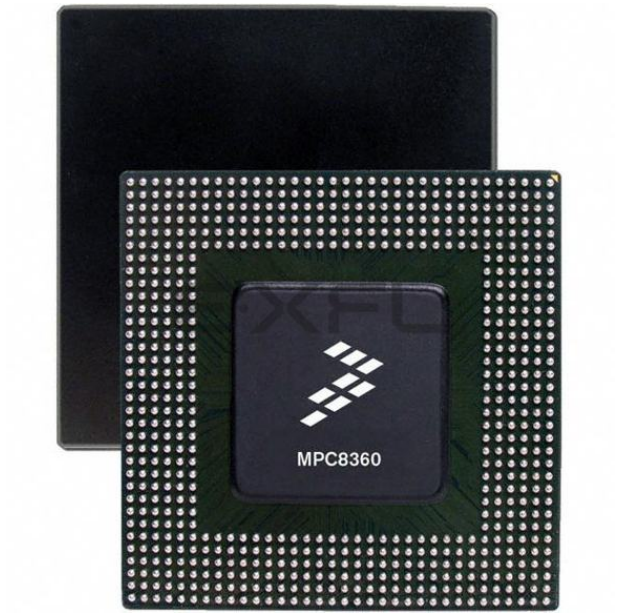

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8360eczuajdg

wide range of protocols including ATM, Ethernet, HDLC, and POS. The QUICC Engine module's enhanced interworking eases the transition and reduces investment costs from ATM to IP based systems. The other major features include a dual DDR SDRAM memory controller for the MPC8360E, which allows equipment providers to partition system parameters and data in an extremely efficient way, such as using one 32-bit DDR memory controller for control plane processing and the other for data plane processing. The MPC8358E has a single DDR SDRAM memory controller. The MPC8360E/58E also offers a 32-bit PCI controller, a flexible local bus, and a dedicated security engine.

This figure shows the MPC8360Eblock diagram.

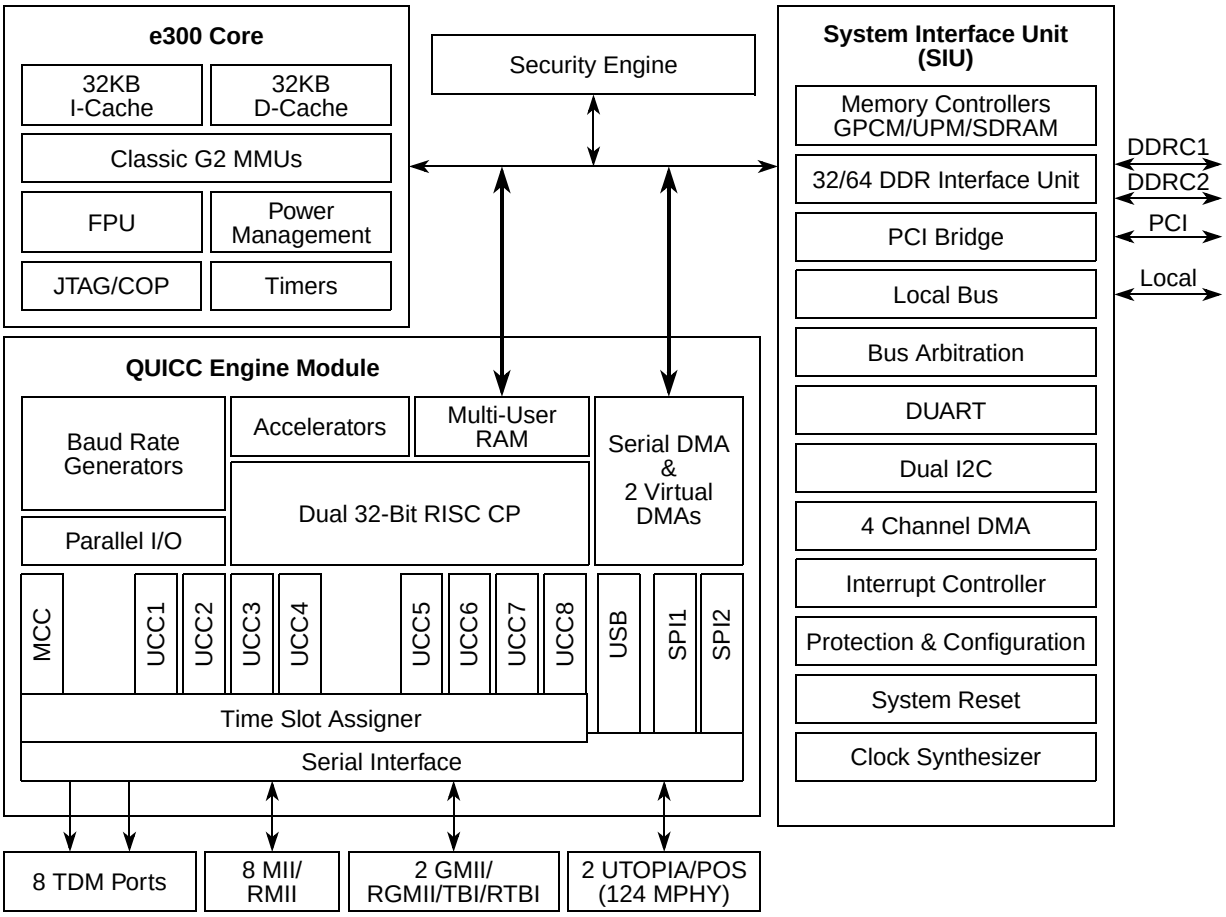


Figure 1. MPC8360E Block Diagram

This figure shows the MPC8358E block diagram.

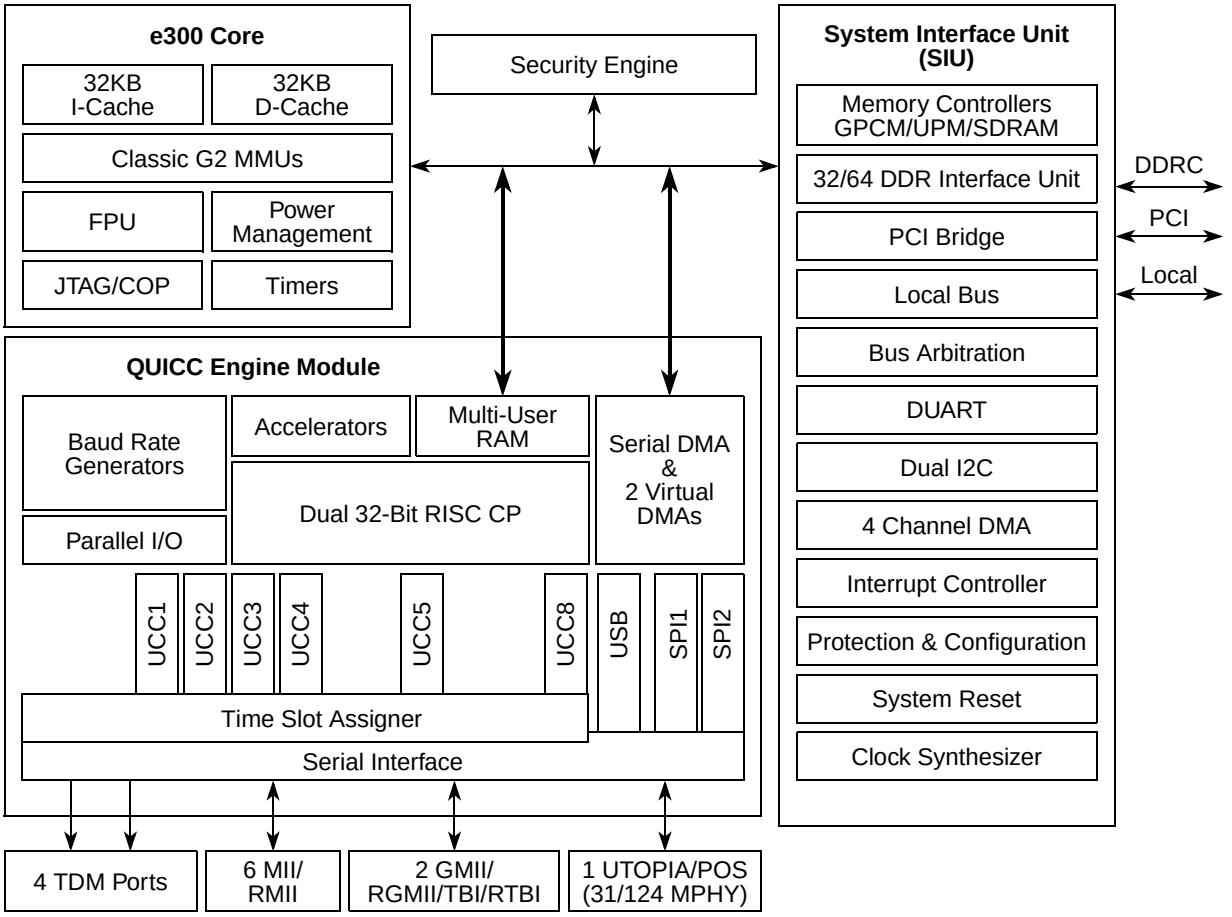


Figure 2. MPC8358E Block Diagram

Major features of the MPC8360E/58E are as follows:

- e300 PowerPC processor core (enhanced version of the MPC603e core)
  - Operates at up to 667 MHz (for the MPC8360E) and 400 MHz (for the MPC8358E)
  - High-performance, superscalar processor core
  - Floating-point, integer, load/store, system register, and branch processing units
  - 32-Kbyte instruction cache, 32-Kbyte data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - Software-compatible with the Freescale processor families implementing the Power Architecture™ technology
- QUICC Engine unit
  - Two 32-bit RISC controllers for flexible support of the communications peripherals, each operating up to 500 MHz (for the MPC8360E) and 400 MHz (for the MPC8358E)
  - Serial DMA channel for receive and transmit on all serial channels
  - QUICC Engine module peripheral request interface (for SEC, PCI, IEEE Std. 1588™)
  - Eight universal communication controllers (UCCs) on the MPC8360E and six UCCs on the MPC8358E supporting the following protocols and interfaces (not all of them simultaneously):
    - IEEE 1588 protocol supported

- 10/100 Mbps Ethernet/IEEE Std. 802.3™ CDMA/CS interface through a media-independent interface (MII, RMII, RGMII)[1]
- 1000 Mbps Ethernet/IEEE 802.3 CDMA/CS interface through a media-independent interface (GMII, RGMII, TBI, RTBI) on UCC1 and UCC2
- 9.6-Kbyte jumbo frames
- ATM full-duplex SAR, up to 622 Mbps (OC-12/STM-4), AAL0, AAL1, and AAL5 in accordance ITU-T I.363.5
- ATM AAL2 CPS, SSSAR, and SSTED up to 155 Mbps (OC-3/STM-1) Mbps full duplex (with 4 CPS packets per cell) in accordance ITU-T I.366.1 and I.363.2
- ATM traffic shaping for CBR, VBR, UBR, and GFR traffic types compatible with ATM forum TM4.1 for up to 64-Kbyte simultaneous ATM channels
- ATM AAL1 structured and unstructured circuit emulation service (CES 2.0) in accordance with ITU-T I.163.1 and ATM Forum af-vtoa-00-0078.000
- IMA (Inverse Multiplexing over ATM) for up to 31 IMA links over 8 IMA groups in accordance with the ATM forum AF-PHY-0086.000 (Version 1.0) and AF-PHY-0086.001 (Version 1.1)
- ATM Transmission Convergence layer support in accordance with ITU-T I.432
- ATM OAM handling features compatible with ITU-T I.610
- PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686, and 3153
- IP support for IPv4 packets including TOS, TTL, and header checksum processing
- Ethernet over first mile IEEE 802.3ah
- Shim header
- Ethernet-to-Ethernet/AAL5/AAL2 inter-working
- L2 Ethernet switching using MAC address or IEEE Std. 802.1P/Q™ VLAN tags
- ATM (AAL2/AAL5) to Ethernet (IP) interworking in accordance with RFC2684 including bridging of ATM ports to Ethernet ports
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- AAL2 protocol rate up to 4 CPS at OC-3/STM-1 rate
- Packet over Sonet (POS) up to 622-Mbps full-duplex 124 MultiPHY
- POS hardware; microcode must be loaded as an IRAM package
- Transparent up to 70-Mbps full-duplex
- HDLC up to 70-Mbps full-duplex
- HDLC BUS up to 10 Mbps
- Asynchronous HDLC
- UART
- BISYNC up to 2 Mbps
- User-programmable Virtual FIFO size
- QUICC multichannel controller (QMC) for 64 TDM channels

— One multichannel communication controller (MCC) only on the MPC8360E supporting the following:
- 256 HDLC or transparent channels
- 128 SS7 channels
- Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces

— Two UTOPIA/POS interfaces on the MPC8360E supporting 124 MultiPHY each (optional 2*128 MultiPHY with extended address) and one UTOPIA/POS interface on the MPC8358E supporting 31/124 MultiPHY

— Two serial peripheral interfaces (SPI); SPI2 is dedicated to Ethernet PHY management

1.SMII or SGMII media-independent interface is not currently supported.

5.2 RESET AC Electrical Characteristics

This section describes the AC electrical specifications for the reset initialization timing requirements of the device. This table provides the reset initialization AC timing specifications for the DDR SDRAM component(s).

Table 11. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$ (input) to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the device is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_SYNC_IN when the device is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$/$\overline{\text{SRESET}}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ negation to $\overline{\text{SRESET}}$ negation (output)	16	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR config signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the device to turn off POR config signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the device to turn on POR config signals with respect to the negation of $\overline{\text{HRESET}}$	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. Refer *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the device is in PCI host mode. Refer *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more details.
3. POR config signals consists of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

This table provides the PLL and DLL lock times.

Table 12. PLL and DLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	µs	—
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.
2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 21, “Clocking,” for more information.

This table provides the input AC timing specifications for the DDR SDRAM interface when GV_{DD}(typ) = 2.5 V.

Table 19. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V	—

Table 20. DDR and DDR2 SDRAM Input AC Timing Specifications Mode

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
MDQS—MDQ/MECC input skew per byte	t_{DISKEW}			ps	1, 2
333 MHz		–750	750		
266 MHz		–1125	1125		
200 MHz		–1250	1250		

Notes:
1. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.
2. Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 ≤n ≤7) or ECC (MECC[{0...7}] if n = 8).

This figure shows the input timing diagram for the DDR controller.

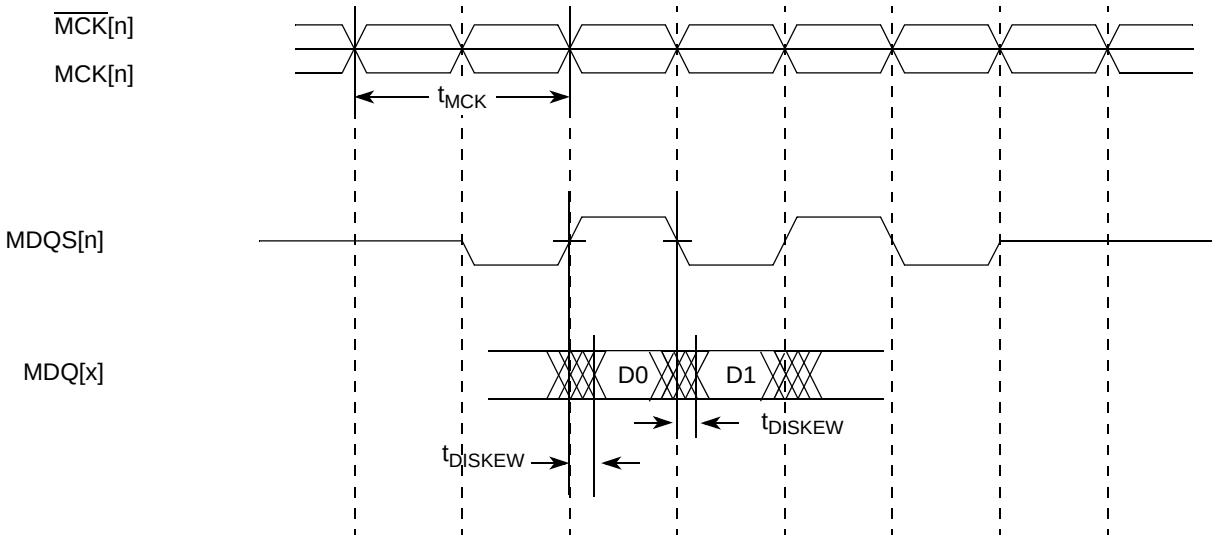


Figure 6. DDR Input Timing Diagram

8.2.4.1 TBI Transmit AC Timing Specifications

This table provides the TBI transmit AC timing specifications.

Table 33. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns	—
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%	—
GTX_CLK to TBI data TCG[9:0] delay	t_{TTKHDX} t_{TTKHDV}	1.0 —	—	— 5.0	ns	3
GTX_CLK clock rise time, (20% to 80%)	t_{TTXR}	—	—	1.0	ns	—
GTX_CLK clock fall time, (80% to 20%)	t_{TTXF}	—	—	1.0	ns	—
GTX_CLK125 reference clock period	t_{G125}	—	8.0	—	ns	2
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	45	—	55	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
3. In rev. 2.0 silicon, due to errata, t_{TTKHDX} minimum is 0.7 ns for UCC1. Refer to Errata *QE_ENET19* in *Chip Errata for the MPC8360E, Rev. 1*.

This figure shows the TBI transmit AC timing diagram.

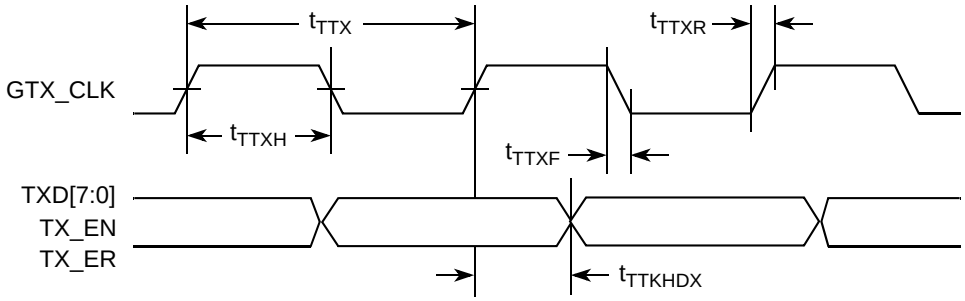


Figure 18. TBI Transmit AC Timing Diagram

Table 41. Local Bus General Timing Parameters—DLL Bypass Mode[9] (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus clock to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	8

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
9. DLL bypass mode is not recommended for use at frequencies above 66 MHz.

This figure provides the AC test load for the local bus.

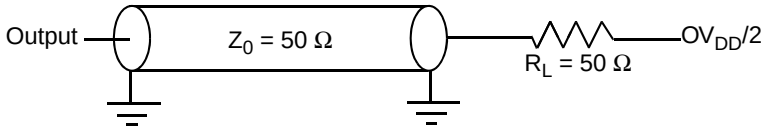


Figure 22. Local Bus C Test Load

This figure provides the AC test load for the I^2C.

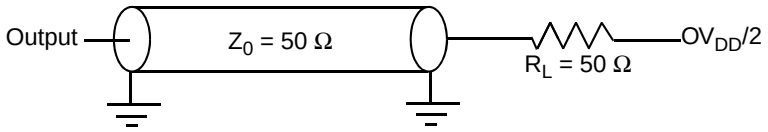


Figure 34. I^2C AC Test Load

This figure shows the AC timing diagram for the I^2C bus.

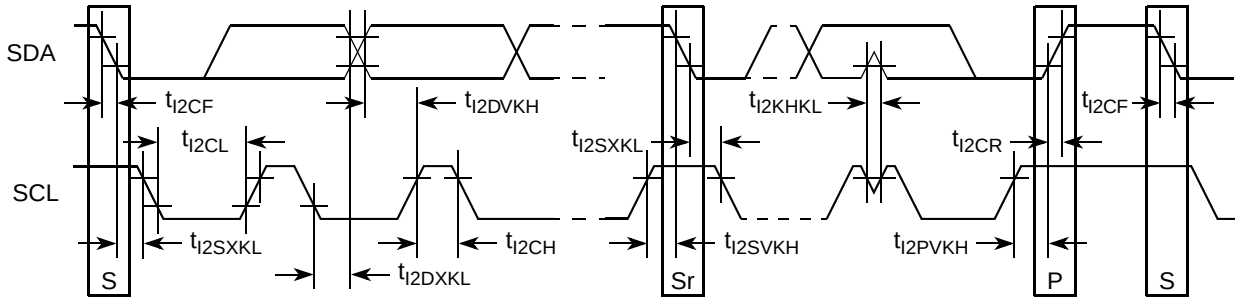


Figure 35. I^2C Bus AC Timing Diagram

12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8360E/58E.

12.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface of the device.

Table 46. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	$0.5 \times OV_{DD}$	$OV_{DD} + 0.5$	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	-0.5	$0.3 \times OV_{DD}$	V
High-level output voltage	V_{OH}	I_{OH} = –500 µA	$0.9 \times OV_{DD}$	—	V
Low-level output voltage	V_{OL}	I_{OL} = 1500 µA	—	$0.1 \times OV_{DD}$	V
Input current	I_{IN}	$0 V \leq V_{IN}$[1] $\leq OV_{DD}$	—	±10	µA

12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the device. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. This table provides the PCI AC timing specifications at 66 MHz.

Table 47. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2, 5
Output hold from clock	t_{PCKHOX}	1	—	ns	2

Table 47. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0.3	—	ns	2, 4, 6

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. In rev. 2.0 silicon, due to errata, t_{PCIHOV} maximum is 6.6 ns. Refer to Errata PCI21 in *Chip Errata for the MPC8360E, Rev. 1*.
6. In rev. 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Refer to Errata PCI17 in *Chip Errata for the MPC8360E, Rev. 1*.

Table 48. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	7.0	—	ns	2, 2
Input hold from clock	t_{PCIXKH}	0.3	—	ns	2, 4, 5

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. In rev. 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Refer to Errata PCI17 in *Chip Errata for the MPC8360E, Rev. 1*.

This figure provides the AC test load for PCI.

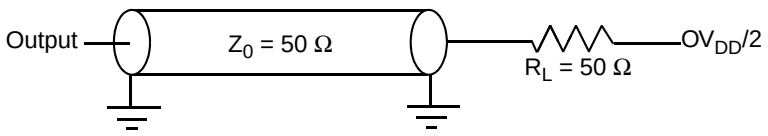


Figure 36. PCI AC Test Load

13.2 Timers AC Timing Specifications

This table provides the timer input and output AC timing specifications.

Table 50. Timers Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Typ	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

This figure provides the AC test load for the timers.

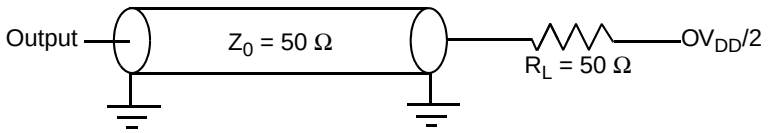


Figure 39. Timers AC Test Load

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8360E/58E.

14.1 GPIO DC Electrical Characteristics

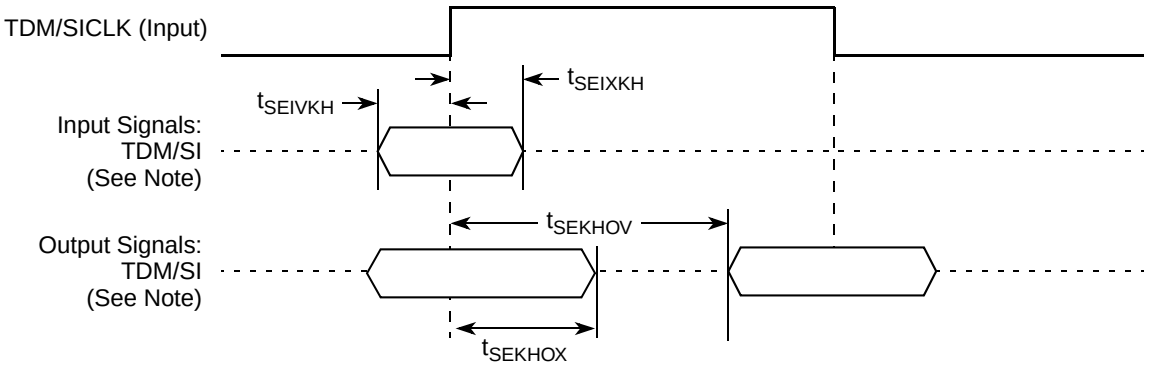
This table provides the DC electrical characteristics for the device GPIO.

Table 51. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	0 V ≤V_{IN} ≤OV_{DD}	—	±10	μA	—

Note:
1. This specification applies when operating from 3.3-V supply.

This figure shows the TDM/SI timing with external clock.



Note: The clock edge is selectable on TDM/SI

Figure 45. TDM/SI AC Timing (External Clock) Diagram

17.3 UTOPIA/POS

This section describes the DC and AC electrical specifications for the UTOPIA/POS of the MPC8360E/58E.

17.4 UTOPIA/POS DC Electrical Characteristics

This table provides the DC electrical characteristics for the device UTOPIA.

Table 59. UTOPIA DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤V_{IN} ≤OV_{DD}	—	±10	μA

17.5 UTOPIA/POS AC Timing Specifications

This table provides the UTOPIA input and output AC timing specifications.

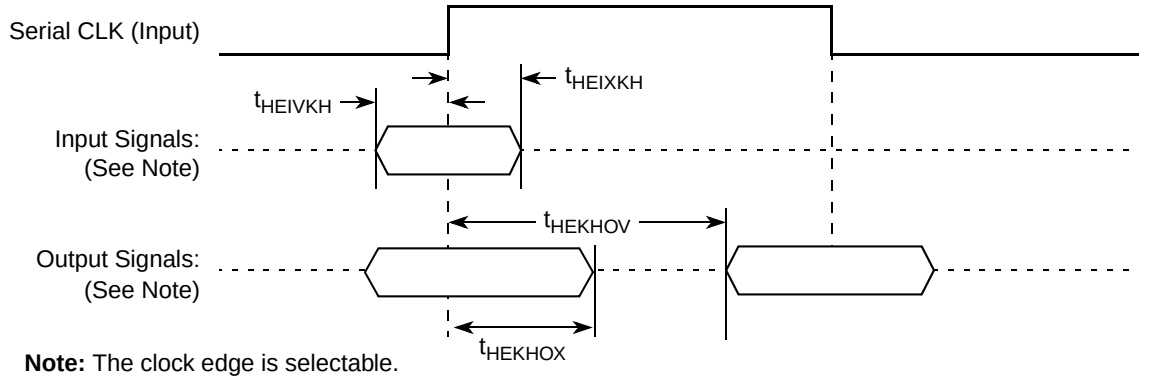
Table 60. UTOPIA AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit	Notes
UTOPIA outputs—Internal clock delay	t_{UIKHOV}	0	11.5	ns	—
UTOPIA outputs—External clock delay	t_{UEKHOV}	1	11.6	ns	—
UTOPIA outputs—Internal clock high impedance	t_{UIKHOX}	0	8.0	ns	—
UTOPIA outputs—External clock high impedance	t_{UEKHOX}	1	10.0	ns	—
UTOPIA inputs—Internal clock input setup time	t_{UIIVKH}	6	—	ns	—
UTOPIA inputs—External clock input setup time	t_{UEIVKH}	4	—	ns	3

18.3 AC Test Load

These figures represent the AC timing from Table 62 and Table 63. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

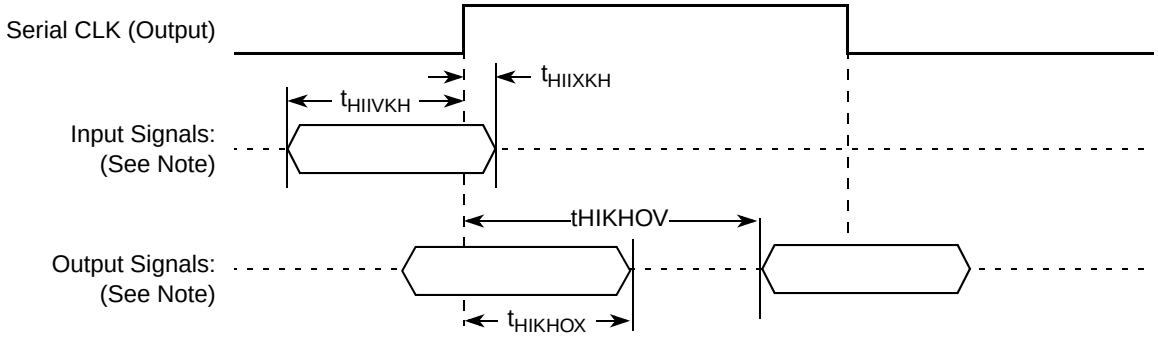
This figure shows the timing with external clock.



Note: The clock edge is selectable.

Figure 50. AC Timing (External Clock) Diagram

This figure shows the timing with internal clock.



Note: The clock edge is selectable.

Figure 51. AC Timing (Internal Clock) Diagram

20 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8360E/58E is available in a tape ball grid array (TBGA), see Section 20.1, “Package Parameters for the TBGA Package,” and Section 20.2, “Mechanical Dimensions of the TBGA Package,” for information on the package.

20.1 Package Parameters for the TBGA Package

The package parameters for rev. 2.0 silicon are as provided in the following list. The package type is 37.5 mm × 37.5 mm, 740 tape ball grid array (TBGA).

Package outline	37.5 mm × 37.5 mm
Interconnects	740
Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder Balls	62 Sn/36 Pb/2 Ag (ZU package) 95.5 Sn/0.5 Cu/4Ag (VV package)
Ball diameter (typical)	0.64 mm

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
No Connect				
NC	AM20, AU19	—	—	—

Notes:
1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. These are On Die Termination pins, used to control DDR2 memories internal termination resistance.
7. This pin must always be tied to GND.
8. This pin must always be left not connected.
9. Refer to *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* section on "RGMII Pins," for information about the two UCC2 Ethernet interface options.
10. It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor for DDR2.

This table shows the pin list of the MPC8358E TBGA package.

Table 67. MPC8358E TBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Controller Interface				
MEMC1_MDQ[0:63]	AJ34, AK33, AL33, AL35, AJ33, AK34, AK32, AM36, AN37, AN35, AR34, AT34, AP37, AP36, AR36, AT35, AP34, AR32, AP32, AM31, AN33, AM34, AM33, AM30, AP31, AM27, AR30, AT32, AN29, AP29, AN27, AR29, AN8, AN7, AM8, AM6, AP9, AN9, AT7, AP7, AU6, AP6, AR4, AR3, AT6, AT5, AR5, AT3, AP4, AM5, AP3, AN3, AN5, AL5, AN4, AM2, AL2, AH5, AK3, AJ2, AJ3, AH4, AK4, AH3	I/O	GV_{DD}	—
MEMC_MECC[0:4]/MSRCID[0:4]	AP24, AN22, AM19, AN19, AM24	I/O	GV_{DD}	—
MEMC_MECC[5]/MDVAL	AM23	I/O	GV_{DD}	—
MEMC_MECC[6:7]	AM22, AN18	I/O	GV_{DD}	—
MEMC_MDM[0:8]	AL36, AN34, AP33, AN28,AT9, AU4, AM3, AJ6,AP27	O	GV_{DD}	—
MEMC_MDQS[0:8]	AK35, AP35, AN31, AM26,AT8, AU3, AL4, AJ5, AP26	I/O	GV_{DD}	—
MEMC_MBA[0:1]	AU29, AU30	O	GV_{DD}	
MEMC_MBA[2]	AT30	O	GV_{DD}	—
MEMC_MA[0:14]	AU21, AP22, AP21, AT21, AU25, AU26, AT23, AR26, AU24, AR23, AR28, AU23, AR22, AU20, AR18	O	GV_{DD}	—
MEMC_MODT[0:3]	AG33, AJ36, AT1, AK2	O	GV_{DD}	6

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{IRQ}}$[4:5]	G33, G32	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[6]/$\overline{\text{LCS}}$[6]/$\overline{\text{CKSTOP\_OUT}}$	E35	I/O	OV_{DD}	—
$\overline{\text{IRQ}}$[7]/$\overline{\text{LCS}}$[7]/$\overline{\text{CKSTOP\_IN}}$	H36	I/O	OV_{DD}	—
DUART				
UART1_SOUT/M1SRCID[0]/ M2SRCID[0]/LSRCID[0]	E32	O	OV_{DD}	—
UART1_SIN/M1SRCID[1]/ M2SRCID[1]/LSRCID[1]	B34	I/O	OV_{DD}	—
$\overline{\text{UART1\_CTS}}$/M1SRCID[2]/ M2SRCID[2]/LSRCID[2]	C34	I/O	OV_{DD}	—
$\overline{\text{UART1\_RTS}}$/M1SRCID[3]/ M2SRCID[3]/LSRCID[3]	A35	O	OV_{DD}	—
I^2C Interface				
IIC1_SDA	D34	I/O	OV_{DD}	2
IIC1_SCL	B35	I/O	OV_{DD}	2
IIC2_SDA	E33	I/O	OV_{DD}	2
IIC2_SCL	C35	I/O	OV_{DD}	2
QUICC Engine				
CE_PA[0]	F8	I/O	LV_{DD0}	—
CE_PA[1:2]	AH1, AG5	I/O	OV_{DD}	—
CE_PA[3:7]	F6, D4, C3, E5, A3	I/O	$LV_{DD}0$	—
CE_PA[8]	AG3	I/O	OV_{DD}	—
CE_PA[9:12]	F7, B3, E6, B4	I/O	$LV_{DD}0$	—
CE_PA[13:14]	AG1, AF6	I/O	OV_{DD}	—
CE_PA[15]	B2	I/O	$LV_{DD}0$	—
CE_PA[16]	AF4	I/O	OV_{DD}	—
CE_PA[17:21]	B16, A16, E17, A17, B17	I/O	$LV_{DD}1$	—
CE_PA[22]	AF3	I/O	OV_{DD}	—
CE_PA[23:26]	C18, D18, E18, A18	I/O	$LV_{DD}1$	—
CE_PA[27:28]	AF2, AE6	I/O	OV_{DD}	—
CE_PA[29]	B19	I/O	$LV_{DD}1$	—
CE_PA[30]	AE5	I/O	OV_{DD}	—
CE_PA[31]	F16	I/O	$LV_{DD}1$	—

This figure shows the internal distribution of clocks within the MPC8358E.

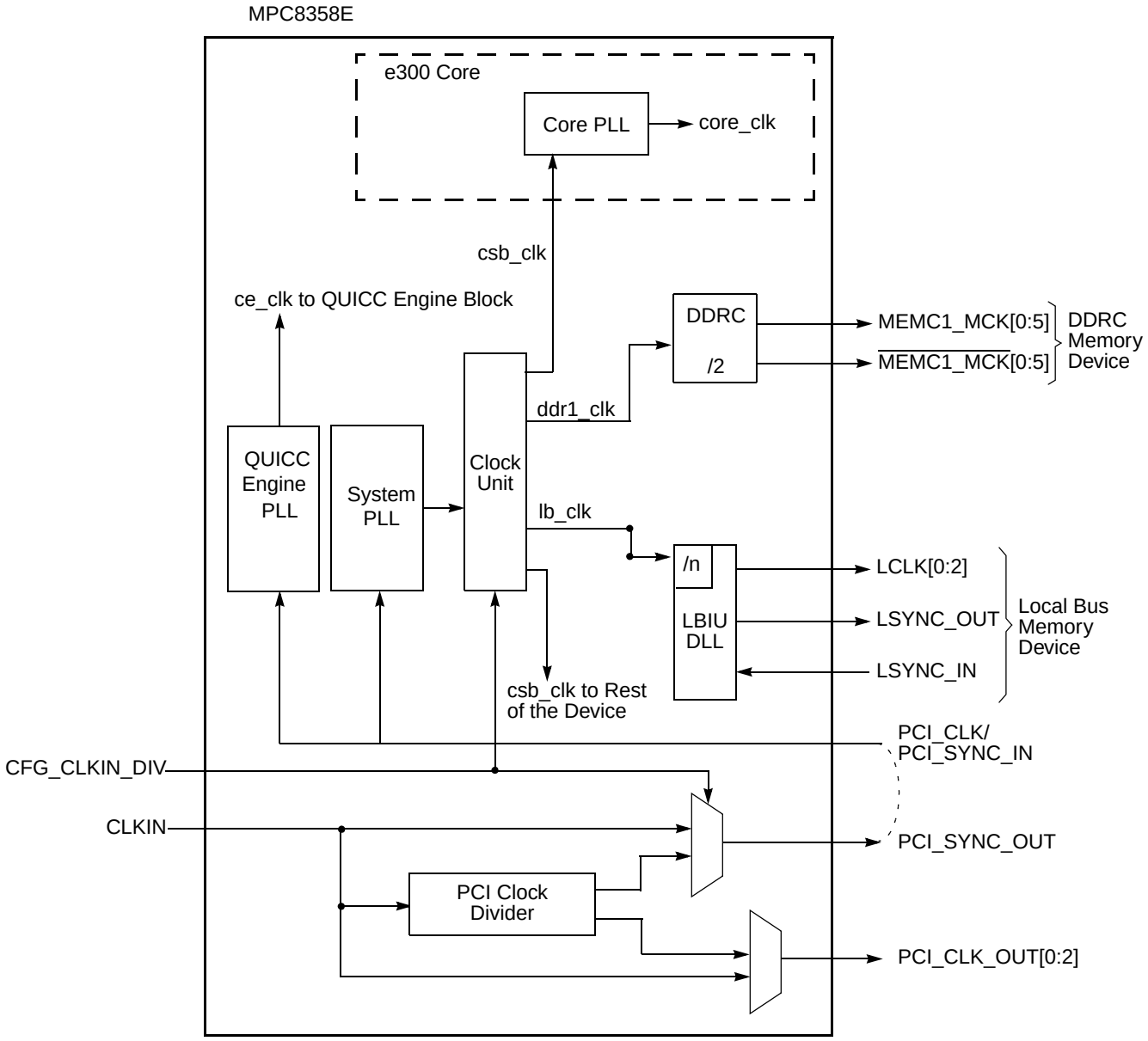


Figure 55. MPC8358E Clock Subsystem

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Note that in PCI host mode, the primary clock input also depends on whether PCI clock outputs are selected with RCWH[PCICKDRV]. When the device is configured as a PCI host device (RCWH[PCIHOST] = 1) and PCI clock output is selected (RCWH[PCICKDRV] = 1), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCIOEN*n*] parameters enable the PCI_CLK_OUT*n*, respectively.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input

The QUICC Engine block VCO frequency is derived from the following equations:

ce_clk = (primary clock input × CEPMF) ÷ (1 + CEPDF)

QE VCO Frequency = *ce_clk* × VCO divider × (1 + CEPDF)

21.4 Suggested PLL Configurations

To simplify the PLL configurations, the device might be separated into two clock domains. The first domain contains the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine block PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. This table shows suggested PLL configurations for 33 and 66 MHz input clocks and illustrates each of the clock domains separately. Any combination of clock domains setting with same input clock are valid. Refer to Section 21, "Clocking," for the appropriate operating frequencies for your device.

Table 76. Suggested PLL Configurations

Conf No.[1]	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock Freq (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
33 MHz CLKIN/PCI_SYNC_IN Options											
s1	**0100**	**0000100**	æ	æ	33	133	266	—	∞	∞	∞
s2	**0100**	**0000101**	æ	æ	33	133	333	—	∞	∞	∞
s3	**0101**	**0000100**	æ	æ	33	166	333	—	∞	∞	∞
s4	**0101**	**0000101**	æ	æ	33	166	416	—	—	∞	∞
s5	**0110**	**0000100**	æ	æ	33	200	400	—	∞	∞	∞
s6	**0110**	**0000110**	æ	æ	33	200	600	—	—	—	∞
s7	**0111**	**0000011**	æ	æ	33	233	350	—	∞	∞	∞
s8	**0111**	**0000100**	æ	æ	33	233	466	—	—	∞	∞
s9	**0111**	**0000101**	æ	æ	33	233	583	—	—	—	∞
s10	**1000**	**0000011**	æ	æ	33	266	400	—	∞	∞	∞
s11	**1000**	**0000100**	æ	æ	33	266	533	—	—	∞	∞
s12	**1000**	**0000101**	æ	æ	33	266	667	—	—	—	∞
s13	**1001**	**0000010**	æ	æ	33	300	300	—	∞	∞	∞
s14	**1001**	**0000011**	æ	æ	33	300	450	—	—	∞	∞
s15	**1001**	**0000100**	æ	æ	33	300	600	—	—	—	∞
s16	**1010**	**0000010**	æ	æ	33	333	333	—	∞	∞	∞
s17	**1010**	**0000011**	æ	æ	33	333	500	—	—	∞	∞
s18	**1010**	**0000100**	æ	æ	33	333	667	—	—	—	∞
c1	æ	æ	**01001**	**0**	33	—	—	300	∞	∞	∞
c2	æ	æ	**01100**	**0**	33	—	—	400	∞	∞	∞
c3	æ	æ	**01110**	**0**	33	—	—	466	—	∞	∞
c4	æ	æ	**01111**	**0**	33	—	—	500	—	∞	∞

Table 76. Suggested PLL Configurations (continued)

Conf No.[1]	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock Freq (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
c5	æ	æ	**10000**	**0**	33	—	—	533	—	∞	∞
c6	æ	æ	**10001**	**0**	33	—	—	566	—	—	∞
66 MHz CLKIN/PCI_SYNC_IN Options											
s1h	**0011**	**0000110**	æ	æ	66	200	400	—	∞	∞	∞
s2h	**0011**	**0000101**	æ	æ	66	200	500	—	—	∞	∞
s3h	**0011**	**0000110**	æ	æ	66	200	600	—	—	—	∞
s4h	**0100**	**0000011**	æ	æ	66	266	400	—	∞	∞	∞
s5h	**0100**	**0000100**	æ	æ	66	266	533	—	—	∞	∞
s6h	**0100**	**0000101**	æ	æ	66	266	667	—	—	—	∞
s7h	**0101**	**0000010**	æ	æ	66	333	333	—	∞	∞	∞
s8h	**0101**	**0000011**	æ	æ	66	333	500	—	—	∞	∞
s9h	**0101**	**0000100**	æ	æ	66	333	667	—	—	—	∞
c1h	æ	æ	**00101**	**0**	66	—	—	333	∞	∞	∞
c2h	æ	æ	**00110**	**0**	66	—	—	400	∞	∞	∞
c3h	æ	æ	**00111**	**0**	66	—	—	466	—	∞	∞
c4h	æ	æ	**01000**	**0**	66	—	—	533	—	∞	∞
c5h	æ	æ	**01001**	**0**	66	—	—	600	—	—	∞

Note:

1. The Conf No. consist of prefix, an index and a postfix. The prefix “s” and “c” stands for “syset” and “ce” respectively. The postfix “h” stands for “high input clock.”"The index is a serial number.

The following steps describe how to use above table. See Example 1.

2. Choose the up or down sections in the table according to input clock rate 33 MHz or 66 MHz.
3. Select a suitable CSB and core clock rates from Table 76. Copy the SPMF and CORE PLL configuration bits.
4. Select a suitable QUICC Engine block clock rate from Table 76. Copy the CEPMF and CEPDF configuration bits.
5. Insert the chosen SPMF, COREPLL, CEPMF and CEPDF to the RCWL fields, respectively.

Example 1. Sample Table Use

Index	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
A	**1000**	**0000011**	**01001**	**0**	33	266	400	300	∞	∞	∞
B	**0100**	**0000100**	**00110**	**0**	66	266	533	400	∞	∞	∞

- **Example A.** To configure the device with CSB clock rate of 266 MHz, core rate of 400 MHz, and QUICC Engine clock rate 300 MHz while the input clock rate is 33 MHz. Conf No. ‘s10’ and ‘c1’ are selected from Table 76. SPMF is 1000, CORPLL is 0000011, CEPMF is 01001, and CEPDF is 0.
- **Example B.** To configure the device with CSBCSB clock rate of 266 MHz, core rate of 533 MHz and QUICC Engine clock rate 400 MHz while the input clock rate is 66 MHz. Conf No. ‘s5h’ and ‘c2h’ are selected from Table 76. SPMF is 0100, CORPLL is 0000100, CEPMF is 00110, and CEPDF is 0.

22 Thermal

This section describes the thermal specifications of the MPC8360E/58E.

22.1 Thermal Characteristics

This table provides the package thermal characteristics for the 37.5 mm × 37.5 mm 740-TBGA package.

Table 77. Package Thermal Characteristics for the TBGA Package

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection on single-layer board (1s)	$R_{\theta JA}$	15	°C/W	1, 2
Junction-to-ambient natural convection on four-layer board (2s2p)	$R_{\theta JA}$	11	°C/W	1, 3
Junction-to-ambient (@1 m/s) on single-layer board (1s)	$R_{\theta JMA}$	10	°C/W	1, 3
Junction-to-ambient (@ 1 m/s) on four-layer board (2s2p)	$R_{\theta JMA}$	8	°C/W	1, 3
Junction-to-ambient (@ 2 m/s) on single-layer board (1s)	$R_{\theta JMA}$	9	°C/W	1, 3
Junction-to-ambient (@ 2 m/s) on four-layer board (2s2p)	$R_{\theta JMA}$	7	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	4.5	°C/W	4
Junction-to-case thermal	$R_{\theta JC}$	1.1	°C/W	5

This figure shows the PLL power supply filter circuit.

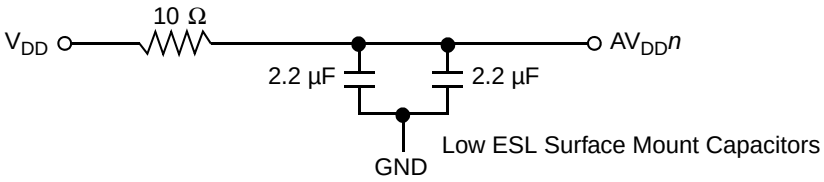


Figure 56. PLL Power Supply Filter Circuit

23.3 Decoupling Recommendations

Due to large address and data buses as well as high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the device system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pins of the device. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

Additionally, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

23.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}, GV_{DD}, or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and GND pins of the device.

23.5 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 57). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.