NXP USA Inc. - MPC8360ECZUAJDGA Datasheet





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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8360eczuajdga

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



- DRAM chip configurations from 64 Mbits to 1 Gigabit with $\times 8/\times 16$ data ports
- Full ECC support (when the MPC8360E is configured as 2×32-bit DDR memory controllers, both support ECC)
- Page mode support (up to 16 simultaneous open pages for DDR1, up to 32 simultaneous open pages for DDR2)
- Contiguous or discontiguous memory mapping
- Read-modify-write support
- Sleep mode support for self refresh SDRAM
- Supports auto refreshing
- Supports source clock mode
- On-the-fly power management using CKE
- Registered DIMM support
- 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
- External driver impedance calibration
- On-die termination (ODT)
- PCI interface
 - PCI Specification Revision 2.3 compatible
 - Data bus widths:
 - Single 32-bit data PCI interface that operates at up to 66 MHz
 - PCI 3.3-V compatible (not 5-V compatible)
 - PCI host bridge capabilities on both interfaces
 - PCI agent mode supported on PCI interface
 - Support for PCI-to-memory and memory-to-PCI streaming
 - Memory prefetching of PCI read accesses and support for delayed read transactions
 - Support for posting of processor-to-PCI and PCI-to-memory writes
 - On-chip arbitration, supporting five masters on PCI
 - Support for accesses to all PCI address spaces
 - Parity support
 - Selectable hardware-enforced coherency
 - Address translation units for address mapping between host and peripheral
 - Dual address cycle supported when the device is the target
 - Internal configuration registers accessible from PCI
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data operating at up to 133 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
 - Three protocol engines available on a per chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user programmable machines (UPMs)
 - Dedicated single data rate SDRAM controller
 - Parity support
 - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
 - Functional and programming compatibility with the MPC8260 interrupt controller
 - Support for 8 external and 35 internal discrete interrupt sources
 - Support for one external (optional) and seven internal machine checkstop interrupt sources

Characteristic	Symbol	Recommended Value	Unit	Notes
PCI, local bus, DUART, system control and power management, I^2C , SPI, and JTAG I/O voltage	OV _{DD}	3.3 V ± 330 mV	V	_
Junction temperature	TJ	0 to 105 -40 to 105	°C	2

Table 2. Recommended Operating Conditions (continued)

Notes:

- 1. GV_{DD}, LV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
- The operating conditions for junction temperature, T_J, on the 600/333/400 MHz and 500/333/500 MHz on rev. 2.0 silicon is 0° to 70 °C. Refer to Errata General9 in *Chip Errata for the MPC8360E, Rev. 1*.
- 3. For more information on Part Numbering, refer to Table 80.

This figure shows the undershoot and overshoot voltages at the interfaces of the device.



1. Note that $t_{\mbox{interface}}$ refers to the clock period associated with the bus clock interface.

Figure 3. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$



Power Sequencing

This figure shows the undershoot and overshoot voltage of the PCI interface of the device for the 3.3-V signals, respectively.



Figure 4. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	OV _{DD} = 3.3 V
PCI signals	25	
PCI output clocks (including PCI_SYNC_OUT)	42	
DDR signal	20 36 (half-strength mode) ¹	GV _{DD} = 2.5 V
DDR2 signal	18 36 (half-strength mode) ¹	GV _{DD} = 1.8 V
10/100/1000 Ethernet signals	42	LV _{DD} = 2.5/3.3 V
DUART, system control, I ² C, SPI, JTAG	42	OV _{DD} = 3.3 V
GPIO signals	42	OV _{DD} = 3.3 V LV _{DD} = 2.5/3.3 V

Note:

1. DDR output impedance values for half strength mode are verified by design and not tested.

2.2 Power Sequencing

This section details the power sequencing considerations for the MPC8360E/58E.





Table 4. MPC8360E TBGA Core Power Dissipation ¹	(continued)
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Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
667	333	500	6.1	6.8	W	2, 3, 5, 9

Notes:

- 1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 6.
- 2. Typical power is based on a voltage of V_{DD} = 1.2 V or 1.3 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.
- 3. Thermal solutions need to design to a value higher than typical power on the end application, T_A target, and I/O power.
- 4. Maximum power is based on a voltage of V_{DD} = 1.2 V, WC process, a junction T_J = 105°C, and an artificial smoke test.
- Maximum power is based on a voltage of V_{DD} = 1.3 V for applications that use 667 MHz (CPU)/500 (QE) with WC process, a junction T₁ = 105° C, and an artificial smoke test.
- 6. Typical power is based on a voltage of V_{DD} = 1.3 V, a junction temperature of T_J = 70° C, and a Dhrystone benchmark application.
- Maximum power is based on a voltage of V_{DD} = 1.3 V for applications that use 667 MHz (CPU) or 500 (QE) with WC process, a junction T_J = 70° C, and an artificial smoke test.
- 8. This frequency combination is only available for rev. 2.0 silicon.
- 9. This frequency combination is not available for rev. 2.0 silicon.

Table 5. MPC8358E TBGA Core Power Dissipation¹

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	300	4.1	4.5	W	2, 3, 4
400	266	400	4.5	5.0	W	2, 3, 4

Notes:

- 1. The values do not include I/O supply power (OV_{DD}, LV_{DD} , GV_{DD}) or AV_{DD} . For I/O power values, see Table 6.
- Typical power is based on a voltage of V_{DD} = 1.2 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.
- 3. Thermal solutions need to design to a value higher than typical power on the end application, T_A target, and I/O power.
- 4. Maximum power is based on a voltage of V_{DD} = 1.2 V, WC process, a junction T_J = 105°C, and an artificial smoke test.



RESET DC Electrical Characteristics

Table 9. GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV (continued)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
GTX_CLK rise and fall time $\label{eq:VDD} \begin{array}{l} \text{LV}_{\text{DD}} = 2.5 \text{ V} \\ \text{LV}_{\text{DD}} = 3.3 \text{ V} \end{array}$	t _{G125R} /t _{G125F}	—	_	0.75 1.0	ns	1
GTX_CLK125 duty cycle GMII & TBI 1000Base-T for RGMII & RTBI	t _{G125H} /t _{G125}	45 47	—	55 53	%	2
GTX_CLK125 jitter	—	—	—	±150	ps	2

Notes:

- 1. Rise and fall times for GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
- GTX_CLK125 is used to generate the GTX clock for the UCC Ethernet transmitter with 2% degradation. The GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by GTX_CLK. See Section 8.2.2, "MII AC Timing Specifications," Section 8.2.3, "RMII AC Timing Specifications," and Section 8.2.5, "RGMII and RTBI AC Timing Specifications" for the duty cycle for 10Base-T and 100Base-T reference clock.

5 **RESET Initialization**

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8360E/58E.

5.1 **RESET DC Electrical Characteristics**

This table provides the DC electrical characteristics for the RESET pins of the device.

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V _{IH}	_	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	_	-0.3	0.8	V
Input current	I _{IN}	_	_	±10	μA
Output high voltage	V _{OH} ²	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V

Table 10. RESET Pins DC Electrical Characteristics ¹

Notes:

1. This table applies for pins PORESET, HRESET, SRESET, and QUIESCE.

2. HRESET and SRESET are open drain pins, thus V_{OH} is not relevant for those pins.





This section describes the DC and AC electrical specifications for the DUART interface of the MPC8360E/58E.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface of the device.

Table 23. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit	Notes
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V	—
Low-level input voltage OV _{DD}	V _{IL}	-0.3	0.8	V	—
High-level output voltage, I _{OH} = −100 μA	V _{OH}	OV _{DD} - 0.4	—	V	—
Low-level output voltage, I _{OL} = 100 μA	V _{OL}	—	0.2	V	—
Input current (0 V ≰⁄ _{IN} ≤OV _{DD})	I _{IN}	—	±10	μA	1

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface of the device.

Table 24.	DUART	AC T	iming	Speci	ifications
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Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	_
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	_	2

Notes:

- 1. Actual attainable baud rate is limited by the latency of interrupt processing.
- 2. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

8 UCC Ethernet Controller: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

8.1 Three-Speed Ethernet Controller (10/100/1000 Mbps)— GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), MII (media independent interface), RMII (reduced media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The MII, RMII, GMII, and TBI interfaces are only defined for 3.3 V, while the RGMII and RTBI interfaces are only defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet



8.2.1.1 GMII Transmit AC Timing Specifications

This table provides the GMII transmit AC timing specifications.

Table 27. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
GTX_CLK clock period	t _{GTX}	_	8.0		ns	_
GTX_CLK duty cycle	t _{GTXH/tGTX}	40	_	60	%	—
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	^t GTKHDX ^t GTKHDV	0.5	_	 5.0	ns	3
GTX_CLK clock rise time, (20% to 80%)	t _{GTXR}	_		1.0	ns	_
GTX_CLK clock fall time, (80% to 20%)	t _{GTXF}	_	_	1.0	ns	—
GTX_CLK125 clock period	t _{G125}	_	8.0	_	ns	2
GTX_CLK125 reference clock duty cycle measured at $LV_{DD/2}$	t _{G125H} /t _{G125}	45		55	%	2

Notes:

- 1. The symbols used for timing specifications follow the pattern t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{ignx} clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- 2. This symbol is used to represent the external GTX_CLK125 signal and does not follow the original symbol naming convention.
- In rev. 2.0 silicon, due to errata, t_{GTKHDX} minimum and t_{GTKHDV} maximum are not supported when the GTX_CLK is selected. Refer to Errata QE_ENET18 in Chip Errata for the MPC8360E, Rev. 1.

This figure shows the GMII transmit AC timing diagram.



Figure 10. GMII Transmit AC Timing Diagram



8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.2.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 29. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TX_CLK clock period 10 Mbps	t _{MTX}		400		ns
TX_CLK clock period 100 Mbps	t _{MTX}	_	40	_	ns
TX_CLK duty cycle	t _{MTXH} /t _{MTX}	35	_	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t _{MTKHDX} t _{MTKHDV}	1	5	 15	ns
TX_CLK data clock rise time, (20% to 80%)	t _{MTXR}	1.0	_	4.0	ns
TX_CLK data clock fall time, (80% to 20%)	t _{MTXF}	1.0		4.0	ns

Note:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub></sub>

This figure shows the MII transmit AC timing diagram.



Figure 12. MII Transmit AC Timing Diagram



GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

8.2.2.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 30. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
RX_CLK clock period 10 Mbps	t _{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t _{MRX}	—	40	—	ns
RX_CLK duty cycle	t _{MRXH} /t _{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t _{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t _{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise time, (20% to 80%)	t _{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time, (80% to 20%)	t _{MRXF}	1.0	—	4.0	ns

Note:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

This figure provides the AC test load.





This figure shows the MII receive AC timing diagram.



Figure 14. MII Receive AC Timing Diagram



Parameter	Symbol ¹	Min	Max	Unit	Notes
LUPWAIT input hold from local bus clock	t _{LBIXKH2}	1.0	_	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT1}	1.5	_	ns	5
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT2}	3.0	_	ns	6
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT3}	2.5	_	ns	7
Local bus clock to LALE rise	t _{LBKHLR}	_	4.5	ns	
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}	_	4.5	ns	
Local bus clock to data valid for LAD/LDP	t _{LBKHOV2}	_	4.5	ns	3
Local bus clock to address valid for LAD	t _{LBKHOV3}	_	4.5	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	1.0	_	ns	3
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	1.0	_	ns	3
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ}		3.8	ns	8

Table 40. Local Bus General Timing Parameters—DLL Enabled (continued)

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the output (O) going invalid (X) or output hold time.
 </sub>
- 2. All timings are in reference to rising edge of LSYNC_IN.
- 3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. t_{LBOTOT1} should be used when RCWH[LALE] is not set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- t_{LBOTOT2} should be used when RCWH[LALE] is set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- 7. t_{LBOTOT3} should be used when RCWH[LALE] is set and when the load on LALE output pin equals to the load on LAD output pins.
- 8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This table describes the general timing parameters of the local bus interface of the device.

Table 41. Local Bus General Timing Parameters—DLL Bypass Mode⁹

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	15	—	ns	2
Input setup to local bus clock	t _{LBIVKH}	7	—	ns	3, 4
Input hold from local bus clock	t _{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT1}	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT2}	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT3}	2.5	_	ns	7

Local Bus AC Electrical Specifications

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to output valid	t _{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ}		4	ns	8

Table 41. Local Bus General Timing Parameters—DLL Bypass Mode⁹ (continued)

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the to the output (O) going invalid (X) or output hold time.
 </sub>
- 2. All timings are in reference to falling edge of LCLK0 (for all outputs and for LGTA and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
- 3. All signals are measured from OV_{DD}/2 of the rising/falling edge of LCLK0 to 0.4 × OV_{DD} of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. t_{LBOTOT1} should be used when RCWH[LALE] is not set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- t_{LBOTOT2} should be used when RCWH[LALE] is set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- 7. t_{LBOTOT3} should be used when RCWH[LALE] is set and when the load on LALE output pin equals to the load on LAD output pins.
- 8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 9. DLL bypass mode is not recommended for use at frequencies above 66 MHz.

This figure provides the AC test load for the local bus.



Figure 22. Local Bus C Test Load



Local Bus AC Electrical Specifications



Figure 25. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Enabled)





I2C AC Electrical Specifications

11.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interface of the device.

Table 45. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 44).

Parameter	Symbol ¹	Min	Max	Unit	Note
SCL clock frequency	f _{I2C}	0	400	kHz	2
Low period of the SCL clock	t _{I2CL}	1.3	_	μs	—
High period of the SCL clock	t _{I2CH}	0.6	_	μs	—
Setup time for a repeated START condition	t _{I2SVKH}	0.6	_	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL}	0.6	_	μs	_
Data setup time	t _{I2DVKH}	100	_	ns	3
Data hold time: CBUS compatible masters I ² C bus devices	t _{I2DXKL}	$\frac{1}{0^2}$	 0.9 ³	μs	—
Rise time of both SDA and SCL signals	t _{I2CR}	20 + 0.1 C _b ⁴	300	ns	—
Fall time of both SDA and SCL signals	t _{I2CF}	20 + 0.1 C _b ⁴	300	ns	—
Set-up time for STOP condition	t _{l2PVKH}	0.6	_	μs	—
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	_	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times \text{OV}_{\text{DD}}$	_	V	_
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times \text{OV}_{\text{DD}}$	_	V	_

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional}

block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

 The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of the falling edge of SCL.

3. The maximum t_{12DVKH} has only to be met if the device does not stretch the LOW period (t_{12CL}) of the SCL signal.

4. C_B = capacitance of one bus line in pF.



This figure provides the AC test load for the I^2C .



Figure 34. I²C AC Test Load

This figure shows the AC timing diagram for the I^2C bus.



12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8360E/58E.

12.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface of the device.

Table 46. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Мах	Unit
High-level input voltage	V _{IH}	$V_{OUT} \ge V_{OH}$ (min) or	$0.5\times\text{OV}_\text{DD}$	OV _{DD} + 0.5	V
Low-level input voltage	V _{IL}	V _{OUT} ≤V _{OL} (max)	-0.5	$0.3 imes OV_{DD}$	V
High-level output voltage	V _{OH}	I _{OH} = -500 μA	$0.9 imes OV_{DD}$	—	V
Low-level output voltage	V _{OL}	l _{OL} = 1500 μA	—	$0.1 imes OV_{DD}$	V
Input current	I _{IN}	0 V ≤V _{IN} ¹ ≤OV _{DD}	—	±10	μA

12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the device. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. This table provides the PCI AC timing specifications at 66 MHz.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Clock to output valid	t _{PCKHOV}	_	6.0	ns	2, 5
Output hold from clock	t _{PCKHOX}	1	—	ns	2

Table 47. PCI AC Timing Specifications at 66 MHz



HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

This figure shows the UTOPIA timing with internal clock.





18 HDLC, BISYNC, Transparent, and Synchronous UART

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent, and synchronous UART protocols of the MPC8360E/58E.

18.1 HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

This table provides the DC electrical characteristics for the device HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 61. HDLC, BISYNC,	Transparent, and Synchronous UART DC Electrical Characteristics
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Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V _{OH}	I _{OH} = -2.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.5	V
Input high voltage	V _{IH}	_	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	_	-0.3	0.8	V
Input current	I _{IN}	0 V ≤V _{IN} ≤OV _{DD}	—	±10	μA

18.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

These tables provide the input and output AC timing specifications for HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 62. HDLC, BISYNC, and Transparent AC Timing Specifications¹

Characteristic	Symbol ²	Min	Мах	Unit
Outputs—Internal clock delay	t _{HIKHOV}	0	11.2	ns
Outputs—External clock delay	t _{HEKHOV}	1	10.8	ns



Mechanical Dimensions of the TBGA Package

20.2 Mechanical Dimensions of the TBGA Package

This figure depicts the mechanical dimensions and bottom surface nomenclature of the device, 740-TBGA package.



Figure 53. Mechanical Dimensions and Bottom Surface Nomenclature of the TBGA Package



Pinout Listings

21 Clocking

This figure shows the internal distribution of clocks within the MPC8360E.



Figure 54. MPC8360E Clock Subsystem



System PLL Configuration

			Input Clock Frequency (MHz) ²			
CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	16.67	25	33.33	66.67
				csb_clk Freq	uency (MHz)	
Low	0110	6:1	100	150	200	
Low	0111	7:1	116	175	233	
Low	1000	8:1	133	200	266	
Low	1001	9:1	150	225	300	
Low	1010	10:1	166	250	333	
Low	1011	11:1	183	275		
Low	1100	12:1	200	300		
Low	1101	13:1	216	325		
Low	1110	14:1	233			
Low	1111	15:1	250			
Low	0000	16:1	266			
High	0010	2:1		-		133
High	0011	3:1			100	200
High	0100	4:1			133	266
High	0101	5:1			166	333
High	0110	6:1			200	
High	0111	7:1			233	
High	1000	8:1				
High	1001	9:1				
High	1010	10:1				
High	1011	11:1				
High	1100	12:1				
High	1101	13:1				
High	1110	14:1				
High	1111	15:1				
High	0000	16:1				

Table 72. CSB Frequency Options (continued)

¹ CFG_CLKIN_DIV is only used for host mode; CLKIN must be tied low and CFG_CLKIN_DIV must be pulled down (low) in agent mode.

 $^2\,$ CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

Part Numbers Fully Addressed by this Document

Device	Package	SVR (Rev. 2.0)	SVR (Rev. 2.1)
MPC8358E	TBGA	0x804A_0020	0x804A_0021
MPC8358	TBGA	0x804B_0020	0x804B_0021

25 Document Revision History

This table provides a revision history for this document.

Table 82. Revision History

Rev. Number	Date	Substantive Change(s)
5	09/2011	 Section 2.2.1, "Power-Up Sequencing", added the current limitation "3A to 5A" for the excessive current. Section 2.1.2, "Power Supply Voltage Specification, Updated the Characteristic for TBGA (MPC8358 & MPC8360 Device) with specific frequency for Core and PLL voltages. Added table footnote 3 to Table 2. Applied table footnotes 1 and 2 to Table 10. Removed table footnotes from Table 19. Applied table footnotes 8 and 9 to Table 40. Applied table footnotes 2 and 3 to Table 41. Applied table footnotes from Table 46. Applied table footnote to last three rows of Table 65.
4	01/2011	 Updated references to the LCRR register throughout Removed references to DDR DLL mode in Section 6.2.2, "DDR and DDR2 SDRAM Output AC Timing Specifications." Changed "Junction-to-Case" to "Junction-to-Ambient" in Section 22.2.4, "Heat Sinks and Junction-to-Ambient Thermal Resistance," and Table 78, "Heat Sinks and Junction-to-Ambient Thermal Resistance of TBGA Package," titles.



Table 82.	Revision	History	(continued)
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Rev. Number	Date	Substantive Change(s)
3	03/2010	 Changed references to RCWH[PCICKEN] to RCWH[PCICKDRV]. In Table 2, added extended temperature characteristics. Added Figure 6, "DDR Input Timing Diagram." In Figure 53, "Mechanical Dimensions and Bottom Surface Nomenclature of the TBGA Package," removed watermark. Updated the title of Table 19,"DDR SDRAM Input AC Timing Specifications." In Table 20, "DDR and DDR2 SDRAM Input AC Timing Specifications Mode," changed table subtitle. In Table 20, "DDR and DDR2 SDRAM Input AC Timing Specifications Mode," changed table subtitle. In Table 27–Table 30, and Table 33—Table 34, changed the rise and fall time specifications to reference 20–80% and 80–20% of the voltage supply, respectively. In Table 38, "IEEE 1588 Timer AC Specifications," changed units to "ns" for t_{I2DVKH}. In Table 45, "I2C AC Electrical Specifications," changed units to "ns" for t_{I2DVKH}. In Table 66, "MPC8360E TBGA Pinout Listing," and Table 67 "MPC8358E TBGA Pinout Listing, added note 7: "This pin must always be tied to GND" to the TEST pin and added a note to SPARE1 stating: "This pin must always be left not connected." In Section 4, "Clock Input Timing," added note regarding rise/fall time on QUICC Engine block input pins. Added Section 4.1, "injol/100/1000 Ethernet DC Electrical Characteristics." In Section 2.1, "Pinout Listing," added sentence stating "Refer to AN3097, 'MPC8360/MPC8358E PowerQUICC Design Checklist,' for proper pin termination and usage." In Section 21, "Clocking," removed statement: "The OCCR[PCICDn] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUTn signals." In Section 21.1, "System PLL Configuration," updated the system VCO frequency conditions. In Table 80, added extended temperature characteristics.
2	12/2007	Initial release.