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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8360evvahfh

- Eight TDM interfaces on the MPC8360E and four TDM interfaces on the MPC8358E with 1-bit mode for E3/T3 rates in clear channel
- Sixteen independent baud rate generators and 30 input clock pins for supplying clocks to UCC and MCC serial channels (MCC is only available on the MPC8360E)
- Four independent 16-bit timers that can be interconnected as four 32-bit timers
- Interworking functionality:
 - Layer 2 10/100-Base T Ethernet switch
 - ATM-to-ATM switching (AAL0, 2, 5)
 - Ethernet-to-ATM switching with L3/L4 support
 - PPP interworking
- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, 802.11i®, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs).
 - Public key execution unit (PKEU) supporting the following:
 - RSA and Diffie-Hellman
 - Programmable field size up to 2048 bits
 - Elliptic curve cryptography
 - F2m and F(p) modes
 - Programmable field size up to 511 bits
 - Data encryption standard execution unit (DEU)
 - DES, 3DES
 - Two key (K1, K2) or three key (K1, K2, K3)
 - ECB and CBC modes for both DES and 3DES
 - Advanced encryption standard unit (AESU)
 - Implements the Rijndael symmetric key cipher
 - Key lengths of 128, 192, and 256 bits, two key
 - ECB, CBC, CCM, and counter modes
 - ARC four execution unit (AFEU)
 - Implements a stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
 - Message digest execution unit (MDEU)
 - SHA with 160-, 224-, or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either SHA or MD5 algorithm
 - Random number generator (RNG)
 - Four crypto-channels, each supporting multi-command descriptor chains
 - Static and/or dynamic assignment of crypto-execution units via an integrated controller
 - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
 - Storage/NAS XOR parity generation accelerator for RAID applications
- Dual DDR SDRAM memory controllers on the MPC8360E and a single DDR SDRAM memory controller on the MPC8358E
 - Programmable timing supporting both DDR1 and DDR2 SDRAM
 - On the MPC8360E, the DDR buses can be configured as two 32-bit buses or one 64-bit bus; on the MPC8358E, the DDR bus can be configured as a 32- or 64-bit bus
 - 32- or 64-bit data interface, up to 333 MHz (for the MPC8360E) and 266 MHz (for the MPC8358E) data rate
 - Four banks of memory, each up to 1 Gbyte

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings¹

Characteristic		Symbol	Max Value	Unit	Notes
Core and PLL supply voltage for MPC8358 Device Part Number with Processor Frequency label of AD=266MHz and AG=400MHz & QUICC Engine Frequency label of E=300MHz & G=400MHz MPC8360 Device Part Number with Processor Frequency label of AG=400MHz and AJ=533MHz & QUICC Engine Frequency label of G=400MHz		V_{DD} & AV_{DD}	−0.3 to 1.32	V	—
Core and PLL supply voltage for MPC8360 device Part Number with Processor Frequency label of AL=667MHz and QUICC Engine Frequency label of H=500MHz		V_{DD} & AV_{DD}	−0.3 to 1.37	V	—
DDR and DDR2 DRAM I/O voltage	DDR DDR2	GV_{DD}	−0.3 to 2.75 −0.3 to 1.89	V	—
Three-speed Ethernet I/O, MII management voltage		LV_{DD}	−0.3 to 3.63	V	—
PCI, local bus, DUART, system control and power management, I ² C, SPI, and JTAG I/O voltage		OV_{DD}	−0.3 to 3.63	V	—
Input voltage	DDR DRAM signals	MV_{IN}	−0.3 to ($GV_{DD} + 0.3$)	V	2, 5
	DDR DRAM reference	MV_{REF}	−0.3 to ($GV_{DD} + 0.3$)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	−0.3 to ($LV_{DD} + 0.3$)	V	4, 5
	Local bus, DUART, CLKIN, system control and power management, I ² C, SPI, and JTAG signals	OV_{IN}	−0.3 to ($OV_{DD} + 0.3$)	V	3, 5
	PCI	OV_{IN}	−0.3 to ($OV_{DD} + 0.3$)	V	6

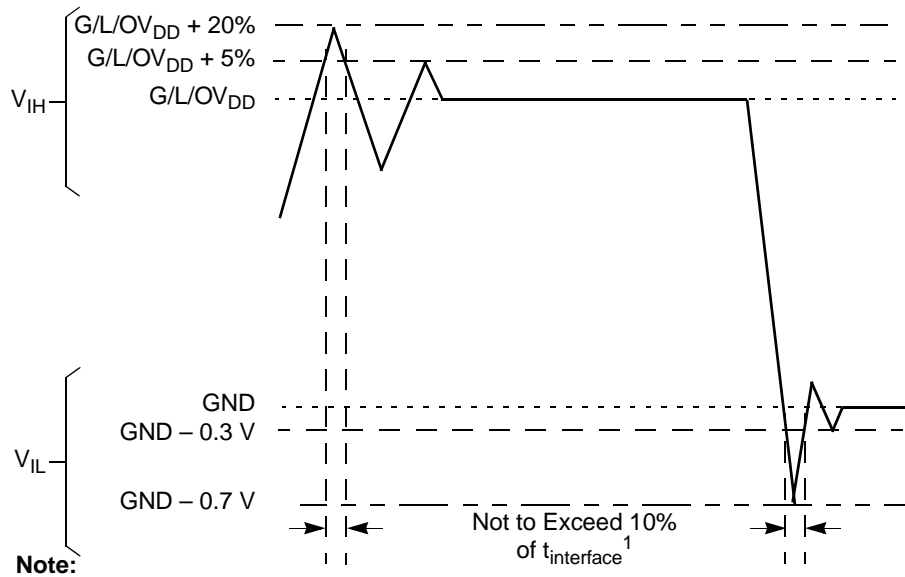
Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value	Unit	Notes
PCI, local bus, DUART, system control and power management, I ² C, SPI, and JTAG I/O voltage	OV _{DD}	3.3 V ± 330 mV	V	—
Junction temperature	T _J	0 to 105 –40 to 105	°C	2

Notes:

1. GV_{DD}, LV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. The operating conditions for junction temperature, T_J, on the 600/333/400 MHz and 500/333/500 MHz on rev. 2.0 silicon is 0° to 70 °C. Refer to Errata General9 in *Chip Errata for the MPC8360E, Rev. 1*.
3. For more information on Part Numbering, refer to [Table 80](#).

This figure shows the undershoot and overshoot voltages at the interfaces of the device.


Figure 3. Overshoot/Undershoot Voltage for GV_{DD}/OV_{DD}/LV_{DD}

2.2.1 Power-Up Sequencing

MPC8360E/58E does not require the core supply voltage (V_{DD} and AV_{DD}) and I/O supply voltages (GV_{DD} , LV_{DD} , and OV_{DD}) to be applied in any particular order. During the power ramp up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there may be a period of time that all input and output pins are actively be driven and cause contention and excessive current from 3A to 5A. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD} , LV_{DD} , and OV_{DD}) and assert **PORESET** before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V, see this figure.

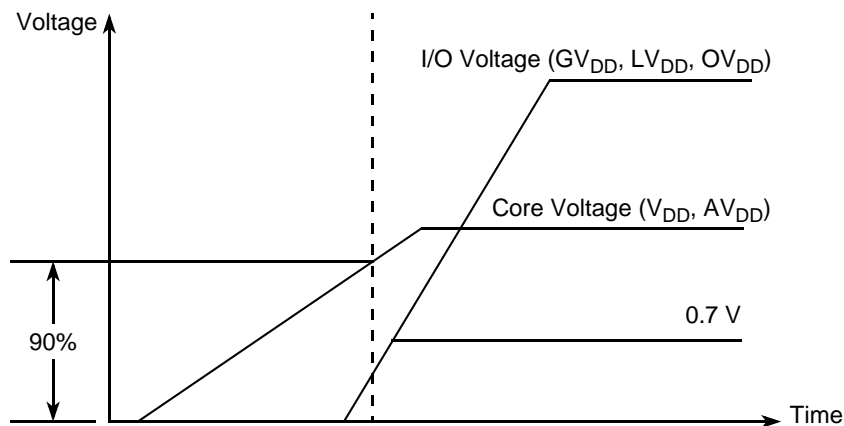


Figure 5. Power Sequencing Example

I/O voltage supplies (GV_{DD} , LV_{DD} , and OV_{DD}) do not have any ordering requirements with respect to one another.

2.2.2 Power-Down Sequencing

The MPC8360E/58E does not require the core supply voltage and I/O supply voltages to be powered down in any particular order.

3 Power Characteristics

The estimated typical power dissipation values are shown in these tables.

Table 4. MPC8360E TBGA Core Power Dissipation¹

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	500	5.0	5.6	W	2, 3, 5
400	266	400	4.5	5.0	W	2, 3, 4
533	266	400	4.8	5.3	W	2, 3, 4
667	333	400	5.8	6.3	W	3, 6, 7, 8
500	333	500	5.9	6.4	W	3, 6, 7, 8

Table 9. GTX_CLK125 AC Timing Specifications

At recommended operating conditions with $LV_{DD} = 2.5 \pm 0.125 \text{ mV}$ / $3.3 \text{ V} \pm 165 \text{ mV}$ (continued)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
GTX_CLK rise and fall time $LV_{DD} = 2.5 \text{ V}$ $LV_{DD} = 3.3 \text{ V}$	t_{G125R}/t_{G125F}	—	—	0.75 1.0	ns	1
GTX_CLK125 duty cycle GMII & TBI 1000Base-T for RGMII & RTBI	t_{G125H}/t_{G125}	45 47	—	55 53	%	2
GTX_CLK125 jitter	—	—	—	± 150	ps	2

Notes:

1. Rise and fall times for GTX_CLK125 are measured from 0.5 and 2.0 V for $LV_{DD} = 2.5 \text{ V}$ and from 0.6 and 2.7 V for $LV_{DD} = 3.3 \text{ V}$.
2. GTX_CLK125 is used to generate the GTX clock for the UCC Ethernet transmitter with 2% degradation. The GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by GTX_CLK. See [Section 8.2.2, “MII AC Timing Specifications,”](#) [Section 8.2.3, “RMII AC Timing Specifications,”](#) and [Section 8.2.5, “RGMII and RTBI AC Timing Specifications”](#) for the duty cycle for 10Base-T and 100Base-T reference clock.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8360E/58E.

5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins of the device.

Table 10. RESET Pins DC Electrical Characteristics ¹

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	−0.3	0.8	V
Input current	I_{IN}	—	—	± 10	μA
Output high voltage	V_{OH} ²	$I_{OH} = -8.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V

Notes:

1. This table applies for pins $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, and $\overline{\text{QUIESCE}}$.
2. $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

This table provides the input AC timing specifications for the DDR SDRAM interface when $GV_{DD}(typ) = 2.5\text{ V}$.

Table 19. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of $2.5\text{ V} \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.31$	V	—
AC input high voltage	V_{IH}	$MV_{REF} + 0.31$	—	V	—

Table 20. DDR and DDR2 SDRAM Input AC Timing Specifications Mode

At recommended operating conditions with GV_{DD} of $(1.8\text{ or }2.5\text{ V}) \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
MDQS—MDQ/MECC input skew per byte 333 MHz 266 MHz 200 MHz	t_{DISKEW}	−750 −1125 −1250	750 1125 1250	ps	1, 2

Notes:

1. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.
2. Maximum possible skew between a data strobe ($MDQS[n]$) and any corresponding bit of data ($MDQ[8n + \{0...7\}]$ if $0 \leq n \leq 7$) or ECC ($MECC[\{0...7\}]$ if $n = 8$).

This figure shows the input timing diagram for the DDR controller.

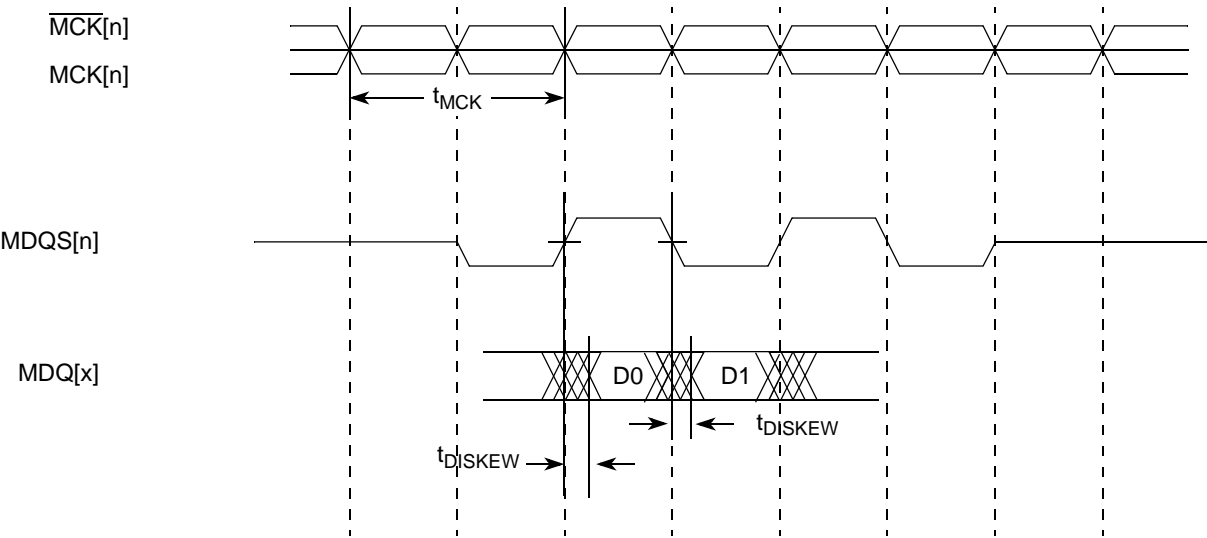


Figure 6. DDR Input Timing Diagram

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8360E/58E.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface of the device.

Table 23. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V	—
Low-level input voltage OV_{DD}	V_{IL}	-0.3	0.8	V	—
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.4$	—	V	—
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V	—
Input current ($0 V \leq V_{IN} \leq OV_{DD}$)	I_{IN}	—	± 10	μA	1

Note:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface of the device.

Table 24. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	—
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	—	2

Notes:

- Actual attainable baud rate is limited by the latency of interrupt processing.
- The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

8 UCC Ethernet Controller: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

8.1 Three-Speed Ethernet Controller (10/100/1000 Mbps)—GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), MII (media independent interface), RMII (reduced media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The MII, RMII, GMII, and TBI interfaces are only defined for 3.3 V, while the RGMII and RTBI interfaces are only defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet

Table 32. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	t_{RMRDVKH}	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	t_{RMRDXKH}	2.0	—	—	ns
REF_CLK clock rise time	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time	t_{RMXF}	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{RMRDVKH} symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, t_{RMRDXKL} symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load.

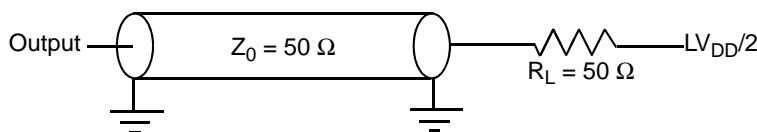


Figure 16. AC Test Load

This figure shows the RMII receive AC timing diagram.

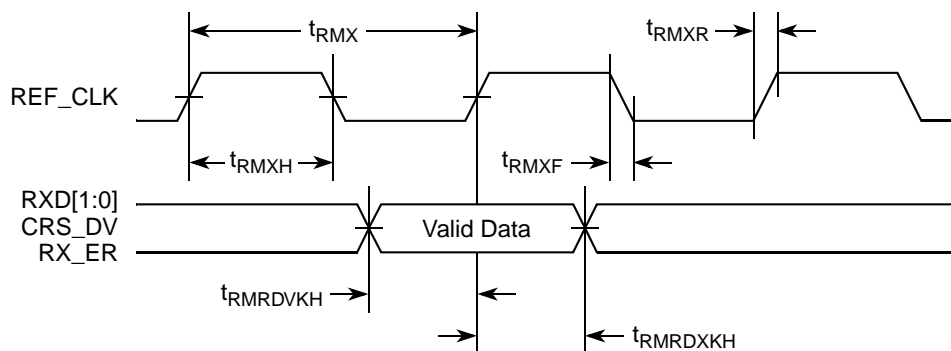


Figure 17. RMII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.5 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 35. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with V_{DD} of 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	$t_{SKRGTKHDX}$ $t_{SKRGTKHDV}$	−0.5 —	—	— 0.5	ns	7
Data to clock input skew (at receiver)	$t_{SKRGDXKH}$ $t_{SKRGDVKH}$	1.0 —	—	— 2.6	ns	2
Clock cycle duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	t_{RGTH}/t_{RGT}	45	50	55	%	4, 5
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 5
Rise time (20–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20–80%)	t_{RGTF}	—	—	0.75	ns	—
GTX_CLK125 reference clock period	t_{G125}	—	8.0	—	ns	6
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%	—

Notes:

- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (Rx) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns can be added to the associated clock signal.
- For 10 and 100 Mbps, t_{RGT} scales to 400 ns \pm 40 ns and 40 ns \pm 4 ns, respectively.
- Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- Duty cycle reference is $V_{DD}/2$.
- This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
- In rev. 2.0 silicon, due to errata, $t_{SKRGTKHDX}$ minimum is −2.3 ns and $t_{SKRGTKHDV}$ maximum is 1 ns for UCC1, 1.2 ns for UCC2 option 1, and 1.8 ns for UCC2 option 2. In rev. 2.1 silicon, due to errata, $t_{SKRGTKHDX}$ minimum is −0.65 ns for UCC2 option 1 and −0.9 for UCC2 option 2, and $t_{SKRGTKHDV}$ maximum is 0.75 ns for UCC1 and UCC2 option 1 and 0.85 for UCC2 option 2. Refer to Errata QE_ENET10 in *Chip Errata for the MPC8360E, Rev. 1*. UCC1 does meet $t_{SKRGTKHDX}$ minimum for rev. 2.1 silicon.

This figure provides the test access port timing diagram.

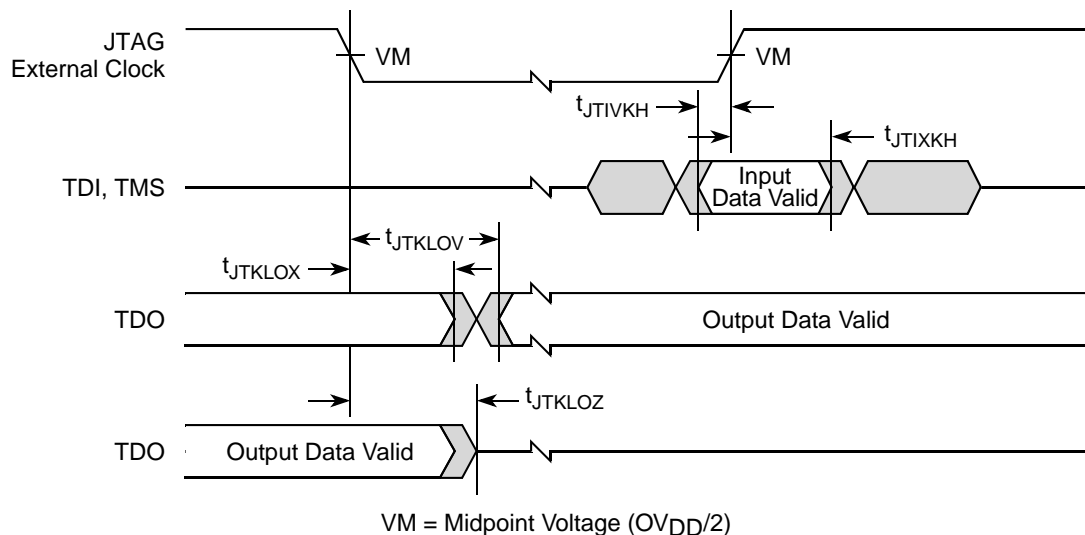


Figure 33. Test Access Port Timing Diagram

11 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8360E/58E.

11.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I²C interface of the device.

Table 44. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	-0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	0.4	V	1
Output fall time from $V_{IH}(\text{min})$ to $V_{IL}(\text{max})$ with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current ($0\text{ V} \leq V_{IN} \leq OV_{DD}$)	I_{IN}	—	± 10	μA	4

Notes:

- Output voltage (open drain or open collector) condition = 3 mA sink current.
- C_B = capacitance of one bus line in pF.
- Refer to the *MPC8360E Integrated Communications Processor Reference Manual* for information on the digital filter used.
- I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

11.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interface of the device.

Table 45. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 44).

Parameter	Symbol ¹	Min	Max	Unit	Note
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXXL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	3
Data hold time: CBUS compatible masters I ² C bus devices	t_{I2DXKL}	— 0 ²	— 0.9 ³	μs	—
Rise time of both SDA and SCL signals	t_{I2CR}	$20 + 0.1 C_B^4$	300	ns	—
Fall time of both SDA and SCL signals	t_{I2CF}	$20 + 0.1 C_B^4$	300	ns	—
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V	—

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXXL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- The maximum t_{I2DVKH} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- C_B = capacitance of one bus line in pF.

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_DEVSEL/CE_PF[16]	E26	I/O	OV _{DD}	5
PCI_IDSEL/CE_PF[17]	F22	I/O	OV _{DD}	—
PCI_SERR/CE_PF[18]	B29	I/O	OV _{DD}	5
PCI_PERR/CE_PF[19]	A29	I/O	OV _{DD}	5
PCI_REQ[0]/CE_PF[20]	F19	I/O	LV _{DD2}	—
PCI_REQ[1]/CPCI_HS_ES/ CE_PF[21]	A21	I/O	LV _{DD2}	—
PCI_REQ[2]/CE_PF[22]	C21	I/O	LV _{DD2}	—
PCI_GNT[0]/CE_PF[23]	E20	I/O	LV _{DD2}	—
PCI_GNT[1]/CPCI1_HS_LED/ CE_PF[24]	B20	I/O	LV _{DD2}	—
PCI_GNT[2]/CPCI1_HS_ENUM/ CE_PF[25]	C20	I/O	LV _{DD2}	—
PCI_MODE	D36	I	OV _{DD}	—
M66EN/CE_PF[4]	B37	I/O	OV _{DD}	—
Local Bus Controller Interface				
LAD[0:31]	N32, N33, N35, N36, P37, P32, P34, R36, R35, R34, R33, T37, T35, T34, T33, U37, T32, U36, U34, V36, V35, W37, W35, V33, V32, W34, Y36, W32, AA37, Y33, AA35, AA34	I/O	OV _{DD}	—
LDP[0]/CKSTOP_OUT	AB37	I/O	OV _{DD}	—
LDP[1]/CKSTOP_IN	AB36	I/O	OV _{DD}	—
LDP[2]/LCS[6]	AB35	I/O	OV _{DD}	—
LDP[3]/LCS[7]	AA33	I/O	OV _{DD}	—
LA[27:31]	AC37, AA32, AC36, AC34, AD36	O	OV _{DD}	—
LCS[0:5]	AD33, AG37, AF34, AE33, AD32, AH37	O	OV _{DD}	—
LWE[0:3]/LSDDQM[0:3]/LBS[0:3]	AG35, AG34, AH36, AE32	O	OV _{DD}	—
LBCTL	AD35	O	OV _{DD}	—
LALE	M37	O	OV _{DD}	—
LGPL0/LSDA10/cfg_reset_source0	AB32	I/O	OV _{DD}	—
LGPL1/LSDWE/cfg_reset_source1	AE37	I/O	OV _{DD}	—
LGPL2/LSDRAS/LOE	AC33	O	OV _{DD}	—
LGPL3/LSDCAS/cfg_reset_source2	AD34	I/O	OV _{DD}	—
LGPL4/LGTA/LUPWAIT/LPBSE	AE35	I/O	OV _{DD}	—
LGPL5/cfg_clkin_div	AF36	I/O	OV _{DD}	—
LCKE	G36	O	OV _{DD}	—
LCLK[0]	J33	O	OV _{DD}	—
LCLK[1]/LCS[6]	J34	O	OV _{DD}	—

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PMC				
$\overline{\text{QUIESCE}}$	B36	O	OV_{DD}	—
System Control				
$\overline{\text{PORESET}}$	L37	I	OV_{DD}	—
$\overline{\text{HRESET}}$	L36	I/O	OV_{DD}	1
$\overline{\text{SRESET}}$	M33	I/O	OV_{DD}	2
Thermal Management				
THERM0	AP19	I	GV_{DD}	—
THERM1	AT31	I	GV_{DD}	—
Power and Ground Signals				
$\text{AV}_{\text{DD}1}$	K35	Power for LBIU DLL (1.2 V)	$\text{AV}_{\text{DD}1}$	—
$\text{AV}_{\text{DD}2}$	K36	Power for CE PLL (1.2 V)	$\text{AV}_{\text{DD}2}$	—
$\text{AV}_{\text{DD}5}$	AM29	Power for e300 PLL (1.2 V)	$\text{AV}_{\text{DD}5}$	—
$\text{AV}_{\text{DD}6}$	K37	Power for system PLL (1.2 V)	$\text{AV}_{\text{DD}6}$	—
GND	A2, A8, A13, A19, A22, A25, A31, A33, A36, B7, B12, B24, B27, B30, C4, C6, C9, C15, C26, C32, D3, D8, D11, D14, D17, D19, D23, D27, E7, E13, E25, E30, E36, F4, F37, G34, H1, H5, H32, H33, J4, J32, J37, K1, L3, L5, L33, L34, M1, M34, M35, N37, P2, P5, P35, P36, R4, T3, U1, U5, U35, V37, W1, W4, W33, W36, Y34, AA3, AA5, AC3, AC32, AC35, AD1, AD37, AE4, AE34, AE36, AF33, AG4, AG6, AG32, AH35, AJ1, AJ4, AJ32, AJ35, AJ37, AK36, AL3, AL34, AM4, AN6, AN23, AN30, AP8, AP12, AP14, AP16, AP17, AP20, AP25, AR6, AR8, AR9, AR19, AR24, AR31, AR35, AR37, AT4, AT10, AT19, AT20, AT25, AU14, AU22, AU28, AU35	—	—	—
GV_{DD}	AD4, AE3, AF1, AF5, AF35, AF37, AG2, AG36, AH33, AH34, AK5, AM1, AM35, AM37, AN2, AN10, AN11, AN12, AN14, AN32, AN36, AP5, AP23, AP28, AR1, AR7, AR10, AR12, AR21, AR25, AR27, AR33, AT15, AT22, AT28, AT33, AU2, AU5, AU16, AU31, AU36	Power for DDR DRAM I/O voltage (2.5 or 1.8 V)	GV_{DD}	—

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
No Connect				
NC	AM20, AU19	—	—	—

Notes:

1. This pin is an open drain signal. A weak pull-up resistor (1 k Ω) should be placed on this pin to OV_{DD}.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 k Ω) should be placed on this pin to OV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. These are On Die Termination pins, used to control DDR2 memories internal termination resistance.
7. This pin must always be tied to GND.
8. This pin must always be left not connected.
9. Refer to *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* section on “RGMII Pins,” for information about the two UCC2 Ethernet interface options.
10. It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor for DDR2.

This table shows the pin list of the MPC8358E TBGA package.

Table 67. MPC8358E TBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Controller Interface				
MEMC1_MDQ[0:63]	AJ34, AK33, AL33, AL35, AJ33, AK34, AK32, AM36, AN37, AN35, AR34, AT34, AP37, AP36, AR36, AT35, AP34, AR32, AP32, AM31, AN33, AM34, AM33, AM30, AP31, AM27, AR30, AT32, AN29, AP29, AN27, AR29, AN8, AN7, AM8, AM6, AP9, AN9, AT7, AP7, AU6, AP6, AR4, AR3, AT6, AT5, AR5, AT3, AP4, AM5, AP3, AN3, AN5, AL5, AN4, AM2, AL2, AH5, AK3, AJ2, AJ3, AH4, AK4, AH3	I/O	GV _{DD}	—
MEMC_MECC[0:4]/MSRCID[0:4]	AP24, AN22, AM19, AN19, AM24	I/O	GV _{DD}	—
MEMC_MECC[5]/MDVAL	AM23	I/O	GV _{DD}	—
MEMC_MECC[6:7]	AM22, AN18	I/O	GV _{DD}	—
MEMC_MDM[0:8]	AL36, AN34, AP33, AN28, AT9, AU4, AM3, AJ6, AP27	O	GV _{DD}	—
MEMC_MDQS[0:8]	AK35, AP35, AN31, AM26, AT8, AU3, AL4, AJ5, AP26	I/O	GV _{DD}	—
MEMC_MBA[0:1]	AU29, AU30	O	GV _{DD}	—
MEMC_MBA[2]	AT30	O	GV _{DD}	—
MEMC_MA[0:14]	AU21, AP22, AP21, AT21, AU25, AU26, AT23, AR26, AU24, AR23, AR28, AU23, AR22, AU20, AR18	O	GV _{DD}	—
MEMC_MODT[0:3]	AG33, AJ36, AT1, AK2	O	GV _{DD}	6

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{IRQ}}[4:5]$	G33, G32	I/O	OV_{DD}	—
$\overline{\text{IRQ}}[6]/\overline{\text{LCS}}[6]/\overline{\text{CKSTOP_OUT}}$	E35	I/O	OV_{DD}	—
$\overline{\text{IRQ}}[7]/\overline{\text{LCS}}[7]/\overline{\text{CKSTOP_IN}}$	H36	I/O	OV_{DD}	—
DUART				
UART1_SOUT/M1SRCID[0]/M2SRCID[0]/LSRCID[0]	E32	O	OV_{DD}	—
UART1_SIN/M1SRCID[1]/M2SRCID[1]/LSRCID[1]	B34	I/O	OV_{DD}	—
$\overline{\text{UART1_CTS}}$ /M1SRCID[2]/M2SRCID[2]/LSRCID[2]	C34	I/O	OV_{DD}	—
$\overline{\text{UART1_RTS}}$ /M1SRCID[3]/M2SRCID[3]/LSRCID[3]	A35	O	OV_{DD}	—
I²C Interface				
IIC1_SDA	D34	I/O	OV_{DD}	2
IIC1_SCL	B35	I/O	OV_{DD}	2
IIC2_SDA	E33	I/O	OV_{DD}	2
IIC2_SCL	C35	I/O	OV_{DD}	2
QUICC Engine				
CE_PA[0]	F8	I/O	LV_{DD0}	—
CE_PA[1:2]	AH1, AG5	I/O	OV_{DD}	—
CE_PA[3:7]	F6, D4, C3, E5, A3	I/O	LV_{DD0}	—
CE_PA[8]	AG3	I/O	OV_{DD}	—
CE_PA[9:12]	F7, B3, E6, B4	I/O	LV_{DD0}	—
CE_PA[13:14]	AG1, AF6	I/O	OV_{DD}	—
CE_PA[15]	B2	I/O	LV_{DD0}	—
CE_PA[16]	AF4	I/O	OV_{DD}	—
CE_PA[17:21]	B16, A16, E17, A17, B17	I/O	LV_{DD1}	—
CE_PA[22]	AF3	I/O	OV_{DD}	—
CE_PA[23:26]	C18, D18, E18, A18	I/O	LV_{DD1}	—
CE_PA[27:28]	AF2, AE6	I/O	OV_{DD}	—
CE_PA[29]	B19	I/O	LV_{DD1}	—
CE_PA[30]	AE5	I/O	OV_{DD}	—
CE_PA[31]	F16	I/O	LV_{DD1}	—

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
CE_PB[0:27]	AE2, AE1, AD5, AD3, AD2, AC6, AC5, AC4, AC2, AC1, AB5, AB4, AB3, AB1, AA6, AA4, AA2, Y6, Y4, Y3, Y2, Y1, W6, W5, W2, V5, V3, V2	I/O	OV _{DD}	—
CE_PC[0:1]	V1, U6	I/O	OV _{DD}	
CE_PC[2:3]	C16, A15	I/O	LV _{DD} 1	—
CE_PC[4:6]	U4, U3, T6	I/O	OV _{DD}	—
CE_PC[7]	C19	I/O	LV _{DD} 2	—
CE_PC[8:9]	A4, C5	I/O	LV _{DD} 0	—
CE_PC[10:30]	T5, T4, T2, T1, R5, R3, R1, C11, D12, F13, B10, C10, E12, A9, B8, D10, A14, E15, B14, D15, AH2	I/O	OV _{DD}	—
CE_PD[0:27]	E11, D9, C8, F11, A7, E9, C7, A6, F10, B6, D7, E8, B5, A5, C2, E4, F5, B1, D2, G5, D1, E2, H6, F3, E1, F2, G3, H4	I/O	OV _{DD}	—
CE_PE[0:31]	K3, J2, F1, G2, J5, H3, G1, H2, K6, J3, K5, K4, L6, P6, P4, P3, P1, N4, N5, N2, N1, M2, M3, M5, M6, L1, L2, L4, E14, C13, C14, B13	I/O	OV _{DD}	—
CE_PF[0:3]	F14, D13, A12, A11	I/O	OV _{DD}	—
Clocks				
PCI_CLK_OUT[0]/CE_PF[26]	B22	I/O	LV _{DD} 2	—
PCI_CLK_OUT[1:2]/CE_PF[27:28]	D22, A23	I/O	OV _{DD}	—
CLKIN	E37	I	OV _{DD}	—
PCI_CLOCK/PCI_SYNC_IN	M36	I	OV _{DD}	—
PCI_SYNC_OUT/CE_PF[29]	D37	I/O	OV _{DD}	3
JTAG				
TCK	K33	I	OV _{DD}	—
TDI	K34	I	OV _{DD}	4
TDO	H37	O	OV _{DD}	3
TMS	J36	I	OV _{DD}	4
TRST	L32	I	OV _{DD}	4
Test				
TEST	L35	I	OV _{DD}	7
TEST_SEL	AU34	I	GV _{DD}	10
PMC				
QUIESCE	B36	O	OV _{DD}	—
System Control				

Table 72. CSB Frequency Options (continued)

CFG_CLKIN_DIV at Reset ¹	SPMF	csb_clk: Input Clock Ratio ²	Input Clock Frequency (MHz) ²			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0110	6:1	100	150	200	
Low	0111	7:1	116	175	233	
Low	1000	8:1	133	200	266	
Low	1001	9:1	150	225	300	
Low	1010	10:1	166	250	333	
Low	1011	11:1	183	275		
Low	1100	12:1	200	300		
Low	1101	13:1	216	325		
Low	1110	14:1	233			
Low	1111	15:1	250			
Low	0000	16:1	266			
High	0010	2:1				133
High	0011	3:1				100
High	0100	4:1				133
High	0101	5:1				166
High	0110	6:1				200
High	0111	7:1				233
High	1000	8:1				
High	1001	9:1				
High	1010	10:1				
High	1011	11:1				
High	1100	12:1				
High	1101	13:1				
High	1110	14:1				
High	1111	15:1				
High	0000	16:1				

¹ CFG_CLKIN_DIV is only used for host mode; CLKIN must be tied low and CFG_CLKIN_DIV must be pulled down (low) in agent mode.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

This table shows heat sinks and junction-to-ambient thermal resistance for TBGA package.

Table 78. Heat Sinks and Junction-to-Ambient Thermal Resistance of TBGA Package

Heat Sink Assuming Thermal Grease	Airflow	35 × 35 mm TBGA
		Junction-to-Ambient Thermal Resistance
AAVID 30 × 30 × 9.4 mm pin fin	Natural convection	10.7
AAVID 30 × 30 × 9.4 mm pin fin	1 m/s	6.2
AAVID 30 × 30 × 9.4 mm pin fin	2 m/s	5.3
AAVID 31 × 35 × 23 mm pin fin	Natural convection	8.1
AAVID 31 × 35 × 23 mm pin fin	1 m/s	4.4
AAVID 31 × 35 × 23 mm pin fin	2 m/s	3.7
Wakefield, 53 × 53 × 25 mm pin fin	Natural convection	5.4
Wakefield, 53 × 53 × 25 mm pin fin	1 m/s	3.2
Wakefield, 53 × 53 × 25 mm pin fin	2 m/s	2.4
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural convection	6.4
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	3.8
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	2.5
MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass	1 m/s	2.8

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following:

Aavid Thermalloy 603-224-9988
 80 Commercial St.
 Concord, NH 03301
 Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
 473 Sapena Ct. #15
 Santa Clara, CA 95054
 Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
 413 North Moss St.
 Burbank, CA 91502
 Internet: www.ctscorp.com

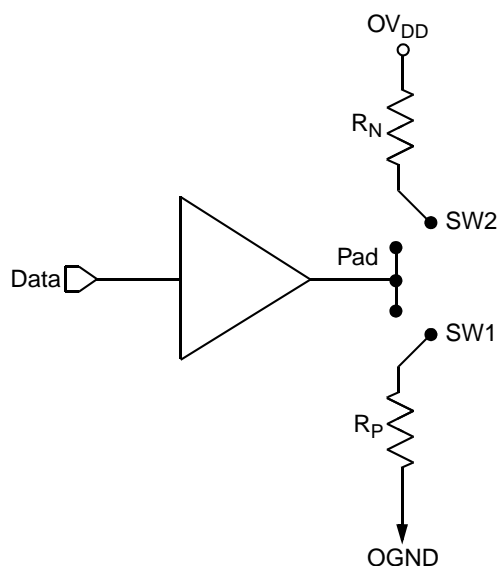


Figure 57. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{\text{source}} \times I_{\text{source}}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term} . The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2) \times I_{\text{source}}$. Solving for the output impedance gives $R_{\text{source}} = R_{\text{term}} \times (V_1/V_2 - 1)$. The drive current is then $I_{\text{source}} = V_1/R_{\text{source}}$.

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD} , nominal OV_{DD} , 105°C.

Table 79. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	20 Target	Z_0	W
R_P	42 Target	25 Target	20 Target	Z_0	W
Differential	NA	NA	NA	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, $T_J = 105^\circ\text{C}$.

23.6 Configuration Pin Muxing

The device provides the user with power-on configuration options that can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

Table 82. Revision History (continued)

Rev. Number	Date	Substantive Change(s)
3	03/2010	<ul style="list-style-type: none"> • Changed references to RCWH[PCICKEN] to RCWH[PCICKDRV]. • In Table 2, added extended temperature characteristics. • Added Figure 6, “DDR Input Timing Diagram.” • In Figure 53, “Mechanical Dimensions and Bottom Surface Nomenclature of the TBGA Package,” removed watermark. • Updated the title of Table 19, “DDR SDRAM Input AC Timing Specifications.” • In Table 20, “DDR and DDR2 SDRAM Input AC Timing Specifications Mode,” changed table subtitle. • In Table 27–Table 30, and Table 33–Table 34, changed the rise and fall time specifications to reference 20–80% and 80–20% of the voltage supply, respectively. • In Table 38, “IEEE 1588 Timer AC Specifications,” changed first parameter to “Timer clock frequency.” • In Table 45, “I2C AC Electrical Specifications,” changed units to “ns” for t_{I2DVKH}. • In Table 66, “MPC8360E TBGA Pinout Listing,” and Table 67 “MPC8358E TBGA Pinout Listing,” added note 7: “This pin must always be tied to GND” to the TEST pin and added a note to SPARE1 stating: “This pin must always be left not connected.” • In Section 4, “Clock Input Timing,” added note regarding rise/fall time on QUICC Engine block input pins. • Added Section 4.3, “Gigabit Reference Clock Input Timing.” • Updated Section 8.1.1, “10/100/1000 Ethernet DC Electrical Characteristics.” • In Section 20.3, “Pinout Listings,” added sentence stating “Refer to AN3097, ‘MPC8360/MPC8358E PowerQUICC Design Checklist,’ for proper pin termination and usage.” • In Section 21, “Clocking,” removed statement: “The OCCR[PCICDn] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUTn signals.” • In Section 21.1, “System PLL Configuration,” updated the system VCO frequency conditions. • In Table 80, added extended temperature characteristics.
2	12/2007	Initial release.