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Understanding Embedded - Microprocessors

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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	Νο
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8360evvajdga

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Overall DC Electrical Characteristics

2.1 **Overall DC Electrical Characteristics**

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings¹

	Characteristic	Symbol	Max Value	Unit	Notes
Core and PLL supply vo	ltage for	V _{DD} & AV _{DD}	-0.3 to 1.32	V	—
MPC8358 Device Part N Processor Frequency la QUICC Engine Frequen	Number with bel of AD=266MHz and AG=400MHz & icy label of E=300MHz & G=400MHz				
MPC8360 Device Part N Processor Frequency la QUICC Engine Frequen	Number with bel of AG=400MHz and AJ=533MHz & icy label of G=400MHz				
Core and PLL supply vo	ltage for	V _{DD} & AV _{DD}	-0.3 to 1.37	V	—
MPC8360 device Part N Processor Frequency la Frequency label of H=50	lumber with bel of AL=667MHz and QUICC Engine 00MHz				
DDR and DDR2 DRAM	I/O voltage DDR DDR2	GV _{DD}	-0.3 to 2.75 -0.3 to 1.89	V	—
Three-speed Ethernet I	O, MII management voltage	LV _{DD}	-0.3 to 3.63	V	—
PCI, local bus, DUART, I ² C, SPI, and JTAG I/O	system control and power management, voltage	OV _{DD}	-0.3 to 3.63	V	—
Input voltage	DDR DRAM signals	MV _{IN}	-0.3 to (GV _{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV _{REF}	-0.3 to (GV _{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV _{IN}	-0.3 to (LV _{DD} + 0.3)	V	4, 5
	Local bus, DUART, CLKIN, system control and power management, I ² C, SPI, and JTAG signals	OV _{IN}	-0.3 to (OV _{DD} + 0.3)	V	3, 5
	PCI	OV _{IN}	-0.3 to (OV _{DD} + 0.3)	V	6



Power Sequencing

This table shows the estimated typical I/O power dissipation for the device.

Interface	Parameter	GV _{DD} (1.8 V)	GV _{DD} (2.5 V)	OV _{DD} (3.3 V)	LV _{DD} (3.3 V)	LV _{DD} (2.5 V)	Unit	Comments
DDR I/O	200 MHz, 1 \times 32 bits	0.3	0.46	_	_	—	W	—
$R_s = 20 \Omega$	200 MHz, 1 \times 64 bits	0.4	0.58		_	—	W	—
$R_t = 50 \Omega$	200 MHz, 2×32 bits	0.6	0.92	_	_	—	W	_
	266 MHz, 1 \times 32 bits	0.35	0.56	_	_	—	W	_
	266 MHz, 1 \times 64 bits	0.46	0.7	_	_	—	W	_
	266 MHz, 2×32 bits	0.7	1.11		—	—	W	_
	333 MHz, 1 \times 32 bits	0.4	0.65	_	_	—	W	_
	333 MHz, 1 \times 64 bits	0.53	0.82		—	—	W	_
	333 MHz, 2×32 bits	0.81	1.3		—	—	W	_
Local Bus I/O	133 MHz, 32 bits	—	—	0.22	_	_	W	_
3 pairs of clocks	83 MHz, 32 bits	—	—	0.14	—	—	W	—
	66 MHz, 32 bits	—	—	0.12	—	—	W	_
	50 MHz, 32 bits	—	—	0.09	—	—	W	_
PCI I/O	33 MHz, 32 bits	—	—	0.05	—	—	W	_
Load = 30 pF	66 MHz, 32 bits	—	—	0.07	—	—	W	—
10/100/1000	MII or RMII	—	—	_	0.01	—	W	Multiply by
Load = 20 pF	GMII or TBI	—	—	_	0.04	—	W	interfaces used.
	RGMII or RTBI	—	—	—	—	0.04	W	
Other I/O	_	—	_	0.1	—	—	W	_

Table 6. Estimated Typical I/O Power Dissipation

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8360E/58E.

NOTE

The rise/fall time on QUICC Engine block input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of V_{DD} ; fall time refers to transitions from 90% to 10% of V_{DD} .



RESET DC Electrical Characteristics

Table 9. GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV (continued)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
GTX_CLK rise and fall time $\label{eq:VDD} \begin{array}{l} \text{LV}_{\text{DD}} = 2.5 \text{ V} \\ \text{LV}_{\text{DD}} = 3.3 \text{ V} \end{array}$	t _{G125R} /t _{G125F}	—	_	0.75 1.0	ns	1
GTX_CLK125 duty cycle GMII & TBI 1000Base-T for RGMII & RTBI	t _{G125H} /t _{G125}	45 47	—	55 53	%	2
GTX_CLK125 jitter	—	—	—	±150	ps	2

Notes:

- 1. Rise and fall times for GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
- GTX_CLK125 is used to generate the GTX clock for the UCC Ethernet transmitter with 2% degradation. The GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by GTX_CLK. See Section 8.2.2, "MII AC Timing Specifications," Section 8.2.3, "RMII AC Timing Specifications," and Section 8.2.5, "RGMII and RTBI AC Timing Specifications" for the duty cycle for 10Base-T and 100Base-T reference clock.

5 **RESET Initialization**

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8360E/58E.

5.1 **RESET DC Electrical Characteristics**

This table provides the DC electrical characteristics for the RESET pins of the device.

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V _{IH}	_	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	_	-0.3	0.8	V
Input current	I _{IN}	_	_	±10	μA
Output high voltage	V _{OH} ²	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V

Table 10. RESET Pins DC Electrical Characteristics ¹

Notes:

1. This table applies for pins PORESET, HRESET, SRESET, and QUIESCE.

2. HRESET and SRESET are open drain pins, thus V_{OH} is not relevant for those pins.



DDR and DDR2 SDRAM AC Electrical Characteristics

This table provides the input AC timing specifications for the DDR SDRAM interface when $GV_{DD}(typ) = 2.5 \text{ V}$.

Table 19. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol	Symbol Min		Unit	Notes
AC input low voltage	V _{IL}	—	MV _{REF} – 0.31	V	—
AC input high voltage	V _{IH}	MV _{REF} + 0.31	_	V	_

Table 20. DDR and DDR2 SDRAM Input AC Timing Specifications Mode

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
MDQS—MDQ/MECC input skew per byte 333 MHz 266 MHz 200 MHz	t _{DISKEW}	-750 -1125 -1250	750 1125 1250	ps	1, 2

Notes:

1. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.

Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 ≤n ≤7) or ECC (MECC[{0...7}] if n = 8).

This figure shows the input timing diagram for the DDR controller.



Figure 6. DDR Input Timing Diagram



DDR and DDR2 SDRAM AC Electrical Characteristics

This figure provides the AC test load for the DDR bus.



Figure 8. DDR AC Test Load

Table 22. DDR and DDR2 SDRAM Measurement Conditions

Symbol	DDR	DDR2	Unit	Notes
V _{TH}	MV _{REF} ± 0.31 V	MV _{REF} ± 0.25 V	V	1
V _{OUT}	$0.5 \times \text{ GV}_{\text{DD}}$	$0.5 \times \text{ GV}_{\text{DD}}$	V	2

Notes:

1. Data input threshold measurement point.

2. Data output measurement point.

This figure shows the DDR SDRAM output timing diagram for source synchronous mode.



Figure 9. DDR SDRAM Output Timing Diagram for Source Synchronous Mode





This section describes the DC and AC electrical specifications for the DUART interface of the MPC8360E/58E.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface of the device.

Table 23. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit	Notes
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V	—
Low-level input voltage OV _{DD}	V _{IL}	-0.3	0.8	V	—
High-level output voltage, I _{OH} = −100 μA	V _{OH}	OV _{DD} - 0.4	—	V	—
Low-level output voltage, I _{OL} = 100 μA	V _{OL}	—	0.2	V	—
Input current (0 V ≰⁄ _{IN} ≤OV _{DD})	I _{IN}	—	±10	μA	1

Note:

1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface of the device.

Table 24.	DUART	AC T	iming	Speci	ifications
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Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	_
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	_	2

Notes:

- 1. Actual attainable baud rate is limited by the latency of interrupt processing.
- 2. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

8 UCC Ethernet Controller: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

8.1 Three-Speed Ethernet Controller (10/100/1000 Mbps)— GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to all GMII (gigabit media independent interface), MII (media independent interface), RMII (reduced media independent interface), TBI (ten-bit interface), RGMII (reduced gigabit media independent interface), and RTBI (reduced ten-bit interface) signals except MDIO (management data input/output) and MDC (management data clock). The MII, RMII, GMII, and TBI interfaces are only defined for 3.3 V, while the RGMII and RTBI interfaces are only defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard reduced pin-count interface for Gigabit Ethernet



GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for the MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

8.1.1 10/100/1000 Ethernet DC Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), reduced media independent interface (RMII) signals, management data input/output (MDIO) and management data clock (MDC).

The MII and RMII interfaces are defined for 3.3 V, while the RGMII and RTBI interfaces can be operated at 2.5 V. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3*. The RMII interface follows the *RMII Consortium RMII Specification Version 1.2*.

Table 25. RGMII/RTBI, GMII, TBI, MII, and RMII DC Electrical Characteristics (when operating at 3.3 V)

Parameter	Symbol	Conditions		Min	Мах	Unit	Notes
Supply voltage 3.3 V	LV _{DD}	-		2.97	3.63	V	1
Output high voltage	V _{OH}	I _{OH} = -4.0 mA	$LV_{DD} = Min$	2.40	LV _{DD} + 0.3	V	—
Output low voltage	V _{OL}	I _{OL} = 4.0 mA	$LV_{DD} = Min$	GND	0.50	V	—
Input high voltage	V _{IH}	—	_	2.0	LV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	—	_	-0.3	0.90	V	—
Input current	I _{IN}	0 V ≤V _{IN} ≤LV _{DD}		—	±10	μA	—

Note:

1. GMII/MII pins that are not needed for RGMII, RMII, or RTBI operation are powered by the OV_{DD} supply.

Table 26. RGMII/RTBI DC Electrical Characteristics	(when o	perating	at 2.5 V)
	·······			,

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV _{DD}	_		2.37	2.63	V
Output high voltage	V _{OH}	I _{OH} = -1.0 mA	LV _{DD} = Min	2.00	LV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	LV _{DD} = Min	GND – 0.3	0.40	V
Input high voltage	V _{IH}	—	LV _{DD} = Min	1.7	LV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	$LV_{DD} = Min$	-0.3	0.70	V
Input current	I _{IN}	0 V ≤V _{II}	_N ≤LV _{DD}	—	±10	μA

8.2 GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII Timing Specifications

This sections describe the GMII transmit and receive AC timing specifications.



8.2.5 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 35. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
Data to clock output skew (at transmitter)	t _{SKRGTKHDX} t _{SKRGTKHDV}	-0.5 		— 0.5	ns	7
Data to clock input skew (at receiver)	t _{SKRGDXKH} t _{SKRGDVKH}	1.0		 2.6	ns	2
Clock cycle duration	t _{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	t _{RGTH} /t _{RGT}	45	50	55	%	4, 5
Duty cycle for 10BASE-T and 100BASE-TX	t _{RGTH} /t _{RGT}	40	50	60	%	3, 5
Rise time (20–80%)	t _{RGTR}	—		0.75	ns	
Fall time (20–80%)	t _{RGTF}	—	_	0.75	ns	
GTX_CLK125 reference clock period	t _{G125}	—	8.0	_	ns	6
GTX_CLK125 reference clock duty cycle	t _{G125H} /t _{G125}	47		53	%	

Notes:

- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (Rx) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- 2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns can be added to the associated clock signal.
- 3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
- 4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- 5. Duty cycle reference is LV_{DD}/2.
- 6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
- 7. In rev. 2.0 silicon, due to errata, t_{SKRGTKHDX} minimum is –2.3 ns and t_{SKRGTKHDV} maximum is 1 ns for UCC1, 1.2 ns for UCC2 option 1, and 1.8 ns for UCC2 option 2. In rev. 2.1 silicon, due to errata, t_{SKRGTKHDX} minimum is –0.65 ns for UCC2 option 1 and –0.9 for UCC2 option 2, and t_{SKRGTKHDV} maximum is 0.75 ns for UCC1 and UCC2 option 1 and 0.85 for UCC2 option 2. Refer to Errata QE_ENET10 in *Chip Errata for the MPC8360E, Rev. 1*. UCC1 does meet t_{SKRGTKHDX} minimum for rev. 2.1 silicon.



10.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device.

This table provides the JTAG AC timing specifications as defined in Figure 30 through Figure 33.

Table 43. JTAG AC Timing Specifications (Independent of CLKIN)¹

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f _{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t _{JTG}	30	—	ns	_
JTAG external clock duty cycle	t _{JTKHKL} /t _{JTG}	45	55	%	_
JTAG external clock rise and fall times	t _{JTGR} & t _{JTGF}	0	2	ns	_
TRST assert time	t _{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	t _{JTDVKH} t _{JTIVKH}	4 4	_	ns	4
Input hold times: Boundary-scan data TMS, TDI	t _{JTDXKH} t _{JTIXKH}	10 10	_	ns	4
Valid times: Boundary-scan data TDO	t _{JTKLDV} t _{JTKLOV}	2 2	11 11	ns	5
Output hold times: Boundary-scan data TDO	t _{jtkldx} t _{jtklox}	2 2	_	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	t _{JTKLDZ} t _{JTKLOZ}	2 2	19 9	ns	5, 6

Notes:

- 2. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
- 4. Non-JTAG signal input timing with respect to t_{TCLK}.
- 5. Non-JTAG signal output timing with respect to t_{TCLK}.
- 6. Guaranteed by design and characterization.

All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 22). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.



JTAG AC Electrical Characteristics

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.



Figure 29. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.



VM = Midpoint Voltage (OV_{DD}/2)

Figure 30. JTAG Clock Input Timing Diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.



This figure provides the boundary-scan timing diagram.



VM = Midpoint Voltage (OV_{DD}/2)



PCI AC Electrical Specifications

Table 47. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Clock to output high impedance	t _{PCKHOZ}	_	14	ns	2, 3
Input setup to clock	t _{PCIVKH}	3.0	_	ns	2, 4
Input hold from clock	t _{PCIXKH}	0.3	_	ns	2, 4, 6

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
 </sub>
- 2. See the timing measurement conditions in the PCI 2.2 Local Bus Specifications.
- 3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.
- 5. In rev. 2.0 silicon, due to errata, t_{PCIHOV} maximum is 6.6 ns. Refer to Errata PCI21 in Chip Errata for the MPC8360E, Rev. 1.
- 6. In rev. 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Refer to Errata PCI17 in Chip Errata for the MPC8360E, Rev. 1.

Table 48. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	t _{PCKHOV}	_	11	ns	2
Output hold from clock	t _{PCKHOX}	2	-	ns	2
Clock to output high impedance	t _{PCKHOZ}	_	14	ns	2, 3
Input setup to clock	t _{PCIVKH}	7.0	_	ns	2, 2
Input hold from clock	t _{PCIXKH}	0.3	_	ns	2, 4, 5

Notes:

- The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
- 2. See the timing measurement conditions in the PCI 2.2 Local Bus Specifications.
- 3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.
- 5. In rev. 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Refer to Errata PCI17 in Chip Errata for the MPC8360E, Rev. 1.

This figure provides the AC test load for PCI.



Figure 36. PCI AC Test Load





14.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 52. GPIO Input AC Timing Specifications¹

Characteristic	Symbol ²	Тур	Unit
GPIO inputs—minimum pulse width	t _{PIWID}	20	ns

Notes:

- 1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
- 2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

This figure provides the AC test load for the GPIO.



Figure 40. GPIO AC Test Load

15 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8360E/58E.

15.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins of the IPIC.

Table 53. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	—	—	±10	μA
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	—	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V

Notes:

1. This table applies for pins IRQ[0:7], IRQ_OUT, MCP_OUT, and CE ports Interrupts.

2. IRQ_OUT and MCP_OUT are open drain pins, thus V_{OH} is not relevant for those pins.



18.3 AC Test Load

These figures represent the AC timing from Table 62 and Table 63. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the timing with external clock.



Figure 50. AC Timing (External Clock) Diagram

This figure shows the timing with internal clock.



Figure 51. AC Timing (Internal Clock) Diagram



Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LCLK[2]/LCS[7]	G37	0	OV _{DD}	—
LSYNC_OUT	F34	0	OV _{DD}	—
LSYNC_IN	G35	I	OV _{DD}	—
	Programmable Interrupt Controller			•
MCP_OUT	E34	0	OV _{DD}	2
IRQ0/MCP_IN	C37	I	OV _{DD}	—
IRQ[1]/M1SRCID[4]/M2SRCID[4]/ LSRCID[4]	F35	I/O	OV _{DD}	
IRQ[2]/M1DVAL/M2DVAL/LDVAL	F36	I/O	OV _{DD}	—
IRQ[3]/CORE_SRESET	H34	I/O	OV _{DD}	—
IRQ[4:5]	G33, G32	I/O	OV _{DD}	—
IRQ[6]/LCS[6]/CKSTOP_OUT	E35	I/O	OV _{DD}	—
IRQ[7]/LCS[7]/CKSTOP_IN	H36	I/O	OV _{DD}	—
	DUART			•
UART1_SOUT/M1SRCID[0]/ M2SRCID[0]/LSRCID[0]	E32	0	OV _{DD}	_
UART1_SIN/M1SRCID[1]/ M2SRCID[1]/LSRCID[1]	B34	I/O	OV _{DD}	_
UART1_CTS/M1SRCID[2]/ M2SRCID[2]/LSRCID[2]	C34	I/O	OV _{DD}	_
UART1_RTS/M1SRCID[3]/ M2SRCID[3]/LSRCID[3]	A35	0	OV _{DD}	—
	I ² C Interface			
IIC1_SDA	D34	I/O	OV _{DD}	2
IIC1_SCL	B35	I/O	OV _{DD}	2
IIC2_SDA	E33	I/O	OV _{DD}	2
IIC2_SCL	C35	I/O	OV _{DD}	2
	QUICC Engine Block			
CE_PA[0]	F8	I/O	LV _{DD0}	—
CE_PA[1:2]	AH1, AG5	I/O	OV _{DD}	_
CE_PA[3:7]	F6, D4, C3, E5, A3	I/O	LV _{DD} 0	
CE_PA[8]	AG3	I/O	OV _{DD}	—
CE_PA[9:12]	F7, B3, E6, B4	I/O	LV _{DD} 0	—
CE_PA[13:14]	AG1, AF6	I/O	OV _{DD}	—
CE_PA[15]	B2	I/O	LV _{DD} 0	_
CE_PA[16]	AF4	I/O	OV _{DD}	_
CE_PA[17:21]	B16, A16, E17, A17, B17	I/O	LV _{DD} 1	



Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	РМС			
QUIESCE	B36	0	OV _{DD}	_
	System Control			
PORESET	L37	I	OV _{DD}	—
HRESET	L36	I/O	OV _{DD}	1
SRESET	M33	I/O	OV _{DD}	2
	Thermal Management			
THERM0	AP19	Ι	GV _{DD}	—
THERM1	AT31	I	GV _{DD}	—
	Power and Ground Signals			
AV _{DD} 1	K35	Power for LBIU DLL (1.2 V)	AV _{DD} 1	_
AV _{DD} 2	К36	Power for CE PLL (1.2 V)	AV _{DD} 2	_
AV _{DD} 5	AM29	Power for e300 PLL (1.2 V)	AV _{DD} 5	_
AV _{DD} 6	К37	Power for system PLL (1.2 V)	AV _{DD} 6	_
GND	A2, A8, A13, A19, A22, A25, A31, A33, A36, B7, B12, B24, B27, B30, C4, C6, C9, C15, C26, C32, D3, D8, D11, D14, D17, D19, D23, D27, E7, E13, E25, E30, E36, F4, F37, G34, H1, H5, H32, H33, J4, J32, J37, K1, L3, L5, L33, L34, M1, M34, M35, N37, P2, P5, P35, P36, R4, T3, U1, U5, U35, V37, W1, W4, W33, W36, Y34, AA3, AA5, AC3, AC32, AC35, AD1, AD37, AE4, AE34, AE36, AF33, AG4, AG6, AG32, AH35, AJ1, AJ4, AJ32, AJ35, AJ37, AK36, AL3, AL34, AM4, AN6, AN23, AN30, AP8, AP12, AP14, AP16, AP17, AP20, AP25, AR6, AR8, AR9, AR19, AR24, AR31, AR35, AR37, AT4, AT10, AT19, AT20, AT25, AU14, AU22, AU28, AU35	_	_	_
GV _{DD}	AD4, AE3, AF1, AF5, AF35, AF37, AG2, AG36, AH33, AH34, AK5, AM1, AM35, AM37, AN2, AN10, AN11, AN12, AN14, AN32, AN36, AP5, AP23, AP28, AR1, AR7, AR10, AR12, AR21, AR25, AR27, AR33, AT15, AT22, AT28, AT33, AU2, AU5, AU16, AU31, AU36	Power for DDR DRAM I/O voltage (2.5 or 1.8 V)	GV _{DD}	



Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes			
No Connect							
NC	AM20, AU19	—	—	—			

Notes:

- 1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}
- 2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
- 3. This output is actively driven during reset rather than being three-stated during reset.
- 4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- 5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
- 6. These are On Die Termination pins, used to control DDR2 memories internal termination resistance.
- 7. This pin must always be tied to GND.
- 8. This pin must always be left not connected.
- 9. Refer to MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual section on "RGMII Pins," for information about the two UCC2 Ethernet interface options.
- 10.It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor for DDR2.

This table shows the pin list of the MPC8358E TBGA package.

Table 67. MPC8358E TBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	DDR SDRAM Memory Controller Interface			
MEMC1_MDQ[0:63]	AJ34, AK33, AL33, AL35, AJ33, AK34, AK32, AM36, AN37, AN35, AR34, AT34, AP37, AP36, AR36, AT35, AP34, AR32, AP32, AM31, AN33, AM34, AM33, AM30, AP31, AM27, AR30, AT32, AN29, AP29, AN27, AR29, AN8, AN7, AM8, AM6, AP9, AN9, AT7, AP7, AU6, AP6, AR4, AR3, AT6, AT5, AR5, AT3, AP4, AM5, AP3, AN3, AN5, AL5, AN4, AM2, AL2, AH5, AK3, AJ2, AJ3, AH4, AK4, AH3	I/O	GV _{DD}	
MEMC_MECC[0:4]/MSRCID[0:4]	AP24, AN22, AM19, AN19, AM24	I/O	GV _{DD}	—
MEMC_MECC[5]/MDVAL	AM23	I/O	GV _{DD}	—
MEMC_MECC[6:7]	AM22, AN18	I/O	GV _{DD}	—
MEMC_MDM[0:8]	AL36, AN34, AP33, AN28,AT9, AU4, AM3, AJ6,AP27	0	GV _{DD}	Ι
MEMC_MDQS[0:8]	AK35, AP35, AN31, AM26,AT8, AU3, AL4, AJ5, AP26	I/O	GV _{DD}	Ι
MEMC_MBA[0:1]	AU29, AU30	0	GV _{DD}	
MEMC_MBA[2]	AT30	0	GV _{DD}	_
MEMC_MA[0:14]	AU21, AP22, AP21, AT21, AU25, AU26, AT23, AR26, AU24, AR23, AR28, AU23, AR22, AU20, AR18	0	GV _{DD}	
MEMC_MODT[0:3]	AG33, AJ36, AT1, AK2	0	GV _{DD}	6



Signal	Package Pin Number	Pin Type	Power Supply	Notes			
CE_PB[0:27]	AE2, AE1, AD5, AD3, AD2, AC6, AC5, AC4, AC2, AC1, AB5, AB4, AB3, AB1, AA6, AA4, AA2, Y6, Y4, Y3, Y2, Y1, W6, W5, W2, V5, V3, V2	I/O	OV _{DD}	_			
CE_PC[0:1]	V1, U6	I/O	OV _{DD}				
CE_PC[2:3]	C16, A15	I/O	LV _{DD} 1	—			
CE_PC[4:6]	U4, U3, T6	I/O	OV _{DD}	—			
CE_PC[7]	C19	I/O	LV _{DD} 2	—			
CE_PC[8:9]	A4, C5	I/O	LV _{DD} 0	—			
CE_PC[10:30]	T5, T4, T2, T1, R5, R3, R1, C11, D12, F13, B10, C10, E12, A9, B8, D10, A14, E15, B14, D15, AH2	I/O	OV _{DD}	_			
CE_PD[0:27]	E11, D9, C8, F11, A7, E9, C7, A6, F10, B6, D7, E8, B5, A5, C2, E4, F5, B1, D2, G5, D1, E2, H6, F3, E1, F2, G3, H4	I/O	OV _{DD}	—			
CE_PE[0:31]	K3, J2, F1, G2, J5, H3, G1, H2, K6, J3, K5, K4, L6, P6, P4, P3, P1, N4, N5, N2, N1, M2, M3, M5, M6, L1, L2, L4, E14, C13, C14, B13	I/O	OV _{DD}	—			
CE_PF[0:3]	F14, D13, A12, A11	I/O	OV _{DD}	—			
	Clocks						
PCI_CLK_OUT[0]/CE_PF[26]	B22	I/O	LV _{DD} 2	—			
PCI_CLK_OUT[1:2]/CE_PF[27:28]	D22, A23	I/O	OV _{DD}	—			
CLKIN	E37	I	OV _{DD}	—			
PCI_CLOCK/PCI_SYNC_IN	M36	I	OV _{DD}	—			
PCI_SYNC_OUT/CE_PF[29]	D37	I/O	OV _{DD}	3			
	JTAG						
ТСК	K33	I	OV _{DD}	_			
TDI	К34	I	OV _{DD}	4			
TDO	H37	0	OV _{DD}	3			
TMS	J36	I	OV _{DD}	4			
TRST	L32	I	OV _{DD}	4			
Test							
TEST	L35	I	OV _{DD}	7			
TEST_SEL	AU34	I	GV _{DD}	10			
PMC							
QUIESCE	B36	0	OV _{DD}	—			
System Control							

Table 67. MPC8358E TBGA Pinout Listing (continued)



clock. When the device is configured as a PCI agent device the CLKIN and the CFG_CLKIN_DIV signals should be tied to GND.

When the device is configured as a PCI host device (RCWH[PCIHOST] = 1) and PCI clock output is disabled (RCWH[PCICKDRV] = 0), clock distribution and balancing done externally on the board. Therefore, PCI_SYNC_IN is the primary input clock.

As shown in Figure 54 and Figure 55, the primary clock input (frequency) is multiplied by the QUICC Engine block phase-locked loop (PLL), the system PLL, and the clock unit to create the QUICC Engine clock (ce_clk), the coherent system bus clock (csb_clk), the internal DDRC1 controller clock ($ddr1_clk$), and the internal clock for the local bus interface unit and DDR2 memory controller (lb_clk).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb_clk = \{PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)\} \times SPMF$$

In PCI host mode, PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV) is the CLKIN frequency; in PCI agent mode, CFG_CLKIN_DIV must be pulled down (low), so PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV) is the PCI_CLK frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, "Reset, Clocking, and Initialization," in the *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more information on the clock subsystem.

The *ce_clk* frequency is determined by the QUICC Engine PLL multiplication factor (RCWL[CEPMF) and the QUICC Engine PLL division factor (RCWL[CEPDF]) according to the following equation:

 $ce_clk = (primary clock input \times CEPMF) \div (1 + CEPDF)$

The internal *ddr1_clk* frequency is determined by the following equation:

 $ddr1_clk = csb_clk \times (1 + RCWL[DDR1CM])$

Note that the lb_clk clock frequency (for DDRC2) is determined by RCWL[LBCM]. The *internal ddr1_clk* frequency is not the external memory bus frequency; *ddr1_clk* passes through the DDRC1 clock divider (\div 2) to create the differential DDRC1 memory bus clock outputs (MEMC1_MCK and MEMC1_MCK). However, the data rate is the same frequency as *ddr1_clk*.

The internal *lb_clk* frequency is determined by the following equation:

 $lb_clk = csb_clk \times (1 + \text{RCWL[LBCM]})$

Note that *lb_clk* is not the external local bus or DDRC2 frequency; *lb_clk* passes through the a LB clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LB clock divider ratio is controlled by LCRR[CLKDIV].

Additionally, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. This table specifies which units have a configurable clock frequency.

Unit	Default Frequency	Options
Security core	csb_clk/3	Off, <i>csb_clk</i> ¹ , <i>csb_clk</i> /2, <i>csb_clk</i> /3
PCI and DMA complex	csb_clk	Off, <i>csb_clk</i>

Table 68	Configurable	Clock	Units
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¹ With limitation, only for slow csb_clk rates, up to 166 MHz.

This table provides the operating frequencies for the TBGA package under recommended operating conditions (see Table 2). All frequency combinations shown in the table below may not be available. Maximum operating frequencies depend on the part



Core PLL Configuration

21.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). This table shows the encodings for RCWL[COREPLL]. COREPLL values not listed in this table should be considered reserved.

RCWL[COREPLL]		core_clk:csb_clk	VCO dividor		
0–1	2–5	6	Ratio	VCO divider	
nn	0000	n	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)	
00	0001	0	1:1	÷2	
01	0001	0	1:1	÷4	
10	0001	0	1:1	÷8	
11	0001	0	1:1	÷8	
00	0001	1	1.5:1	÷2	
01	0001	1	1.5:1	÷4	
10	0001	1	1.5:1	÷8	
11	0001	1	1.5:1	÷8	
00	0010	0	2:1	÷2	
01	0010	0	2:1	÷4	
10	0010	0	2:1	÷8	
11	0010	0	2:1	÷8	
00	0010	1	2.5:1	÷2	
01	0010	1	2.5:1	÷4	
10	0010	1	2.5:1	÷8	
11	0010	1	2.5:1	÷8	
00	0011	0	3:1	÷2	
01	0011	0	3:1	÷4	
10	0011	0	3:1	÷8	
11	0011	0	3:1	÷8	

Table 73. e300 Core PLL Configuration

NOTE

Core VCO frequency = Core frequency \times VCO divider. The VCO divider (RCWL[COREPLL[0:1]]) must be set properly so that the core VCO frequency is in the range of 800–1800 MHz. Having a core frequency below the CSB frequency is not a possible option because the core frequency must be equal to or greater than the CSB frequency.



22.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

 T_I = junction temperature (° C)

 T_C = case temperature of the package (° C)

 $R_{\theta JC}$ = junction to case thermal resistance (° C/W)

 P_D = power dissipation (W)

23 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8360E/58E. Additional information can be found in *MPC8360E/MPC8358E PowerQUICC Design Checklist* (AN3097).

23.1 System Clocking

The device includes two PLLs, as follows.

- The platform PLL (AV_{DD}1) generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in Section 21.1, "System PLL Configuration."
- The e300 core PLL (AV_{DD}2) generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 21.2, "Core PLL Configuration."

23.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD} 1, AV_{DD} 2, respectively). The AV_{DD} level should always be equivalent to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in Figure 56, one to each of the five AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.