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NXP USA Inc. - MPC8360EVVALFG Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8360evvalfg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Overall DC Electrical Characteristics

2.1 **Overall DC Electrical Characteristics**

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings¹

	Characteristic	Symbol	Max Value	Unit	Notes
Core and PLL supply voltage for		V _{DD} & AV _{DD}	-0.3 to 1.32	V	—
MPC8358 Device Part Number with Processor Frequency label of AD=266MHz and AG=400MHz & QUICC Engine Frequency label of E=300MHz & G=400MHz					
MPC8360 Device Part N Processor Frequency la QUICC Engine Frequen	Number with bel of AG=400MHz and AJ=533MHz & icy label of G=400MHz				
Core and PLL supply vo	ltage for	V _{DD} & AV _{DD}	-0.3 to 1.37	V	—
MPC8360 device Part N Processor Frequency la Frequency label of H=50	lumber with bel of AL=667MHz and QUICC Engine 00MHz				
DDR and DDR2 DRAM	I/O voltage DDR DDR2	GV _{DD}	-0.3 to 2.75 -0.3 to 1.89	V	—
Three-speed Ethernet I	O, MII management voltage	LV _{DD}	-0.3 to 3.63	V	—
PCI, local bus, DUART, I ² C, SPI, and JTAG I/O	system control and power management, voltage	OV _{DD}	-0.3 to 3.63	V	—
Input voltage	DDR DRAM signals	MV _{IN}	-0.3 to (GV _{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV _{REF}	-0.3 to (GV _{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV _{IN}	-0.3 to (LV _{DD} + 0.3)	V	4, 5
	Local bus, DUART, CLKIN, system control and power management, I ² C, SPI, and JTAG signals	OV _{IN}	-0.3 to (OV _{DD} + 0.3)	V	3, 5
	PCI	OV _{IN}	-0.3 to (OV _{DD} + 0.3)	V	6



DDR and DDR2 SDRAM AC Electrical Characteristics

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input high voltage	V _{IH}	MV _{REF} + 0.18	GV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.18	V	—
Output leakage current	I _{OZ}	—	±10	μA	4
Output high current (V _{OUT} = 1.95 V)	I _{ОН}	-15.2	-	mA	—
Output low current (V _{OUT} = 0.35 V)	I _{OL}	15.2	_	mA	—
MV _{REF} input leakage current	I _{VREF}	—	±10	μA	—
Input current (0 V ≰⁄ _{IN} ≤OV _{DD})	I _{IN}	—	±10	μA	_

Table 16. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V (continued)

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.

- 2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
- 3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
- 4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

This table provides the DDR capacitance when $GV_{DD}(typ) = 2.5$ V.

Table 17. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C _{DIO}	_	0.5	pF	1

Note:

1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25° C, V_{OUT} = $GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM interface when $GV_{DD}(typ) = 1.8 V$.

Table 18. DDR2 SDRAM Input AC Timing Specifications for GV_{DD}(typ) = 1.8 V

At recommended operating conditions with GV_{DD} of 1.8 V ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V _{IL}	—	MV _{REF} – 0.25	V	—
AC input high voltage	V _{IH}	MV _{REF} + 0.25	_	V	_



DDR and DDR2 SDRAM AC Electrical Characteristics

This table provides the input AC timing specifications for the DDR SDRAM interface when $GV_{DD}(typ) = 2.5 \text{ V}$.

Table 19. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V _{IL}	—	MV _{REF} – 0.31	V	—
AC input high voltage	V _{IH}	MV _{REF} + 0.31	_	V	_

Table 20. DDR and DDR2 SDRAM Input AC Timing Specifications Mode

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
MDQS—MDQ/MECC input skew per byte 333 MHz 266 MHz 200 MHz	t _{DISKEW}	-750 -1125 -1250	750 1125 1250	ps	1, 2

Notes:

1. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.

Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 ≤n ≤7) or ECC (MECC[{0...7}] if n = 8).

This figure shows the input timing diagram for the DDR controller.



Figure 6. DDR Input Timing Diagram



Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter ⁸	Symbol ¹	Min	Мах	Unit	Notes
MDQS epilogue end	t _{DDKHME}	-0.6	0.9	ns	7

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
 </sub>
- 2. All MCK/ \overline{MCK} referenced measurements are made from the crossing of the two signals ±0.1 V.
- In the source synchronous mode, MCK/MCK can be shifted in ¼ applied cycle increments through the clock control register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
- ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.
- 5. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. Refer MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual for a description and understanding of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the device.
- All outputs are referenced to the rising edge of MCK(n) at the pins of the device. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
- 8. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.
- 9. In rev. 2.0 silicon, t_{DDKHMH} maximum meets the specification of 0.6 ns. In rev. 2.0 silicon, due to errata, t_{DDKHMH} minimum is –0.9 ns. Refer to Errata DDR18 in *Chip Errata for the MPC8360E, Rev. 1*.

This figure shows the DDR SDRAM output timing for address skew with respect to any MCK.







GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

8.2.1.2 GMII Receive AC Timing Specifications

This table provides the GMII receive AC timing specifications.

Table 28. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
RX_CLK clock period	t _{GRX}	_	8.0	—	ns	_
RX_CLK duty cycle	t _{GRXH} /t _{GRX}	40		60	%	—
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{GRDVKH}	2.0		—	ns	—
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t _{GRDXKH}	0.2		—	ns	2
RX_CLK clock rise time, (20% to 80%)	t _{GRXR}	_		1.0	ns	—
RX_CLK clock fall time, (80% to 20%)	t _{GRXF}	_	_	1.0	ns	—

Notes:

- 1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- In rev. 2.0 silicon, due to errata, t_{GRDXKH} minimum is 0.5 which is not compliant with the standard. Refer to Errata QE_ENET18 in Chip Errata for the MPC8360E, Rev. 1.

This figure shows the GMII receive AC timing diagram.



Figure 11. GMII Receive AC Timing Diagram



8.2.4.1 TBI Transmit AC Timing Specifications

This table provides the TBI transmit AC timing specifications.

Table 33. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
GTX_CLK clock period	t _{TTX}	_	8.0	_	ns	—
GTX_CLK duty cycle	t _{TTXH} /t _{TTX}	40	—	60	%	—
GTX_CLK to TBI data TCG[9:0] delay	t _{TTKHDX} t _{TTKHDV}	1.0	—	 5.0	ns	3
GTX_CLK clock rise time, (20% to 80%)	t _{TTXR}	_	—	1.0	ns	—
GTX_CLK clock fall time, (80% to 20%)	t _{TTXF}	_	_	1.0	ns	—
GTX_CLK125 reference clock period	t _{G125}	_	8.0	_	ns	2
GTX_CLK125 reference clock duty cycle	t _{G125H} /t _{G125}	45	—	55	ns	—

Notes:

- The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 2. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
- 3. In rev. 2.0 silicon, due to errata, t_{TTKHDX} minimum is 0.7 ns for UCC1. Refer to Errata QE_ENET19 in Chip Errata for the MPC8360E, Rev. 1.

This figure shows the TBI transmit AC timing diagram.



Figure 18. TBI Transmit AC Timing Diagram





Figure 27. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (DLL Bypass Mode)



JTAG AC Electrical Characteristics

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.



Figure 29. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.



VM = Midpoint Voltage (OV_{DD}/2)

Figure 30. JTAG Clock Input Timing Diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.



This figure provides the boundary-scan timing diagram.



VM = Midpoint Voltage (OV_{DD}/2)





I2C AC Electrical Specifications

11.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interface of the device.

Table 45. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 44).

Parameter	Symbol ¹	Min	Max	Unit	Note
SCL clock frequency	f _{I2C}	0	400	kHz	2
Low period of the SCL clock	t _{I2CL}	1.3	_	μs	—
High period of the SCL clock	t _{I2CH}	0.6	_	μs	—
Setup time for a repeated START condition	t _{I2SVKH}	0.6	_	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL}	0.6	_	μs	_
Data setup time	t _{I2DVKH}	100	_	ns	3
Data hold time: CBUS compatible masters I ² C bus devices	t _{I2DXKL}	$\frac{1}{0^2}$	 0.9 ³	μs	—
Rise time of both SDA and SCL signals	t _{I2CR}	20 + 0.1 C _b ⁴	300	ns	—
Fall time of both SDA and SCL signals	t _{I2CF}	20 + 0.1 C _b ⁴	300	ns	—
Set-up time for STOP condition	t _{I2PVKH}	0.6	_	μs	—
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	_	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times \text{OV}_{\text{DD}}$	_	V	_
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times \text{OV}_{\text{DD}}$	_	V	_

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional}

block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

 The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) to bridge the undefined region of the falling edge of SCL.

3. The maximum t_{12DVKH} has only to be met if the device does not stretch the LOW period (t_{12CL}) of the SCL signal.

4. C_B = capacitance of one bus line in pF.



This figure provides the AC test load for the I^2C .



Figure 34. I²C AC Test Load

This figure shows the AC timing diagram for the I^2C bus.



12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8360E/58E.

12.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface of the device.

Table 46. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Мах	Unit
High-level input voltage	V _{IH}	$V_{OUT} \ge V_{OH}$ (min) or	$0.5\times\text{OV}_\text{DD}$	OV _{DD} + 0.5	V
Low-level input voltage	V _{IL}	V _{OUT} ≤V _{OL} (max)	-0.5	$0.3 imes OV_{DD}$	V
High-level output voltage	V _{OH}	I _{OH} = -500 μA	$0.9 imes OV_{DD}$	—	V
Low-level output voltage	V _{OL}	l _{OL} = 1500 μA	—	$0.1 imes OV_{DD}$	V
Input current	I _{IN}	0 V ≤V _{IN} ¹ ≤OV _{DD}	—	±10	μA

12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the device. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. This table provides the PCI AC timing specifications at 66 MHz.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Clock to output valid	t _{PCKHOV}	_	6.0	ns	2, 5
Output hold from clock	t _{PCKHOX}	1	—	ns	2

Table 47. PCI AC Timing Specifications at 66 MHz

PCI AC Electrical Specifications

Table 47. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Clock to output high impedance	t _{PCKHOZ}	_	14	ns	2, 3
Input setup to clock	t _{PCIVKH}	3.0	_	ns	2, 4
Input hold from clock	t _{PCIXKH}	0.3	_	ns	2, 4, 6

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
 </sub>
- 2. See the timing measurement conditions in the PCI 2.2 Local Bus Specifications.
- 3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.
- 5. In rev. 2.0 silicon, due to errata, t_{PCIHOV} maximum is 6.6 ns. Refer to Errata PCI21 in Chip Errata for the MPC8360E, Rev. 1.
- 6. In rev. 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Refer to Errata PCI17 in Chip Errata for the MPC8360E, Rev. 1.

Table 48. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	t _{PCKHOV}	_	11	ns	2
Output hold from clock	t _{PCKHOX}	2	-	ns	2
Clock to output high impedance	t _{PCKHOZ}	_	14	ns	2, 3
Input setup to clock	t _{PCIVKH}	7.0	_	ns	2, 2
Input hold from clock	t _{PCIXKH}	0.3	_	ns	2, 4, 5

Notes:

- The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
- 2. See the timing measurement conditions in the PCI 2.2 Local Bus Specifications.
- 3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.
- 5. In rev. 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Refer to Errata PCI17 in Chip Errata for the MPC8360E, Rev. 1.

This figure provides the AC test load for PCI.



Figure 36. PCI AC Test Load



Timers AC Timing Specifications

13.2 Timers AC Timing Specifications

This table provides the timer input and output AC timing specifications.

Table 50. Timers Input AC Timing Specifications¹

Characteristic	Symbol ²	Тур	Unit
Timers inputs—minimum pulse width	t _{TIWID}	20	ns

Notes:

- 1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
- 2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

This figure provides the AC test load for the timers.



Figure 39. Timers AC Test Load

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8360E/58E.

14.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the device GPIO.

Table 51. GPIO DC Electrical Charac

Characteristic	Symbol	Condition	Min	Мах	Unit	Notes
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	—	V	1
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V	1
Input low voltage	V _{IL}	—	-0.3	0.8	V	—
Input current	I _{IN}	$0 \ V \leq V_{IN} \leq OV_{DD}$	—	±10	μA	—

Note:

1. This specification applies when operating from 3.3-V supply.



IPIC AC Timing Specifications

15.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 54. IPIC Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
IPIC inputs—minimum pulse width	t _{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any
external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when
working in edge triggered mode.

16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8360E/58E.

16.1 SPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the device SPI.

Table 55. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	0 V ≤V _{IN} ≤OV _{DD}	_	±10	μA

16.2 SPI AC Timing Specifications

This table and provide the SPI input and output AC timing specifications.

Table 56. SPI AC Timing Specifications¹

Characteristic	Symbol ²	Min	Мах	Unit
SPI outputs—Master mode (internal clock) delay	t _{NIKHOX} t _{NIKHOV}	0.3	8	ns
SPI outputs—Slave mode (external clock) delay	t _{NEKHOX} t _{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t _{NIIVKH}	8	—	ns
SPI inputs—Master mode (internal clock) input hold time	t _{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t _{NEIVKH}	4	—	ns



Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_DEVSEL/CE_PF[16]	E26	I/O	OV _{DD}	5
PCI_IDSEL/CE_PF[17]	F22	I/O	OV _{DD}	
PCI_SERR/CE_PF[18]	B29	I/O	OV _{DD}	5
PCI_PERR/CE_PF[19]	A29	I/O	OV _{DD}	5
PCI_REQ[0]/CE_PF[20]	F19	I/O	LV _{DD} 2	—
PCI_REQ[1]/CPCI_HS_ES/ CE_PF[21]	A21	I/O	LV _{DD} 2	—
PCI_REQ[2]/CE_PF[22]	C21	I/O	LV _{DD} 2	
PCI_GNT[0]/CE_PF[23]	E20	I/O	LV _{DD} 2	
PCI_GNT[1]/CPCI1_HS_LED/ CE_PF[24]	B20	I/O	LV _{DD} 2	
PCI_GNT[2]/CPCI1_HS_ENUM/ CE_PF[25]	C20	I/O	LV _{DD} 2	
PCI_MODE	D36	I	OV _{DD}	—
M66EN/CE_PF[4]	B37	I/O	OV _{DD}	
	Local Bus Controller Interface			
LAD[0:31]	N32, N33, N35, N36, P37, P32, P34, R36, R35, R34, R33, T37, T35, T34, T33, U37, T32, U36, U34, V36, V35, W37, W35, V33, V32, W34, Y36, W32, AA37, Y33, AA35, AA34	I/O	OV _{DD}	_
LDP[0]/CKSTOP_OUT	AB37	I/O	OV _{DD}	
LDP[1]/CKSTOP_IN	AB36	I/O	OV _{DD}	
LDP[2]/LCS[6]	AB35	I/O	OV _{DD}	
LDP[3]/LCS[7]	AA33	I/O	OV _{DD}	
LA[27:31]	AC37, AA32, AC36, AC34, AD36	0	OV _{DD}	
LCS[0:5]	AD33, AG37, AF34, AE33, AD32, AH37	0	OV_{DD}	
LWE[0:3]/LSDDQM[0:3]/LBS[0:3]	AG35, AG34, AH36, AE32	0	OV_{DD}	
LBCTL	AD35	0	OV_{DD}	
LALE	M37	0	OV_{DD}	
LGPL0/LSDA10/cfg_reset_source0	AB32	I/O	OV_{DD}	
LGPL1/LSDWE/cfg_reset_source1	AE37	I/O	OV_{DD}	
LGPL2/LSDRAS/LOE	AC33	0	OV_{DD}	
LGPL3/LSDCAS/cfg_reset_source2	AD34	I/O	OV_{DD}	
LGPL4/LGTA/LUPWAIT/LPBSE	AE35	I/O	OV_{DD}	
LGPL5/cfg_clkin_div	AF36	I/O	OV_{DD}	
LCKE	G36	0	OV _{DD}	—
LCLK[0]	J33	0	OV _{DD}	—
LCLK[1]/LCS[6]	J34	0	OV _{DD}	—



Pinout Listings

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes		
No Connect						
NC	AM20, AU19	—	—	—		

Notes:

- 1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}
- 2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
- 3. This output is actively driven during reset rather than being three-stated during reset.
- 4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- 5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
- 6. These are On Die Termination pins, used to control DDR2 memories internal termination resistance.
- 7. This pin must always be tied to GND.
- 8. This pin must always be left not connected.
- 9. Refer to MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual section on "RGMII Pins," for information about the two UCC2 Ethernet interface options.
- 10.It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor for DDR2.

This table shows the pin list of the MPC8358E TBGA package.

Table 67. MPC8358E TBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	DDR SDRAM Memory Controller Interface			
MEMC1_MDQ[0:63]	AJ34, AK33, AL33, AL35, AJ33, AK34, AK32, AM36, AN37, AN35, AR34, AT34, AP37, AP36, AR36, AT35, AP34, AR32, AP32, AM31, AN33, AM34, AM33, AM30, AP31, AM27, AR30, AT32, AN29, AP29, AN27, AR29, AN8, AN7, AM8, AM6, AP9, AN9, AT7, AP7, AU6, AP6, AR4, AR3, AT6, AT5, AR5, AT3, AP4, AM5, AP3, AN3, AN5, AL5, AN4, AM2, AL2, AH5, AK3, AJ2, AJ3, AH4, AK4, AH3	I/O	GV _{DD}	
MEMC_MECC[0:4]/MSRCID[0:4]	AP24, AN22, AM19, AN19, AM24	I/O	GV _{DD}	—
MEMC_MECC[5]/MDVAL	AM23	I/O	GV _{DD}	—
MEMC_MECC[6:7]	AM22, AN18	I/O	GV _{DD}	—
MEMC_MDM[0:8]	AL36, AN34, AP33, AN28,AT9, AU4, AM3, AJ6,AP27	0	GV _{DD}	Ι
MEMC_MDQS[0:8]	AK35, AP35, AN31, AM26,AT8, AU3, AL4, AJ5, AP26	I/O	GV _{DD}	Ι
MEMC_MBA[0:1]	AU29, AU30	0	GV _{DD}	
MEMC_MBA[2]	AT30	0	GV _{DD}	_
MEMC_MA[0:14]	AU21, AP22, AP21, AT21, AU25, AU26, AT23, AR26, AU24, AR23, AR28, AU23, AR22, AU20, AR18	0	GV _{DD}	
MEMC_MODT[0:3]	AG33, AJ36, AT1, AK2	0	GV _{DD}	6



Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes	
PCI_MODE	D36	I	OV _{DD}		
M66EN/CE_PF[4]	B37	I/O	OV _{DD}		
	Local Bus Controller Interface				
LAD[0:31]	N32, N33, N35, N36, P37, P32, P34, R36, R35, R34, R33, T37, T35, T34, T33, U37, T32, U36, U34, V36, V35, W37, W35, V33, V32, W34, Y36, W32, AA37, Y33, AA35, AA34	I/O	OV _{DD}	_	
LDP[0]/CKSTOP_OUT	AB37	I/O	OV_{DD}	_	
LDP[1]/CKSTOP_IN	AB36	I/O	OV _{DD}	_	
LDP[2]/LCS[6]	AB35	I/O	OV _{DD}	_	
LDP[3]/LCS[7]	AA33	I/O	OV _{DD}		
LA[27:31]	AC37, AA32, AC36, AC34, AD36	0	OV _{DD}		
LCS[0:5]	AD33, AG37, AF34, AE33, AD32, AH37	0	OV _{DD}		
LWE[0:3]/LSDDQM[0:3]/LBS[0:3]	AG35, AG34, AH36, AE32	0	OV _{DD}		
LBCTL	AD35	0	OV _{DD}		
LALE	M37	0	OV _{DD}		
LGPL0/LSDA10/cfg_reset_source0	AB32	I/O	OV _{DD}		
LGPL1/LSDWE/cfg_reset_source1	AE37	I/O	OV _{DD}		
LGPL2/LSDRAS/LOE	AC33	0	OV _{DD}		
LGPL3/LSDCAS/cfg_reset_source2	AD34	I/O	OV _{DD}		
LGPL4/LGTA/LUPWAIT/LPBSE	AE35	I/O	OV _{DD}	_	
LGPL5/cfg_clkin_div	AF36	I/O	OV _{DD}	_	
LCKE	G36	0	OV _{DD}		
LCLK[0]	J33	0	OV _{DD}	_	
LCLK[1]/LCS[6]	J34	0	OV _{DD}	_	
LCLK[2]/LCS[7]	G37	0	OV _{DD}		
LSYNC_OUT	F34	0	OV _{DD}		
LSYNC_IN	G35	I	OV _{DD}		
Programmable Interrupt Controller					
MCP_OUT	E34	0	OV _{DD}	2	
IRQ0/MCP_IN	C37	I	OV _{DD}	_	
IRQ[1]/M1SRCID[4]/M2SRCID[4]/ LSRCID[4]	F35	I/O	OV_{DD}		
IRQ[2]/M1DVAL/M2DVAL/LDVAL	F36	I/O	OV _{DD}	_	
IRQ[3]/CORE_SRESET	H34	I/O	OV_{DD}		



This figure shows the internal distribution of clocks within the MPC8358E.





The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Note that in PCI host mode, the primary clock input also depends on whether PCI clock outputs are selected with RCWH[PCICKDRV]. When the device is configured as a PCI host device (RCWH[PCIHOST] = 1) and PCI clock output is selected (RCWH[PCICKDRV] = 1), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (\div 2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCIOEN*n*] parameters enable the PCI_CLK_OUT*n*, respectively.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input





ordered, see Section 24.1, "Part Numbers Fully Addressed by this Document," for part ordering details and contact your Freescale sales representative or authorized distributor for more information.

Characteristic ¹	400 MHz	533 MHz	667 MHz ²	Unit
e300 core frequency (<i>core_clk</i>)	266–400	266–533	266–667	MHz
Coherent system bus frequency (<i>csb_clk</i>)		MHz		
QUICC Engine frequency ³ (<i>ce_clk</i>)		MHz		
DDR and DDR2 memory bus frequency (MCLK) ⁴		MHz		
Local bus frequency (LCLK <i>n</i>) ⁵	16.67–133			MHz
PCI input frequency (CLKIN or PCI_CLK)	25–66.67		MHz	
Security core maximum internal operating frequency	133	133	166	MHz

Table 69. Operating Frequencies for the TBGA Package

Notes:

- 1. The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
- 2. The 667 MHz core frequency is based on a 1.3 V V_{DD} supply voltage.
- 3. The 500 MHz QE frequency is based on a 1.3 V V_{DD} supply voltage.
- 4. The DDR data rate is 2x the DDR memory bus frequency.
- 5. The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWL[LBCM]).

21.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] and RCWL[SVCOD] parameters. This table shows the multiplication factor encodings for the system PLL.

RCWL[SPMF]	System PLL Multiplication Factor
0000	× 16
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11

Table 70. System PLL Multiplication Factors

System PLL Configuration

RCWL[SPMF]	System PLL Multiplication Factor
1100	× 12
1101	× 13
1110	× 14
1111	× 15

The RCWL[SVCOD] denotes the system PLL VCO internal frequency as shown in this table.

-	
RCWL[SVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

Table 71. System PLL VCO Divider

NOTE

The VCO divider must be set properly so that the system VCO frequency is in the range of 600-1400 MHz.

The system VCO frequency is derived from the following equations:

- $csb_clk = \{PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)\} \times SPMF$
- System VCO Frequency = *csb_clk* × VCO divider (if both RCWL[DDRCM] and RCWL[LBCM] are cleared) OR
- System VCO frequency = $2 \times csb_clk \times$ VCO divider (if either RCWL[DDRCM] or RCWL[LBCM] are set).

As described in Section 21, "Clocking," the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). This table shows the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

			Input Clock Frequency (MHz) ²			
CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2:1				133
Low	0011	3:1			100	200
Low	0100	4:1		100	133	266
Low	0101	5:1		125	166	333

Table 72. CSB Frequency Options

Part Numbers Fully Addressed by this Document

Device	Package	SVR (Rev. 2.0)	SVR (Rev. 2.1)
MPC8358E	TBGA	0x804A_0020	0x804A_0021
MPC8358	TBGA	0x804B_0020	0x804B_0021

25 Document Revision History

This table provides a revision history for this document.

Table 82. Revision History

Rev. Number	Date	Substantive Change(s)
5	09/2011	 Section 2.2.1, "Power-Up Sequencing", added the current limitation "3A to 5A" for the excessive current. Section 2.1.2, "Power Supply Voltage Specification, Updated the Characteristic for TBGA (MPC8358 & MPC8360 Device) with specific frequency for Core and PLL voltages. Added table footnote 3 to Table 2. Applied table footnotes 1 and 2 to Table 10. Removed table footnotes from Table 19. Applied table footnotes 8 and 9 to Table 40. Applied table footnotes 2 and 3 to Table 41. Applied table footnotes from Table 46. Applied table footnote to last three rows of Table 65.
4	01/2011	 Updated references to the LCRR register throughout Removed references to DDR DLL mode in Section 6.2.2, "DDR and DDR2 SDRAM Output AC Timing Specifications." Changed "Junction-to-Case" to "Junction-to-Ambient" in Section 22.2.4, "Heat Sinks and Junction-to-Ambient Thermal Resistance," and Table 78, "Heat Sinks and Junction-to-Ambient Thermal Resistance of TBGA Package," titles.