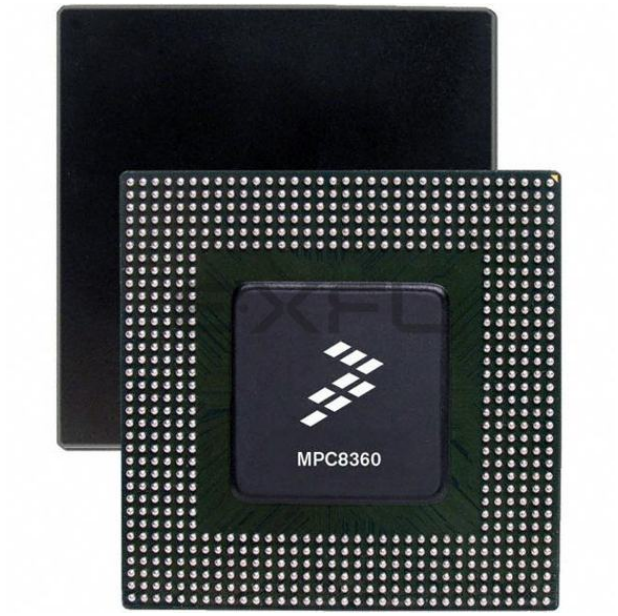

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8360evvalfh

- 10/100 Mbps Ethernet/IEEE Std. 802.3™ CDMA/CS interface through a media-independent interface (MII, RMII, RGMII)[1]
- 1000 Mbps Ethernet/IEEE 802.3 CDMA/CS interface through a media-independent interface (GMII, RGMII, TBI, RTBI) on UCC1 and UCC2
- 9.6-Kbyte jumbo frames
- ATM full-duplex SAR, up to 622 Mbps (OC-12/STM-4), AAL0, AAL1, and AAL5 in accordance ITU-T I.363.5
- ATM AAL2 CPS, SSSAR, and SSTED up to 155 Mbps (OC-3/STM-1) Mbps full duplex (with 4 CPS packets per cell) in accordance ITU-T I.366.1 and I.363.2
- ATM traffic shaping for CBR, VBR, UBR, and GFR traffic types compatible with ATM forum TM4.1 for up to 64-Kbyte simultaneous ATM channels
- ATM AAL1 structured and unstructured circuit emulation service (CES 2.0) in accordance with ITU-T I.163.1 and ATM Forum af-vtoa-00-0078.000
- IMA (Inverse Multiplexing over ATM) for up to 31 IMA links over 8 IMA groups in accordance with the ATM forum AF-PHY-0086.000 (Version 1.0) and AF-PHY-0086.001 (Version 1.1)
- ATM Transmission Convergence layer support in accordance with ITU-T I.432
- ATM OAM handling features compatible with ITU-T I.610
- PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686, and 3153
- IP support for IPv4 packets including TOS, TTL, and header checksum processing
- Ethernet over first mile IEEE 802.3ah
- Shim header
- Ethernet-to-Ethernet/AAL5/AAL2 inter-working
- L2 Ethernet switching using MAC address or IEEE Std. 802.1P/Q™ VLAN tags
- ATM (AAL2/AAL5) to Ethernet (IP) interworking in accordance with RFC2684 including bridging of ATM ports to Ethernet ports
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- AAL2 protocol rate up to 4 CPS at OC-3/STM-1 rate
- Packet over Sonet (POS) up to 622-Mbps full-duplex 124 MultiPHY
- POS hardware; microcode must be loaded as an IRAM package
- Transparent up to 70-Mbps full-duplex
- HDLC up to 70-Mbps full-duplex
- HDLC BUS up to 10 Mbps
- Asynchronous HDLC
- UART
- BISYNC up to 2 Mbps
- User-programmable Virtual FIFO size
- QUICC multichannel controller (QMC) for 64 TDM channels

— One multichannel communication controller (MCC) only on the MPC8360E supporting the following:
- 256 HDLC or transparent channels
- 128 SS7 channels
- Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces

— Two UTOPIA/POS interfaces on the MPC8360E supporting 124 MultiPHY each (optional 2*128 MultiPHY with extended address) and one UTOPIA/POS interface on the MPC8358E supporting 31/124 MultiPHY

— Two serial peripheral interfaces (SPI); SPI2 is dedicated to Ethernet PHY management

1.SMII or SGMII media-independent interface is not currently supported.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Max Value	Unit	Notes
Core and PLL supply voltage for MPC8358 Device Part Number with Processor Frequency label of AD=266MHz and AG=400MHz & QUICC Engine Frequency label of E=300MHz & G=400MHz MPC8360 Device Part Number with Processor Frequency label of AG=400MHz and AJ=533MHz & QUICC Engine Frequency label of G=400MHz		V_{DD} & AV_{DD}	–0.3 to 1.32	V	—
Core and PLL supply voltage for MPC8360 device Part Number with Processor Frequency label of AL=667MHz and QUICC Engine Frequency label of H=500MHz		V_{DD} & AV_{DD}	–0.3 to 1.37	V	—
DDR and DDR2 DRAM I/O voltage DDR DDR2		GV_{DD}	 –0.3 to 2.75 –0.3 to 1.89	V	—
Three-speed Ethernet I/O, MII management voltage		LV_{DD}	–0.3 to 3.63	V	—
PCI, local bus, DUART, system control and power management, I^2C, SPI, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	4, 5
	Local bus, DUART, CLKIN, system control and power management, I^2C, SPI, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3, 5
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6

This figure shows the undershoot and overshoot voltage of the PCI interface of the device for the 3.3-V signals, respectively.

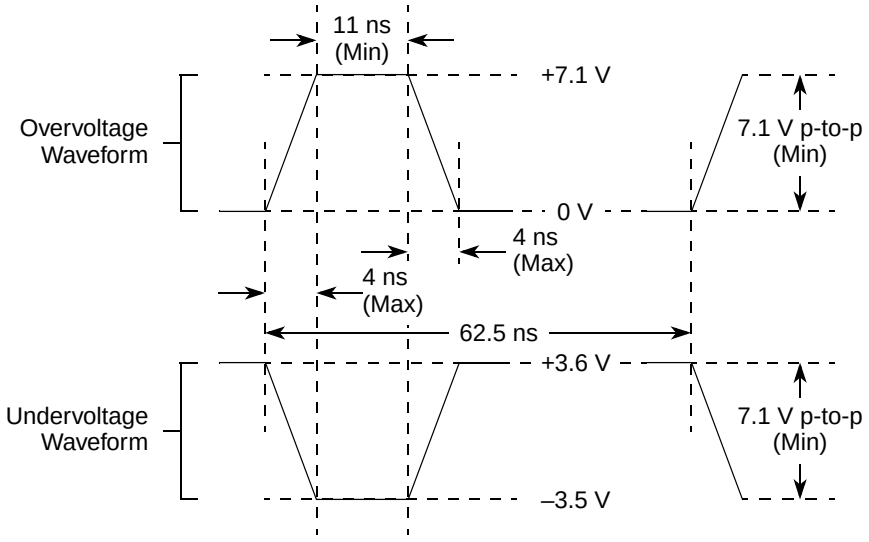


Figure 4. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	OV_{DD} = 3.3 V
PCI signals	25	
PCI output clocks (including PCI_SYNC_OUT)	42	
DDR signal	20 36 (half-strength mode)[1]	GV_{DD} = 2.5 V
DDR2 signal	18 36 (half-strength mode)[1]	GV_{DD} = 1.8 V
10/100/1000 Ethernet signals	42	LV_{DD} = 2.5/3.3 V
DUART, system control, I^2C, SPI, JTAG	42	OV_{DD} = 3.3 V
GPIO signals	42	OV_{DD} = 3.3 V LV_{DD} = 2.5/3.3 V

Note:
1. DDR output impedance values for half strength mode are verified by design and not tested.

2.2 Power Sequencing

This section details the power sequencing considerations for the MPC8360E/58E.

Table 4. MPC8360E TBGA Core Power Dissipation[1] (continued)

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
667	333	500	6.1	6.8	W	2, 3, 5, 9

Notes:
1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 6.
2. Typical power is based on a voltage of V_{DD} = 1.2 V or 1.3 V, a junction temperature of T_J = 105° C, and a Dhrystone benchmark application.
3. Thermal solutions need to design to a value higher than typical power on the end application, T_A target, and I/O power.
4. Maximum power is based on a voltage of V_{DD} = 1.2 V, WC process, a junction T_J = 105° C, and an artificial smoke test.
5. Maximum power is based on a voltage of V_{DD} = 1.3 V for applications that use 667 MHz (CPU)/500 (QE) with WC process, a junction T_J = 105° C, and an artificial smoke test.
6. Typical power is based on a voltage of V_{DD} = 1.3 V, a junction temperature of T_J = 70° C, and a Dhrystone benchmark application.
7. Maximum power is based on a voltage of V_{DD} = 1.3 V for applications that use 667 MHz (CPU) or 500 (QE) with WC process, a junction T_J = 70° C, and an artificial smoke test.
8. This frequency combination is only available for rev. 2.0 silicon.
9. This frequency combination is not available for rev. 2.0 silicon.

Table 5. MPC8358E TBGA Core Power Dissipation[1]

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	300	4.1	4.5	W	2, 3, 4
400	266	400	4.5	5.0	W	2, 3, 4

Notes:
1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 6.
2. Typical power is based on a voltage of V_{DD} = 1.2 V, a junction temperature of T_J = 105° C, and a Dhrystone benchmark application.
3. Thermal solutions need to design to a value higher than typical power on the end application, T_A target, and I/O power.
4. Maximum power is based on a voltage of V_{DD} = 1.2 V, WC process, a junction T_J = 105° C, and an artificial smoke test.

This table shows the estimated typical I/O power dissipation for the device.

Table 6. Estimated Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	Unit	Comments
DDR I/O 65% utilization R_S = 20 Ω R_t = 50 Ω 2 pairs of clocks	200 MHz, 1 × 32 bits	0.3	0.46	—	—	—	W	—
	200 MHz, 1 × 64 bits	0.4	0.58	—	—	—	W	—
	200 MHz, 2 × 32 bits	0.6	0.92	—	—	—	W	—
	266 MHz, 1 × 32 bits	0.35	0.56	—	—	—	W	—
	266 MHz, 1 × 64 bits	0.46	0.7	—	—	—	W	—
	266 MHz, 2 × 32 bits	0.7	1.11	—	—	—	W	—
	333 MHz, 1 × 32 bits	0.4	0.65	—	—	—	W	—
	333 MHz, 1 × 64 bits	0.53	0.82	—	—	—	W	—
	333 MHz, 2 × 32 bits	0.81	1.3	—	—	—	W	—
Local Bus I/O Load = 25 pf 3 pairs of clocks	133 MHz, 32 bits	—	—	0.22	—	—	W	—
	83 MHz, 32 bits	—	—	0.14	—	—	W	—
	66 MHz, 32 bits	—	—	0.12	—	—	W	—
	50 MHz, 32 bits	—	—	0.09	—	—	W	—
PCI I/O Load = 30 pF	33 MHz, 32 bits	—	—	0.05	—	—	W	—
	66 MHz, 32 bits	—	—	0.07	—	—	W	—
10/100/1000 Ethernet I/O Load = 20 pF	MII or RMII	—	—	—	0.01	—	W	Multiply by number of interfaces used.
	GMII or TBI	—	—	—	0.04	—	W	
	RGMII or RTBI	—	—	—	—	0.04	W	
Other I/O	—	—	—	0.1	—	—	W	—

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8360E/58E.

NOTE

The rise/fall time on QUICC Engine block input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of V_{DD}; fall time refers to transitions from 90% to 10% of V_{DD}.

Table 16. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	MV_{REF} + 0.18	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.18	V	—
Output leakage current	I_{OZ}	—	±10	µA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–15.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	15.2	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	±10	µA	—
Input current (0 V ≤V_{IN} ≤OV_{DD})	I_{IN}	—	±10	µA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤V_{OUT} ≤GV_{DD}.

This table provides the DDR capacitance when GV_{DD}(typ) = 2.5 V.

Table 17. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25° C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM interface when GV_{DD}(typ) = 1.8 V.

Table 18. DDR2 SDRAM Input AC Timing Specifications for GV_{DD}(typ) = 1.8 V

At recommended operating conditions with GV_{DD} of 1.8 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V	—

Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode (continued)

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) ± 5%.

Parameter[8]	Symbol[1]	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKHME}	–0.6	0.9	ns	7

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. In the source synchronous mode, MCK/$\overline{\text{MCK}}$ can be shifted in ¼ applied cycle increments through the clock control register. For the skew measurements referenced for t_{AOSKEW} it is assumed that the clock adjustment is set to align the address/command valid with the rising edge of MCK.
4. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.
5. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. In source synchronous mode, this is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. Refer *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
6. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the device.
7. All outputs are referenced to the rising edge of MCK(n) at the pins of the device. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
8. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.
9. In rev. 2.0 silicon, t_{DDKHMH} maximum meets the specification of 0.6 ns. In rev. 2.0 silicon, due to errata, t_{DDKHMH} minimum is –0.9 ns. Refer to Errata DDR18 in *Chip Errata for the MPC8360E, Rev. 1*.

This figure shows the DDR SDRAM output timing for address skew with respect to any MCK.

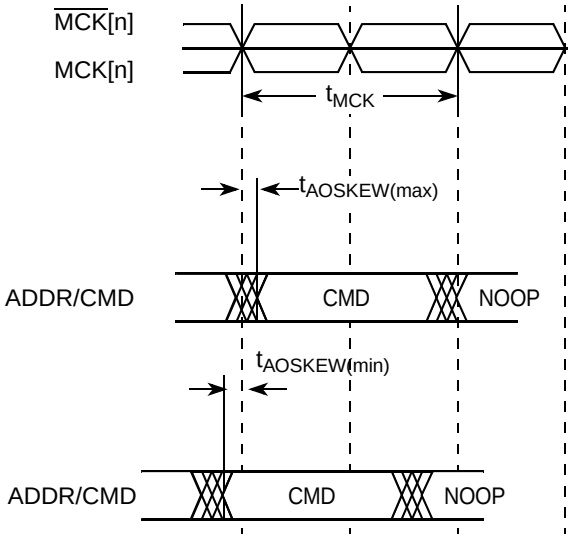


Figure 7. Timing Diagram for t_{AOSKEW} Measurement

Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for the MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

8.1.1 10/100/1000 Ethernet DC Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), reduced media independent interface (RMII) signals, management data input/output (MDIO) and management data clock (MDC).

The MII and RMII interfaces are defined for 3.3 V, while the RGMII and RTBI interfaces can be operated at 2.5 V. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3.* The RMII interface follows the *RMII Consortium RMII Specification Version 1.2.*

Table 25. RGMII/RTBI, GMII, TBI, MII, and RMII DC Electrical Characteristics (when operating at 3.3 V)

Parameter	Symbol	Conditions		Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD}	—		2.97	3.63	V	1
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	LV_{DD} = Min	2.40	LV_{DD} + 0.3	V	—
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	LV_{DD} = Min	GND	0.50	V	—
Input high voltage	V_{IH}	—	—	2.0	LV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	—	—	–0.3	0.90	V	—
Input current	I_{IN}	0 V ≤V_{IN} ≤LV_{DD}		—	±10	μA	—

Note:
1. GMII/MII pins that are not needed for RGMII, RMII, or RTBI operation are powered by the OV_{DD} supply.

Table 26. RGMII/RTBI DC Electrical Characteristics (when operating at 2.5 V)

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.00	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	–0.3	0.70	V
Input current	I_{IN}	0 V ≤V_{IN} ≤LV_{DD}		—	±10	μA

8.2 GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII Timing Specifications

This sections describe the GMII transmit and receive AC timing specifications.

Table 32. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise time	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load.

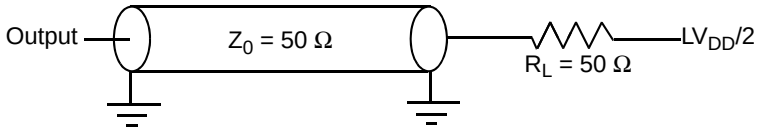


Figure 16. AC Test Load

This figure shows the RMII receive AC timing diagram.

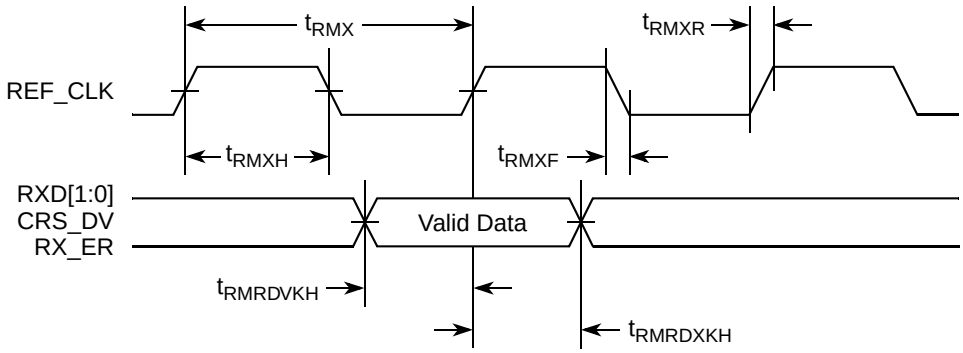


Figure 17. RMII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.3.3 IEEE 1588 Timer AC Specifications

This table provides the IEEE 1588 timer AC specifications.

Table 38. IEEE 1588 Timer AC Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Timer clock frequency	t_{TMRCK}	0	70	MHz	1
Input setup to timer clock	t_{TMRCKS}	—	—	—	2, 3
Input hold from timer clock	t_{TMRCKH}	—	—	—	2, 3
Output clock to output valid	t_{GCLKNV}	0	6	ns	—
Timer alarm to output valid	t_{TMRAL}	—	—	—	2

Notes:
1. The timer can operate on rtc_clock or tmr_clock. These clocks get muxed and any one of them can be selected. The minimum and maximum requirement for both rtc_clock and tmr_clock are the same.
2. These are asynchronous signals.
3. Inputs need to be stable at least one TMR clock.

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8360E/58E.

9.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface.

Table 39. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.4	—	V
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current	I_{IN}	—	±10	µA

9.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface of the device.

Table 40. Local Bus General Timing Parameters—DLL Enabled

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	—	ns	2
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	1.7	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.9	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4

10.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the device.

This table provides the JTAG AC timing specifications as defined in Figure 30 through Figure 33.

Table 43. JTAG AC Timing Specifications (Independent of CLKIN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock duty cycle	t_{JTKHKL}/t_{JTG}	45	55	%	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 22). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

14.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 52. GPIO Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Typ	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

This figure provides the AC test load for the GPIO.

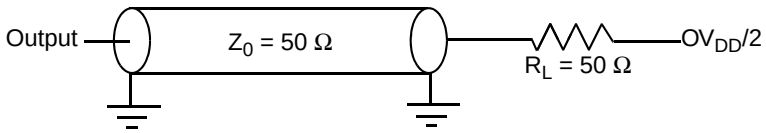


Figure 40. GPIO AC Test Load

15 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8360E/58E.

15.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins of the IPIC.

Table 53. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±10	μA
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, $\overline{\text{MCP\_OUT}}$, and CE ports Interrupts.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

Table 56. SPI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

This figure provides the AC test load for the SPI.

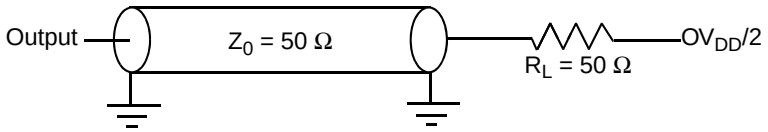
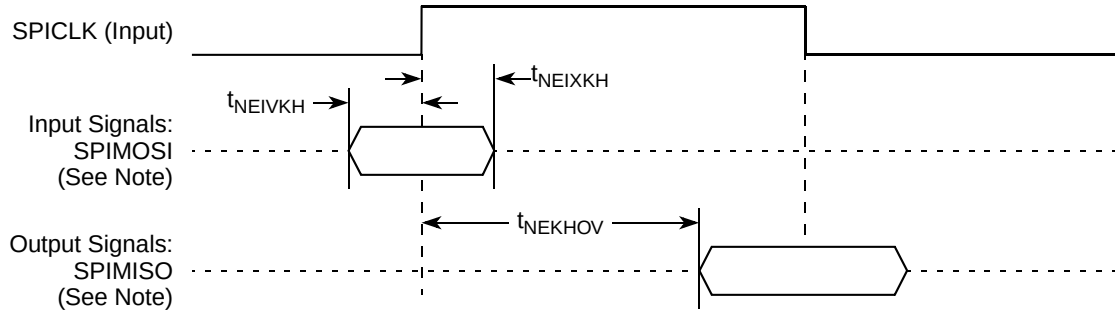


Figure 41. SPI AC Test Load

These figures represent the AC timing from Table 56. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

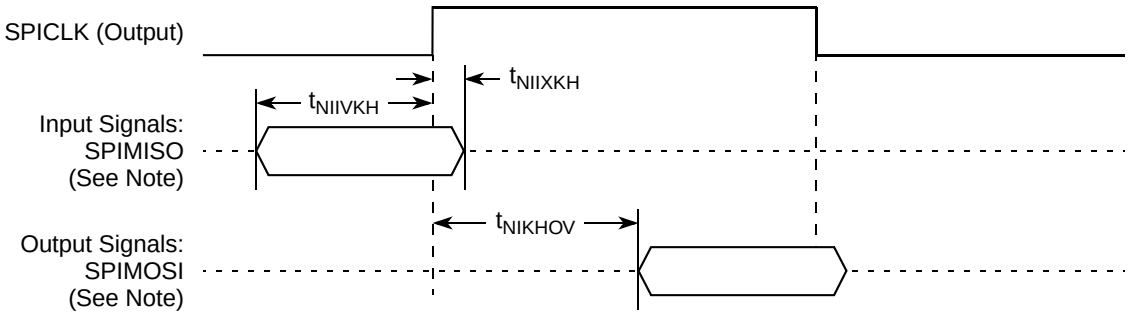
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 42. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in Master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 43. SPI AC Timing in Master Mode (Internal Clock) Diagram

This figure shows the UTOPIA timing with internal clock.

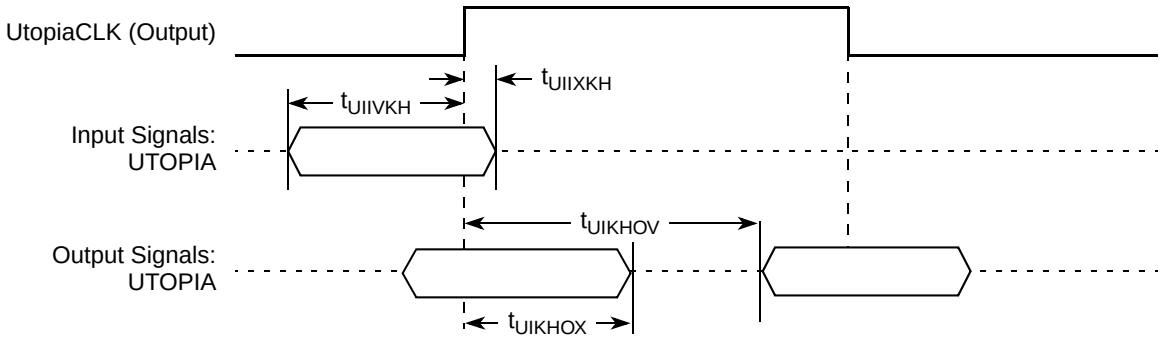


Figure 48. UTOPIA AC Timing (Internal Clock) Diagram

18 HDLC, BISYNC, Transparent, and Synchronous UART

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent, and synchronous UART protocols of the MPC8360E/58E.

18.1 HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

This table provides the DC electrical characteristics for the device HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 61. HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤V_{IN} ≤OV_{DD}	—	±10	μA

18.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

These tables provide the input and output AC timing specifications for HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 62. HDLC, BISYNC, and Transparent AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	t_{HIKHOV}	0	11.2	ns
Outputs—External clock delay	t_{HEKHOV}	1	10.8	ns

19 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8360E/58E.

19.1 USB DC Electrical Characteristics

This table provides the DC electrical characteristics for the USB interface.

Table 64. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 µA	V_{OH}	OV_{DD} – 0.4	—	V
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current	I_{IN}	—	±10	µA

19.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface of the device.

Table 65. USB General Timing Parameters

Parameter	Symbol[1]	Min	Max	Unit	Notes	Note
USB clock cycle time	t_{USCK}	20.83	—	ns	Full speed 48 MHz	—
USB clock cycle time	t_{USCK}	166.67	—	ns	Low speed 6 MHz	—
Skew between TXP and TXN	t_{USTSPN}	—	5	ns	—	2
Skew among RXP, RXN, and RXD	$t_{USRSPND}$	—	10	ns	Full speed transitions	2
Skew among RXP, RXN, and RXD	t_{USRPND}	—	100	ns	Low speed transitions	2

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(state)(signal)}}$ for receive signals and $t_{\text{(first two letters of functional block)(state)(signal)}}$ for transmit signals. For example, $t_{USRSPND}$ symbolizes USB timing (US) for the USB receive signals skew (RS) among RXP, RXN, and RXD (PND). Also, t_{USTSPN} symbolizes USB timing (US) for the USB transmit signals skew (TS) between TXP and TXN (PN).
2. Skew measurements are done at $OV_{DD}/2$ of the rising or falling edge of the signals.

This figure provide the AC test load for the USB.

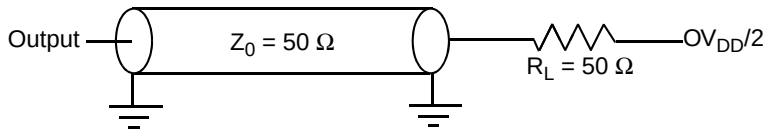


Figure 52. USB AC Test Load

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
No Connect				
NC	AM20, AU19	—	—	—

Notes:
1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. These are On Die Termination pins, used to control DDR2 memories internal termination resistance.
7. This pin must always be tied to GND.
8. This pin must always be left not connected.
9. Refer to *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* section on "RGMII Pins," for information about the two UCC2 Ethernet interface options.
10. It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor for DDR2.

This table shows the pin list of the MPC8358E TBGA package.

Table 67. MPC8358E TBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Controller Interface				
MEMC1_MDQ[0:63]	AJ34, AK33, AL33, AL35, AJ33, AK34, AK32, AM36, AN37, AN35, AR34, AT34, AP37, AP36, AR36, AT35, AP34, AR32, AP32, AM31, AN33, AM34, AM33, AM30, AP31, AM27, AR30, AT32, AN29, AP29, AN27, AR29, AN8, AN7, AM8, AM6, AP9, AN9, AT7, AP7, AU6, AP6, AR4, AR3, AT6, AT5, AR5, AT3, AP4, AM5, AP3, AN3, AN5, AL5, AN4, AM2, AL2, AH5, AK3, AJ2, AJ3, AH4, AK4, AH3	I/O	GV_{DD}	—
MEMC_MECC[0:4]/MSRCID[0:4]	AP24, AN22, AM19, AN19, AM24	I/O	GV_{DD}	—
MEMC_MECC[5]/MDVAL	AM23	I/O	GV_{DD}	—
MEMC_MECC[6:7]	AM22, AN18	I/O	GV_{DD}	—
MEMC_MDM[0:8]	AL36, AN34, AP33, AN28,AT9, AU4, AM3, AJ6,AP27	O	GV_{DD}	—
MEMC_MDQS[0:8]	AK35, AP35, AN31, AM26,AT8, AU3, AL4, AJ5, AP26	I/O	GV_{DD}	—
MEMC_MBA[0:1]	AU29, AU30	O	GV_{DD}	
MEMC_MBA[2]	AT30	O	GV_{DD}	—
MEMC_MA[0:14]	AU21, AP22, AP21, AT21, AU25, AU26, AT23, AR26, AU24, AR23, AR28, AU23, AR22, AU20, AR18	O	GV_{DD}	—
MEMC_MODT[0:3]	AG33, AJ36, AT1, AK2	O	GV_{DD}	6

21.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). This table shows the encodings for RCWL[COREPLL]. COREPLL values not listed in this table should be considered reserved.

Table 73. e300 Core PLL Configuration

RCWL[COREPLL]			***core_clk*:*csb_clk* Ratio**	**VCO divider**
0–1	**2–5**	**6**		
nn	**0000**	n	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
00	**0001**	0	1:1	÷2
01	**0001**	0	1:1	÷4
10	**0001**	0	1:1	÷8
11	**0001**	0	1:1	÷8
00	**0001**	1	1.5:1	÷2
01	**0001**	1	1.5:1	÷4
10	**0001**	1	1.5:1	÷8
11	**0001**	1	1.5:1	÷8
00	**0010**	0	2:1	÷2
01	**0010**	0	2:1	÷4
10	**0010**	0	2:1	÷8
11	**0010**	0	2:1	÷8
00	**0010**	1	2.5:1	÷2
01	**0010**	1	2.5:1	÷4
10	**0010**	1	2.5:1	÷8
11	**0010**	1	2.5:1	÷8
00	**0011**	0	3:1	÷2
01	**0011**	0	3:1	÷4
10	**0011**	0	3:1	÷8
11	**0011**	0	3:1	÷8

NOTE

Core VCO frequency = Core frequency × VCO divider. The VCO divider (RCWL[COREPLL[0:1]]) must be set properly so that the core VCO frequency is in the range of 800–1800 MHz. Having a core frequency below the CSB frequency is not a possible option because the core frequency must be equal to or greater than the CSB frequency.

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (° C)
T_B = board temperature at the package perimeter (° C)
$R_{\theta JA}$ = junction to board thermal resistance (° C/W) per JESD51-8
P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

22.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (° C)
T_T = thermocouple temperature on top of package (° C)
Ψ_{JT} = junction-to-ambient thermal resistance (° C/W)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

22.2.4 Heat Sinks and Junction-to-Ambient Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (° C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (° C/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (° C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-millennium.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Interface material vendors include the following:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

22.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb force (4.5 kg force). If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

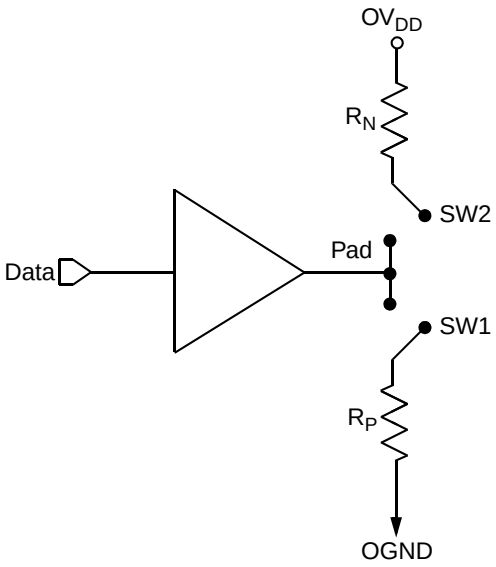


Figure 57. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD}, nominal OV_{DD}, 105° C.

Table 79. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	20 Target	Z_0	W
R_P	42 Target	25 Target	20 Target	Z_0	W
Differential	NA	NA	NA	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, T_J = 105° C.

23.6 Configuration Pin Muxing

The device provides the user with power-on configuration options that can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.