NXP USA Inc. - <u>MPC8360EZUAHFH Datasheet</u>





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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8360ezuahfh

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DC Electrical Characteristics



4.1 DC Electrical Characteristics

This table provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the device.

|--|

Parameter	Condition	Symbol	Min	Мах	Unit
Input high voltage	—	V _{IH}	2.7	OV _{DD} + 0.3	V
Input low voltage	—	V _{IL}	-0.3	0.4	V
CLKIN input current	0 V ≤V _{IN} ≤OV _{DD}	I _{IN}	—	±10	μA
PCI_SYNC_IN input current	0 V ≤V _{IN} ≤0.5V or OV _{DD} – 0.5V ≤V _{IN} ≤OV _{DD}	I _{IN}	_	±10	μΑ
PCI_SYNC_IN input current	0.5 V ≤V _{IN} ≤OV _{DD} – 0.5 V	I _{IN}	—	±100	μA

4.2 AC Electrical Characteristics

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 8.	CLKIN	AC	Timing	Specifications
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Parameter/Condition	Symbol	Min	Typical	Мах	Unit	Notes
CLKIN/PCI_CLK frequency	f _{CLKIN}	—	—	66.67	MHz	1
CLKIN/PCI_CLK cycle time	t _{CLKIN}	15	—	_	ns	—
CLKIN/PCI_CLK rise and fall time	t _{KH} , t _{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t _{KHK} /t _{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	±150	ps	4, 5

Notes:

- 1. **Caution:** The system, core, USB, security, and 10/100/1000 Ethernet must not exceed their respective maximum or minimum operating frequencies.
- 2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 V and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the total input jitter-short term and long term-and is guaranteed by design.
- 5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.

4.3 Gigabit Reference Clock Input Timing

This table provides the Gigabit reference clocks (GTX_CLK125) AC timing specifications.

Table 9. GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 \pm 0.125 mV/ 3.3 V \pm 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
GTX_CLK125 frequency	t _{G125}	_	125	_	MHz	_
GTX_CLK125 cycle time	t _{G125}	_	8		ns	



6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the device when $GV_{DD}(typ) = 1.8 \text{ V}.$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV _{DD}	1.71	1.89	V	1
I/O reference voltage	MV _{REF}	$0.49 imes \text{GV}_{\text{DD}}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.125	GV _{DD} + 0.3	V	_
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.125	V	_
Output leakage current	I _{OZ}	_	±10	μA	4
Output high current (V _{OUT} = 1.420 V)	I _{OH}	-13.4	—	mA	
Output low current (V _{OUT} = 0.280 V)	I _{OL}	13.4	—	mA	
MV _{REF} input leakage current	I _{VREF}	_	±10	μA	
Input current (0 V ≰⁄ _{IN} ≤OV _{DD})	I _{IN}	—	±10	μA	_

Table 14. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.

 MV_{REF} is expected to equal 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} cannot exceed ±2% of the DC value.

 V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to equal MV_{REF}. This rail should track variations in the DC level of MV_{REF}.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

This table provides the DDR2 capacitance when $GV_{DD}(typ) = 1.8$ V.

Table 15. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) of the device when $GV_{DD}(typ) = 2.5 \text{ V}.$

Table 16. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	GV _{DD}	2.375	2.625	V	1
I/O reference voltage	MV _{REF}	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} - 0.04	MV _{REF} + 0.04	V	3



DDR and DDR2 SDRAM AC Electrical Characteristics

This figure provides the AC test load for the DDR bus.



Figure 8. DDR AC Test Load

Table 22. DDR and DDR2 SDRAM Measurement Conditions

Symbol	DDR	DDR2	Unit	Notes
V _{TH}	MV _{REF} ± 0.31 V	MV _{REF} ± 0.25 V	V	1
V _{OUT}	$0.5 \times \text{ GV}_{\text{DD}}$	$0.5 \times \text{ GV}_{\text{DD}}$	V	2

Notes:

1. Data input threshold measurement point.

2. Data output measurement point.

This figure shows the DDR SDRAM output timing diagram for source synchronous mode.



Figure 9. DDR SDRAM Output Timing Diagram for Source Synchronous Mode



GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

8.2.1.2 GMII Receive AC Timing Specifications

This table provides the GMII receive AC timing specifications.

Table 28. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
RX_CLK clock period	t _{GRX}	_	8.0	—	ns	_
RX_CLK duty cycle	t _{GRXH} /t _{GRX}	40		60	%	—
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{GRDVKH}	2.0		—	ns	—
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t _{GRDXKH}	0.2		—	ns	2
RX_CLK clock rise time, (20% to 80%)	t _{GRXR}	_		1.0	ns	—
RX_CLK clock fall time, (80% to 20%)	t _{GRXF}	_	_	1.0	ns	—

Notes:

- 1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- In rev. 2.0 silicon, due to errata, t_{GRDXKH} minimum is 0.5 which is not compliant with the standard. Refer to Errata QE_ENET18 in Chip Errata for the MPC8360E, Rev. 1.

This figure shows the GMII receive AC timing diagram.



Figure 11. GMII Receive AC Timing Diagram



8.2.4.1 TBI Transmit AC Timing Specifications

This table provides the TBI transmit AC timing specifications.

Table 33. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
GTX_CLK clock period	t _{TTX}	_	8.0	_	ns	—
GTX_CLK duty cycle	t _{TTXH} /t _{TTX}	40	—	60	%	—
GTX_CLK to TBI data TCG[9:0] delay	t _{TTKHDX} t _{TTKHDV}	1.0	—	 5.0	ns	3
GTX_CLK clock rise time, (20% to 80%)	t _{TTXR}	_	—	1.0	ns	—
GTX_CLK clock fall time, (80% to 20%)	t _{TTXF}	_	_	1.0	ns	—
GTX_CLK125 reference clock period	t _{G125}	_	8.0	_	ns	2
GTX_CLK125 reference clock duty cycle	t _{G125H} /t _{G125}	45	—	55	ns	—

Notes:

- The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- 2. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
- 3. In rev. 2.0 silicon, due to errata, t_{TTKHDX} minimum is 0.7 ns for UCC1. Refer to Errata QE_ENET19 in Chip Errata for the MPC8360E, Rev. 1.

This figure shows the TBI transmit AC timing diagram.



Figure 18. TBI Transmit AC Timing Diagram



Ethernet Management Interface Electrical Characteristics

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.



Figure 20. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI, and RTBI are specified in Section 8.1, "Three-Speed Ethernet Controller (10/100/1000 Mbps)— GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage (3.3 V)	OV _{DD}	—		2.97	3.63	V
Output high voltage	V _{OH}	$I_{OH} = -1.0 \text{ mA}$	$OV_{DD} = Min$	2.10	OV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	$OV_{DD} = Min$	GND	0.50	V
Input high voltage	V _{IH}	—		2.00	—	V
Input low voltage	V _{IL}	—		—	0.80	V
Input current	I _{IN}	0 V ≤V _{IN} ≤OV _{DD}		—	±10	μA

Table 36. MII Management DC Electrica	I Characteristics When Powered at 3.3 V
---------------------------------------	---



8.3.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 37. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC frequency	f _{MDC}	—	2.5	—	MHz	2
MDC period	t _{MDC}	—	400	—	ns	—
MDC clock pulse width high	t _{MDCH}	32	—	—	ns	_
MDC to MDIO delay	^t мрткнрх ^t мрткнрv	10 —	_	 110	ns	3
MDIO to MDC setup time	t _{MDRDVKH}	10	—	—	ns	—
MDIO to MDC hold time	t _{MDRDXKH}	0	—	—	ns	—
MDC rise time	t _{MDCR}	—	—	10	ns	—
MDC fall time	t _{MDHF}	_	_	10	ns	

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDRDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
 </sub>
- This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
- 3. This parameter is dependent on the ce_clk speed (that is, for a ce_clk of 200 MHz, the delay is 90 ns and for a ce_clk of 300 MHz, the delay is 63 ns).

This figure shows the MII management AC timing diagram.



Figure 21. MII Management Interface Timing Diagram



Local Bus DC Electrical Characteristics

8.3.3 IEEE 1588 Timer AC Specifications

This table provides the IEEE 1588 timer AC specifications.

Table 38. IEEE 1588 Timer AC Specifications

Parameter	Symbol	Min	Мах	Unit	Notes
Timer clock frequency	t _{TMRCK}	0	70	MHz	1
Input setup to timer clock	t _{TMRCKS}	—	—	—	2, 3
Input hold from timer clock	t _{TMRCKH}	—	—	—	2, 3
Output clock to output valid	t _{GCLKNV}	0	6	ns	_
Timer alarm to output valid	t _{TMRAL}	_		_	2

Notes:

1. The timer can operate on rtc_clock or tmr_clock. These clocks get muxed and any one of them can be selected. The minimum and maximum requirement for both rtc_clock and tmr_clock are the same.

- 2. These are asynchronous signals.
- 3. Inputs need to be stable at least one TMR clock.

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8360E/58E.

9.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface.

Table 39. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
High-level output voltage, I _{OH} = −100 μA	V _{OH}	OV _{DD} - 0.4	—	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V _{OL}	—	0.2	V
Input current	I _{IN}	—	±10	μA

9.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface of the device.

Table 40. Local Bus General Timing Parameters—DLL Enabled

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus cycle time	t _{LBK}	7.5	_	ns	2
Input setup to local bus clock (except LUPWAIT)	t _{LBIVKH1}	1.7	_	ns	3, 4
LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.9	_	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	t _{LBIXKH1}	1.0		ns	3, 4



These figures show the local bus signals.



Figure 24. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)



This figure provides the test access port timing diagram.



VM = Midpoint Voltage (OV_{DD}/2)

Figure 33. Test Access Port Timing Diagram

11 I²C

This section describes the DC and AC electrical characteristics for the I^2C interface of the MPC8360E/58E.

11.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I^2C interface of the device.

Table 44. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V _{IH}	$0.7 imes OV_{DD}$	OV _{DD} + 0.3	V	—
Input low voltage level	V _{IL}	-0.3	$0.3 imes OV_{DD}$	V	—
Low level output voltage	V _{OL}	0	0.4	V	1
Output fall time from $V_{IH}(\text{min})$ to $V_{IL}(\text{max})$ with a bus capacitance from 10 to 400 pF	^t I2KLKV	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t _{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	CI	_	10	pF	—
Input current (0 V ≤V _{IN} ≤OV _{DD})	I _{IN}		±10	μA	4

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.

- 2. C_B = capacitance of one bus line in pF.
- 3. Refer to the MPC8360E Integrated Communications Processor Reference Manual for information on the digital filter used.
- 4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

PCI AC Electrical Specifications

Table 47. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Clock to output high impedance	t _{PCKHOZ}	_	14	ns	2, 3
Input setup to clock	t _{PCIVKH}	3.0	_	ns	2, 4
Input hold from clock	t _{PCIXKH}	0.3	_	ns	2, 4, 6

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
 </sub>
- 2. See the timing measurement conditions in the PCI 2.2 Local Bus Specifications.
- 3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.
- 5. In rev. 2.0 silicon, due to errata, t_{PCIHOV} maximum is 6.6 ns. Refer to Errata PCI21 in Chip Errata for the MPC8360E, Rev. 1.
- 6. In rev. 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Refer to Errata PCI17 in Chip Errata for the MPC8360E, Rev. 1.

Table 48. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	t _{PCKHOV}	_	11	ns	2
Output hold from clock	t _{PCKHOX}	2	-	ns	2
Clock to output high impedance	t _{PCKHOZ}	_	14	ns	2, 3
Input setup to clock	t _{PCIVKH}	7.0	_	ns	2, 2
Input hold from clock	t _{PCIXKH}	0.3	_	ns	2, 4, 5

Notes:

- The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
- 2. See the timing measurement conditions in the PCI 2.2 Local Bus Specifications.
- 3. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 4. Input timings are measured at the pin.
- 5. In rev. 2.0 silicon, due to errata, t_{PCIXKH} minimum is 1 ns. Refer to Errata PCI17 in Chip Errata for the MPC8360E, Rev. 1.

This figure provides the AC test load for PCI.



Figure 36. PCI AC Test Load



HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

This figure shows the UTOPIA timing with internal clock.





18 HDLC, BISYNC, Transparent, and Synchronous UART

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent, and synchronous UART protocols of the MPC8360E/58E.

18.1 HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

This table provides the DC electrical characteristics for the device HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 61. HDLC, BISYNC,	Transparent, and Synchronous UART DC Electrical Characteristics
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Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V _{OH}	I _{OH} = -2.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.5	V
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	0 V ≤V _{IN} ≤OV _{DD}	—	±10	μA

18.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

These tables provide the input and output AC timing specifications for HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 62. HDLC, BISYNC, and Transparent AC Timing Specifications¹

Characteristic	Symbol ²	Min	Мах	Unit
Outputs—Internal clock delay	t _{HIKHOV}	0	11.2	ns
Outputs—External clock delay	t _{HEKHOV}	1	10.8	ns



Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_DEVSEL/CE_PF[16]	E26	I/O	OV _{DD}	5
PCI_IDSEL/CE_PF[17]	F22	I/O	OV _{DD}	
PCI_SERR/CE_PF[18]	B29	I/O	OV _{DD}	5
PCI_PERR/CE_PF[19]	A29	I/O	OV _{DD}	5
PCI_REQ[0]/CE_PF[20]	F19	I/O	LV _{DD} 2	—
PCI_REQ[1]/CPCI_HS_ES/ CE_PF[21]	A21	I/O	LV _{DD} 2	—
PCI_REQ[2]/CE_PF[22]	C21	I/O	LV _{DD} 2	
PCI_GNT[0]/CE_PF[23]	E20	I/O	LV _{DD} 2	
PCI_GNT[1]/CPCI1_HS_LED/ CE_PF[24]	B20	I/O	LV _{DD} 2	_
PCI_GNT[2]/CPCI1_HS_ENUM/ CE_PF[25]	C20	I/O	LV _{DD} 2	
PCI_MODE	D36	I	OV _{DD}	
M66EN/CE_PF[4]	B37	I/O	OV _{DD}	—
	Local Bus Controller Interface			
LAD[0:31]	N32, N33, N35, N36, P37, P32, P34, R36, R35, R34, R33, T37, T35, T34, T33, U37, T32, U36, U34, V36, V35, W37, W35, V33, V32, W34, Y36, W32, AA37, Y33, AA35, AA34	I/O	OV _{DD}	_
LDP[0]/CKSTOP_OUT	AB37	I/O	OV _{DD}	
LDP[1]/CKSTOP_IN	AB36	I/O	OV _{DD}	
LDP[2]/LCS[6]	AB35	I/O	OV _{DD}	
LDP[3]/LCS[7]	AA33	I/O	OV _{DD}	
LA[27:31]	AC37, AA32, AC36, AC34, AD36	0	OV _{DD}	
LCS[0:5]	AD33, AG37, AF34, AE33, AD32, AH37	0	OV_{DD}	
LWE[0:3]/LSDDQM[0:3]/LBS[0:3]	AG35, AG34, AH36, AE32	0	OV_{DD}	
LBCTL	AD35	0	OV_{DD}	
LALE	M37	0	OV_{DD}	
LGPL0/LSDA10/cfg_reset_source0	AB32	I/O	OV_{DD}	
LGPL1/LSDWE/cfg_reset_source1	AE37	I/O	OV_{DD}	
LGPL2/LSDRAS/LOE	AC33	0	OV_{DD}	
LGPL3/LSDCAS/cfg_reset_source2	AD34	I/O	OV _{DD}	
LGPL4/LGTA/LUPWAIT/LPBSE	AE35	I/O	OV_{DD}	
LGPL5/cfg_clkin_div	AF36	I/O	OV_{DD}	
LCKE	G36	0	OV _{DD}	_
LCLK[0]	J33	0	OV _{DD}	—
LCLK[1]/LCS[6]	J34	0	OV _{DD}	—



Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MWE	AT26	0	GV _{DD}	—
MEMC_MRAS	AT29	0	GV _{DD}	—
MEMC_MCAS	AT24	0	GV _{DD}	—
MEMC_MCS[0:3]	AU27, AT27, AU8, AU7	0	GV _{DD}	—
MEMC_MCKE[0:1]	AL32, AU33	0	GV _{DD}	3
MEMC_MCK[0:5]	AK37, AT37, AN1, AR2, AN25, AK1	0	GV _{DD}	—
MEMC_MCK[0:5]	AL37, AT36, AP2, AT2, AN24, AL1	0	GV _{DD}	—
MDIC[0:1]	AH6, AP30	I/O	GV _{DD}	11
	PCI			
PCI_INTA/IRQ_OUT/CE_PF[5]	A20	I/O	LV _{DD} 2	2
PCI_RESET_OUT/CE_PF[6]	E19	I/O	LV _{DD} 2	—
PCI_AD[31:30]/CE_PG[31:30]	D20, D21	I/O	LV _{DD} 2	—
PCI_AD[29:25]/CE_PG[29:25]	A24, B23, C23, E23, A26	I/O	OV _{DD}	—
PCI_AD[24]/CE_PG[24]	B21	I/O	LV _{DD} 2	—
PCI_AD[23:0]/CE_PG[23:0]	C24, C25, D25, B25, E24, F24, A27, A28, F27, A30, C30, D30, E29, B31, C31, D31, D32, A32, C33, B33, F30, E31, A34, D33	I/O	OV _{DD}	—
PCI_C/BE[3:0]/CE_PF[10:7]	E22, B26, E28, F28	I/O	OV _{DD}	—
PCI_PAR/CE_PF[11]	D28	I/O	OV _{DD}	—
PCI_FRAME/CE_PF[12]	D26	I/O	OV _{DD}	5
PCI_TRDY/CE_PF[13]	C27	I/O	OV _{DD}	5
PCI_IRDY/CE_PF[14]	C28	I/O	OV _{DD}	5
PCI_STOP/CE_PF[15]	B28	I/O	OV _{DD}	5
PCI_DEVSEL/CE_PF[16]	E26	I/O	OV _{DD}	5
PCI_IDSEL/CE_PF[17]	F22	I/O	OV _{DD}	_
PCI_SERR/CE_PF[18]	B29	I/O	OV _{DD}	5
PCI_PERR/CE_PF[19]	A29	I/O	OV _{DD}	5
PCI_REQ[0]/CE_PF[20]	F19	I/O	LV _{DD} 2	—
PCI_REQ[1]/CPCI_HS_ES/ CE_PF[21]	A21	I/O	LV _{DD} 2	-
PCI_REQ[2]/CE_PF[22]	C21	I/O	LV _{DD} 2	—
PCI_GNT[0]/CE_PF[23]	E20	I/O	LV _{DD} 2	—
PCI_GNT[1]/CPCI1_HS_LED/ CE_PF[24]	B20	I/O	LV _{DD} 2	—
PCI_GNT[2]/CPCI1_HS_ENUM/ CE_PF[25]	C20	I/O	LV _{DD} 2	_



Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes		
IRQ[4:5]	G33, G32	I/O	OV _{DD}	—		
IRQ[6]/LCS[6]/CKSTOP_OUT	E35	I/O	OV _{DD}	—		
IRQ[7]/LCS[7]/CKSTOP_IN	H36	I/O	OV _{DD}	—		
	DUART					
UART1_SOUT/M1SRCID[0]/ M2SRCID[0]/LSRCID[0]	E32	0	OV _{DD}	_		
UART1_SIN/M1SRCID[1]/ M2SRCID[1]/LSRCID[1]	B34	I/O	OV _{DD}			
UART1_CTS/M1SRCID[2]/ M2SRCID[2]/LSRCID[2]	C34	I/O	OV _{DD}			
UART1_RTS/M1SRCID[3]/ M2SRCID[3]/LSRCID[3]	A35	0	OV _{DD}	_		
	I ² C Interface			<u></u>		
IIC1_SDA	D34	I/O	OV _{DD}	2		
IIC1_SCL	B35	I/O	OV _{DD}	2		
IIC2_SDA	E33	I/O	OV _{DD}	2		
IIC2_SCL	C35	I/O	OV _{DD}	2		
QUICC Engine						
CE_PA[0]	F8	I/O	LV _{DD0}	—		
CE_PA[1:2]	AH1, AG5	I/O	OV _{DD}	—		
CE_PA[3:7]	F6, D4, C3, E5, A3	I/O	LV _{DD} 0	—		
CE_PA[8]	AG3	I/O	OV _{DD}	—		
CE_PA[9:12]	F7, B3, E6, B4	I/O	LV _{DD} 0	—		
CE_PA[13:14]	AG1, AF6	I/O	OV _{DD}	—		
CE_PA[15]	B2	I/O	LV _{DD} 0	—		
CE_PA[16]	AF4	I/O	OV _{DD}	—		
CE_PA[17:21]	B16, A16, E17, A17, B17	I/O	LV _{DD} 1	—		
CE_PA[22]	AF3	I/O	OV _{DD}	—		
CE_PA[23:26]	C18, D18, E18, A18	I/O	LV _{DD} 1	—		
CE_PA[27:28]	AF2, AE6	I/O	OV _{DD}	—		
CE_PA[29]	B19	I/O	LV _{DD} 1	—		
CE_PA[30]	AE5	I/O	OV_{DD}	—		
CE_PA[31]	F16	I/O	LV _{DD} 1	—		



Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	No Connect			
NC	AM16, AM17, AM20, AN13, AN16, AN17, AP10, AP11, AP13, AP15, AP18, AR11, AR13, AR14, AR15, AR16, AR17, AR20, AT11, AT12, AT13, AT14, AT16, AT17, AT18, AU10, AU11, AU12, AU13, AU15, AU19	_	_	

Notes:

- 1. This pin is an open drain signal. A weak pull-up resistor (1 k Ω) should be placed on this pin to OV_{DD}.
- 2. This pin is an open drain signal. A weak pull-up resistor (2–10 k Ω) should be placed on this pin to OV_{DD} .
- 3. This output is actively driven during reset rather than being three-stated during reset.
- 4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- 5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
- 6. These are On Die Termination pins, used to control DDR2 memories internal termination resistance.
- 7. This pin must always be tied to GND.
- 8. This pin must always be left not connected.
- 9. Refer to MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual section on "RGMII Pins," for information about the two UCC2 Ethernet interface options.
- 10. This pin must always be tied to GV_{DD} .
- 11. It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor for DDR2.



Pinout Listings

clock. When the device is configured as a PCI agent device the CLKIN and the CFG_CLKIN_DIV signals should be tied to GND.

When the device is configured as a PCI host device (RCWH[PCIHOST] = 1) and PCI clock output is disabled (RCWH[PCICKDRV] = 0), clock distribution and balancing done externally on the board. Therefore, PCI_SYNC_IN is the primary input clock.

As shown in Figure 54 and Figure 55, the primary clock input (frequency) is multiplied by the QUICC Engine block phase-locked loop (PLL), the system PLL, and the clock unit to create the QUICC Engine clock (ce_clk), the coherent system bus clock (csb_clk), the internal DDRC1 controller clock ($ddr1_clk$), and the internal clock for the local bus interface unit and DDR2 memory controller (lb_clk).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb_clk = \{PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)\} \times SPMF$$

In PCI host mode, PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV) is the CLKIN frequency; in PCI agent mode, CFG_CLKIN_DIV must be pulled down (low), so PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV) is the PCI_CLK frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, "Reset, Clocking, and Initialization," in the *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more information on the clock subsystem.

The *ce_clk* frequency is determined by the QUICC Engine PLL multiplication factor (RCWL[CEPMF) and the QUICC Engine PLL division factor (RCWL[CEPDF]) according to the following equation:

 $ce_clk = (primary clock input \times CEPMF) \div (1 + CEPDF)$

The internal *ddr1_clk* frequency is determined by the following equation:

 $ddr1_clk = csb_clk \times (1 + RCWL[DDR1CM])$

Note that the lb_clk clock frequency (for DDRC2) is determined by RCWL[LBCM]. The *internal ddr1_clk* frequency is not the external memory bus frequency; *ddr1_clk* passes through the DDRC1 clock divider (\div 2) to create the differential DDRC1 memory bus clock outputs (MEMC1_MCK and MEMC1_MCK). However, the data rate is the same frequency as *ddr1_clk*.

The internal *lb_clk* frequency is determined by the following equation:

 $lb_clk = csb_clk \times (1 + \text{RCWL[LBCM]})$

Note that *lb_clk* is not the external local bus or DDRC2 frequency; *lb_clk* passes through the a LB clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LB clock divider ratio is controlled by LCRR[CLKDIV].

Additionally, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. This table specifies which units have a configurable clock frequency.

Unit	Default Frequency	Options
Security core	csb_clk/3	Off, <i>csb_clk</i> ¹ , <i>csb_clk</i> /2, <i>csb_clk</i> /3
PCI and DMA complex	csb_clk	Off, <i>csb_clk</i>

Table 68	Configurable	Clock	Units
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¹ With limitation, only for slow csb_clk rates, up to 166 MHz.

This table provides the operating frequencies for the TBGA package under recommended operating conditions (see Table 2). All frequency combinations shown in the table below may not be available. Maximum operating frequencies depend on the part





ordered, see Section 24.1, "Part Numbers Fully Addressed by this Document," for part ordering details and contact your Freescale sales representative or authorized distributor for more information.

Characteristic ¹	400 MHz	400 MHz 533 MHz		Unit
e300 core frequency (<i>core_clk</i>)	266–400	266–533	266–667	MHz
Coherent system bus frequency (<i>csb_clk</i>)			MHz	
QUICC Engine frequency ³ (<i>ce_clk</i>)	266–500			MHz
DDR and DDR2 memory bus frequency (MCLK) ⁴		MHz		
Local bus frequency (LCLK <i>n</i>) ⁵			MHz	
PCI input frequency (CLKIN or PCI_CLK)	25–66.67		MHz	
Security core maximum internal operating frequency	133	133	166	MHz

Table 69. Operating Frequencies for the TBGA Package

Notes:

- 1. The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCLK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
- 2. The 667 MHz core frequency is based on a 1.3 V V_{DD} supply voltage.
- 3. The 500 MHz QE frequency is based on a 1.3 V V_{DD} supply voltage.
- 4. The DDR data rate is 2x the DDR memory bus frequency.
- 5. The local bus frequency is 1/2, 1/4, or 1/8 of the *lb_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWL[LBCM]).

21.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] and RCWL[SVCOD] parameters. This table shows the multiplication factor encodings for the system PLL.

RCWL[SPMF]	System PLL Multiplication Factor
0000	× 16
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11

Table 70. System PLL Multiplication Factors



System PLL Configuration

			Input Clock Frequency (MHz) ²) ²
CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0110	6:1	100	150	200	
Low	0111	7:1	116	175	233	
Low	1000	8:1	133	200	266	
Low	1001	9:1	150	225	300	
Low	1010	10:1	166	250	333	
Low	1011	11:1	183	275		
Low	1100	12:1	200	300		
Low	1101	13:1	216	325		
Low	1110	14:1	233		-	
Low	1111	15:1	250			
Low	0000	16:1	266			
High	0010	2:1		-		133
High	0011	3:1			100	200
High	0100	4:1			133	266
High	0101	5:1			166	333
High	0110	6:1			200	
High	0111	7:1			233	
High	1000	8:1				
High	1001	9:1				
High	1010	10:1				
High	1011	11:1				
High	1100	12:1				
High	1101	13:1				
High	1110	14:1				
High	1111	15:1				
High	0000	16:1				

Table 72. CSB Frequency Options (continued)

¹ CFG_CLKIN_DIV is only used for host mode; CLKIN must be tied low and CFG_CLKIN_DIV must be pulled down (low) in agent mode.

 $^2\,$ CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.



22.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

 T_I = junction temperature (° C)

 T_C = case temperature of the package (° C)

 $R_{\theta JC}$ = junction to case thermal resistance (° C/W)

 P_D = power dissipation (W)

23 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8360E/58E. Additional information can be found in *MPC8360E/MPC8358E PowerQUICC Design Checklist* (AN3097).

23.1 System Clocking

The device includes two PLLs, as follows.

- The platform PLL (AV_{DD}1) generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in Section 21.1, "System PLL Configuration."
- The e300 core PLL (AV_{DD}2) generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 21.2, "Core PLL Configuration."

23.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD} 1, AV_{DD} 2, respectively). The AV_{DD} level should always be equivalent to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in Figure 56, one to each of the five AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.