NXP USA Inc. - <u>MPC8360EZUAJDG Datasheet</u>





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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Communications; QUICC Engine, Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8360ezuajdg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



This figure shows the MPC8358E block diagram.



Figure 2. MPC8358E Block Diagram

Major features of the MPC8360E/58E are as follows:

- e300 PowerPC processor core (enhanced version of the MPC603e core)
 - Operates at up to 667 MHz (for the MPC8360E) and 400 MHz (for the MPC8358E)
 - High-performance, superscalar processor core
 - Floating-point, integer, load/store, system register, and branch processing units
 - 32-Kbyte instruction cache, 32-Kbyte data cache
 - Lockable portion of L1 cache
 - Dynamic power management
 - Software-compatible with the Freescale processor families implementing the Power Architecture[™] technology
- QUICC Engine unit
 - Two 32-bit RISC controllers for flexible support of the communications peripherals, each operating up to 500 MHz (for the MPC8360E) and 400 MHz (for the MPC8358E)
 - Serial DMA channel for receive and transmit on all serial channels
 - QUICC Engine module peripheral request interface (for SEC, PCI, IEEE Std. 1588TM)
 - Eight universal communication controllers (UCCs) on the MPC8360E and six UCCs on the MPC8358E supporting the following protocols and interfaces (not all of them simultaneously):
 - IEEE 1588 protocol supported



Power Sequencing

This figure shows the undershoot and overshoot voltage of the PCI interface of the device for the 3.3-V signals, respectively.



Figure 4. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	OV _{DD} = 3.3 V
PCI signals	25	
PCI output clocks (including PCI_SYNC_OUT)	42	
DDR signal	20 36 (half-strength mode) ¹	GV _{DD} = 2.5 V
DDR2 signal	18 36 (half-strength mode) ¹	GV _{DD} = 1.8 V
10/100/1000 Ethernet signals	42	LV _{DD} = 2.5/3.3 V
DUART, system control, I ² C, SPI, JTAG	42	OV _{DD} = 3.3 V
GPIO signals	42	OV _{DD} = 3.3 V LV _{DD} = 2.5/3.3 V

Note:

1. DDR output impedance values for half strength mode are verified by design and not tested.

2.2 Power Sequencing

This section details the power sequencing considerations for the MPC8360E/58E.



Power Sequencing

This table shows the estimated typical I/O power dissipation for the device.

Interface	Parameter	GV _{DD} (1.8 V)	GV _{DD} (2.5 V)	OV _{DD} (3.3 V)	LV _{DD} (3.3 V)	LV _{DD} (2.5 V)	Unit	Comments
DDR I/O	200 MHz, 1 \times 32 bits	0.3	0.46	_	_	—	W	—
$R_s = 20 \Omega$	200 MHz, 1 \times 64 bits	0.4	0.58			—	W	—
$R_t = 50 \Omega$	200 MHz, 2×32 bits	0.6	0.92	_	_	—	W	_
	266 MHz, 1 \times 32 bits	0.35	0.56	_	_	—	W	_
	266 MHz, 1 \times 64 bits	0.46	0.7	_	_	—	W	_
	266 MHz, 2×32 bits	0.7	1.11		—	—	W	_
	333 MHz, 1 \times 32 bits	0.4	0.65	_	_	—	W	_
	333 MHz, 1 \times 64 bits	0.53	0.82		—	—	W	_
	333 MHz, 2×32 bits	0.81	1.3		—	—	W	_
Local Bus I/O	133 MHz, 32 bits	—	—	0.22	_	_	W	_
3 pairs of clocks	83 MHz, 32 bits	—	—	0.14	—	—	W	—
	66 MHz, 32 bits	—	—	0.12	—	—	W	_
	50 MHz, 32 bits	—	—	0.09	—	—	W	_
PCI I/O	33 MHz, 32 bits	—	—	0.05	—	—	W	_
Load = 30 pF	66 MHz, 32 bits	—	—	0.07	—	—	W	—
10/100/1000	MII or RMII	—	—	_	0.01	—	W	Multiply by
Load = 20 pF	GMII or TBI	—	— — — 0.04 — W inte	interfaces used.				
	RGMII or RTBI	—	—	—	—	0.04	W	
Other I/O	_	—	_	0.1	—	—	W	—

Table 6. Estimated Typical I/O Power Dissipation

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8360E/58E.

NOTE

The rise/fall time on QUICC Engine block input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of V_{DD} ; fall time refers to transitions from 90% to 10% of V_{DD} .



6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the device when $GV_{DD}(typ) = 1.8 \text{ V}.$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV _{DD}	1.71	1.89	V	1
I/O reference voltage	MV _{REF}	$0.49 imes \text{GV}_{\text{DD}}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.125	GV _{DD} + 0.3	V	_
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.125	V	_
Output leakage current	I _{OZ}	_	±10	μA	4
Output high current (V _{OUT} = 1.420 V)	I _{OH}	-13.4	—	mA	
Output low current (V _{OUT} = 0.280 V)	I _{OL}	13.4	—	mA	
MV _{REF} input leakage current	I _{VREF}	_	±10	μA	
Input current (0 V ≰⁄ _{IN} ≤OV _{DD})	I _{IN}	—	±10	μA	_

Table 14. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.

 MV_{REF} is expected to equal 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} cannot exceed ±2% of the DC value.

 V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to equal MV_{REF}. This rail should track variations in the DC level of MV_{REF}.

4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

This table provides the DDR2 capacitance when $GV_{DD}(typ) = 1.8$ V.

Table 15. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, DQS	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) of the device when $GV_{DD}(typ) = 2.5 \text{ V}.$

Table 16. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	GV _{DD}	2.375	2.625	V	1
I/O reference voltage	MV _{REF}	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} - 0.04	MV _{REF} + 0.04	V	3



8.2.1.1 GMII Transmit AC Timing Specifications

This table provides the GMII transmit AC timing specifications.

Table 27. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
GTX_CLK clock period	t _{GTX}	_	8.0		ns	_
GTX_CLK duty cycle	t _{GTXH/tGTX}	40	_	60	%	—
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	^t GTKHDX ^t GTKHDV	0.5	_	 5.0	ns	3
GTX_CLK clock rise time, (20% to 80%)	t _{GTXR}	_		1.0	ns	_
GTX_CLK clock fall time, (80% to 20%)	t _{GTXF}	_	_	1.0	ns	—
GTX_CLK125 clock period	t _{G125}	_	8.0	_	ns	2
GTX_CLK125 reference clock duty cycle measured at $LV_{DD/2}$	t _{G125H} /t _{G125}	45		55	%	2

Notes:

- 1. The symbols used for timing specifications follow the pattern t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{ignx} clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- 2. This symbol is used to represent the external GTX_CLK125 signal and does not follow the original symbol naming convention.
- In rev. 2.0 silicon, due to errata, t_{GTKHDX} minimum and t_{GTKHDV} maximum are not supported when the GTX_CLK is selected. Refer to Errata QE_ENET18 in Chip Errata for the MPC8360E, Rev. 1.

This figure shows the GMII transmit AC timing diagram.



Figure 10. GMII Transmit AC Timing Diagram



8.2.5 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 35. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
Data to clock output skew (at transmitter)	t _{SKRGTKHDX} t _{SKRGTKHDV}	-0.5 		— 0.5	ns	7
Data to clock input skew (at receiver)	t _{SKRGDXKH} t _{SKRGDVKH}	1.0		 2.6	ns	2
Clock cycle duration	t _{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	t _{RGTH} /t _{RGT}	45	50	55	%	4, 5
Duty cycle for 10BASE-T and 100BASE-TX	t _{RGTH} /t _{RGT}	40	50	60	%	3, 5
Rise time (20–80%)	t _{RGTR}	—		0.75	ns	
Fall time (20–80%)	t _{RGTF}	—	_	0.75	ns	
GTX_CLK125 reference clock period	t _{G125}	—	8.0	_	ns	6
GTX_CLK125 reference clock duty cycle	t _{G125H} /t _{G125}	47		53	%	

Notes:

- Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (Rx) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- 2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns can be added to the associated clock signal.
- 3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
- 4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- 5. Duty cycle reference is LV_{DD}/2.
- 6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
- 7. In rev. 2.0 silicon, due to errata, t_{SKRGTKHDX} minimum is –2.3 ns and t_{SKRGTKHDV} maximum is 1 ns for UCC1, 1.2 ns for UCC2 option 1, and 1.8 ns for UCC2 option 2. In rev. 2.1 silicon, due to errata, t_{SKRGTKHDX} minimum is –0.65 ns for UCC2 option 1 and –0.9 for UCC2 option 2, and t_{SKRGTKHDV} maximum is 0.75 ns for UCC1 and UCC2 option 1 and 0.85 for UCC2 option 2. Refer to Errata QE_ENET10 in *Chip Errata for the MPC8360E, Rev. 1*. UCC1 does meet t_{SKRGTKHDX} minimum for rev. 2.1 silicon.

Local Bus AC Electrical Specifications

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to output valid	t _{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ}		4	ns	8

Table 41. Local Bus General Timing Parameters—DLL Bypass Mode⁹ (continued)

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the to the output (O) going invalid (X) or output hold time.
 </sub>
- 2. All timings are in reference to falling edge of LCLK0 (for all outputs and for LGTA and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
- 3. All signals are measured from OV_{DD}/2 of the rising/falling edge of LCLK0 to 0.4 × OV_{DD} of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. t_{LBOTOT1} should be used when RCWH[LALE] is not set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- t_{LBOTOT2} should be used when RCWH[LALE] is set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- 7. t_{LBOTOT3} should be used when RCWH[LALE] is set and when the load on LALE output pin equals to the load on LAD output pins.
- 8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 9. DLL bypass mode is not recommended for use at frequencies above 66 MHz.

This figure provides the AC test load for the local bus.



Figure 22. Local Bus C Test Load



These figures show the local bus signals.



Figure 24. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)





Figure 27. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (DLL Bypass Mode)



JTAG DC Electrical Characteristics



Figure 28. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (DLL Enabled)

10 JTAG

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8360E/58E.

10.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface of the device.

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V _{OH}	I _{OH} = -6.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	—	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V
Input high voltage	V _{IH}	—	2.5	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	$0 V \leq V_{IN} \leq OV_{DD}$	_	±10	μA



This figure provides the test access port timing diagram.



VM = Midpoint Voltage (OV_{DD}/2)

Figure 33. Test Access Port Timing Diagram

11 I²C

This section describes the DC and AC electrical characteristics for the I^2C interface of the MPC8360E/58E.

11.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I^2C interface of the device.

Table 44. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 10%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V _{IH}	$0.7 imes OV_{DD}$	OV _{DD} + 0.3	V	—
Input low voltage level	V _{IL}	-0.3	$0.3 imes OV_{DD}$	V	—
Low level output voltage	V _{OL}	0	0.4	V	1
Output fall time from $V_{IH}(\text{min})$ to $V_{IL}(\text{max})$ with a bus capacitance from 10 to 400 pF	^t I2KLKV	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t _{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	CI	_	10	pF	—
Input current (0 V ≤V _{IN} ≤OV _{DD})	I _{IN}		±10	μA	4

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.

- 2. C_B = capacitance of one bus line in pF.
- 3. Refer to the MPC8360E Integrated Communications Processor Reference Manual for information on the digital filter used.
- 4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.





14.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 52. GPIO Input AC Timing Specifications¹

Characteristic	Symbol ²	Тур	Unit
GPIO inputs—minimum pulse width	t _{PIWID}	20	ns

Notes:

- 1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
- 2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

This figure provides the AC test load for the GPIO.



Figure 40. GPIO AC Test Load

15 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8360E/58E.

15.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins of the IPIC.

Table 53. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	—	—	±10	μA
Output low voltage	V _{OL}	I _{OL} = 6.0 mA	—	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V

Notes:

1. This table applies for pins IRQ[0:7], IRQ_OUT, MCP_OUT, and CE ports Interrupts.

2. IRQ_OUT and MCP_OUT are open drain pins, thus V_{OH} is not relevant for those pins.



Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_DEVSEL/CE_PF[16]	E26	I/O	OV _{DD}	5
PCI_IDSEL/CE_PF[17]	F22	I/O	OV _{DD}	
PCI_SERR/CE_PF[18]	B29	I/O	OV _{DD}	5
PCI_PERR/CE_PF[19]	A29	I/O	OV _{DD}	5
PCI_REQ[0]/CE_PF[20]	F19	I/O	LV _{DD} 2	—
PCI_REQ[1]/CPCI_HS_ES/ CE_PF[21]	A21	I/O	LV _{DD} 2	—
PCI_REQ[2]/CE_PF[22]	C21	I/O	LV _{DD} 2	
PCI_GNT[0]/CE_PF[23]	E20	I/O	LV _{DD} 2	
PCI_GNT[1]/CPCI1_HS_LED/ CE_PF[24]	B20	I/O	LV _{DD} 2	_
PCI_GNT[2]/CPCI1_HS_ENUM/ CE_PF[25]	C20	I/O	LV _{DD} 2	
PCI_MODE	D36	I	OV _{DD}	—
M66EN/CE_PF[4]	B37	I/O	OV _{DD}	
	Local Bus Controller Interface			
LAD[0:31]	N32, N33, N35, N36, P37, P32, P34, R36, R35, R34, R33, T37, T35, T34, T33, U37, T32, U36, U34, V36, V35, W37, W35, V33, V32, W34, Y36, W32, AA37, Y33, AA35, AA34	I/O	OV _{DD}	_
LDP[0]/CKSTOP_OUT	AB37	I/O	OV _{DD}	
LDP[1]/CKSTOP_IN	AB36	I/O	OV _{DD}	
LDP[2]/LCS[6]	AB35	I/O	OV _{DD}	
LDP[3]/LCS[7]	AA33	I/O	OV _{DD}	
LA[27:31]	AC37, AA32, AC36, AC34, AD36	0	OV _{DD}	
LCS[0:5]	AD33, AG37, AF34, AE33, AD32, AH37	0	OV_{DD}	
LWE[0:3]/LSDDQM[0:3]/LBS[0:3]	AG35, AG34, AH36, AE32	0	OV_{DD}	
LBCTL	AD35	0	OV_{DD}	
LALE	M37	0	OV_{DD}	
LGPL0/LSDA10/cfg_reset_source0	AB32	I/O	OV_{DD}	
LGPL1/LSDWE/cfg_reset_source1	AE37	I/O	OV_{DD}	
LGPL2/LSDRAS/LOE	AC33	0	OV_{DD}	
LGPL3/LSDCAS/cfg_reset_source2	AD34	I/O	OV_{DD}	
LGPL4/LGTA/LUPWAIT/LPBSE	AE35	I/O	OV_{DD}	
LGPL5/cfg_clkin_div	AF36	I/O	OV_{DD}	
LCKE	G36	0	OV _{DD}	—
LCLK[0]	J33	0	OV _{DD}	—
LCLK[1]/LCS[6]	J34	0	OV _{DD}	—



Pinout Listings

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
No Connect				
NC	AM20, AU19	—	—	—

Notes:

- 1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}
- 2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.
- 3. This output is actively driven during reset rather than being three-stated during reset.
- 4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- 5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
- 6. These are On Die Termination pins, used to control DDR2 memories internal termination resistance.
- 7. This pin must always be tied to GND.
- 8. This pin must always be left not connected.
- 9. Refer to MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual section on "RGMII Pins," for information about the two UCC2 Ethernet interface options.
- 10.It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor for DDR2.

This table shows the pin list of the MPC8358E TBGA package.

Table 67. MPC8358E TBGA Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	DDR SDRAM Memory Controller Interface			
MEMC1_MDQ[0:63]	AJ34, AK33, AL33, AL35, AJ33, AK34, AK32, AM36, AN37, AN35, AR34, AT34, AP37, AP36, AR36, AT35, AP34, AR32, AP32, AM31, AN33, AM34, AM33, AM30, AP31, AM27, AR30, AT32, AN29, AP29, AN27, AR29, AN8, AN7, AM8, AM6, AP9, AN9, AT7, AP7, AU6, AP6, AR4, AR3, AT6, AT5, AR5, AT3, AP4, AM5, AP3, AN3, AN5, AL5, AN4, AM2, AL2, AH5, AK3, AJ2, AJ3, AH4, AK4, AH3	I/O	GV _{DD}	
MEMC_MECC[0:4]/MSRCID[0:4]	AP24, AN22, AM19, AN19, AM24	I/O	GV _{DD}	—
MEMC_MECC[5]/MDVAL	AM23	I/O	GV _{DD}	—
MEMC_MECC[6:7]	AM22, AN18	I/O	GV _{DD}	—
MEMC_MDM[0:8]	AL36, AN34, AP33, AN28,AT9, AU4, AM3, AJ6,AP27	0	GV _{DD}	Ι
MEMC_MDQS[0:8]	AK35, AP35, AN31, AM26,AT8, AU3, AL4, AJ5, AP26	I/O	GV _{DD}	Ι
MEMC_MBA[0:1]	AU29, AU30	0	GV _{DD}	
MEMC_MBA[2]	AT30	0	GV _{DD}	_
MEMC_MA[0:14]	AU21, AP22, AP21, AT21, AU25, AU26, AT23, AR26, AU24, AR23, AR28, AU23, AR22, AU20, AR18	0	GV _{DD}	
MEMC_MODT[0:3]	AG33, AJ36, AT1, AK2	0	GV _{DD}	6



Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MWE	AT26	0	GV _{DD}	—
MEMC_MRAS	AT29	0	GV _{DD}	—
MEMC_MCAS	AT24	0	GV _{DD}	—
MEMC_MCS[0:3]	AU27, AT27, AU8, AU7	0	GV _{DD}	—
MEMC_MCKE[0:1]	AL32, AU33	0	GV _{DD}	3
MEMC_MCK[0:5]	AK37, AT37, AN1, AR2, AN25, AK1	0	GV _{DD}	—
MEMC_MCK[0:5]	AL37, AT36, AP2, AT2, AN24, AL1	0	GV _{DD}	—
MDIC[0:1]	AH6, AP30	I/O	GV _{DD}	11
	PCI			
PCI_INTA/IRQ_OUT/CE_PF[5]	A20	I/O	LV _{DD} 2	2
PCI_RESET_OUT/CE_PF[6]	E19	I/O	LV _{DD} 2	—
PCI_AD[31:30]/CE_PG[31:30]	D20, D21	I/O	LV _{DD} 2	—
PCI_AD[29:25]/CE_PG[29:25]	A24, B23, C23, E23, A26	I/O	OV _{DD}	—
PCI_AD[24]/CE_PG[24]	B21	I/O	LV _{DD} 2	—
PCI_AD[23:0]/CE_PG[23:0]	C24, C25, D25, B25, E24, F24, A27, A28, F27, A30, C30, D30, E29, B31, C31, D31, D32, A32, C33, B33, F30, E31, A34, D33	I/O	OV _{DD}	_
PCI_C/BE[3:0]/CE_PF[10:7]	E22, B26, E28, F28	I/O	OV _{DD}	—
PCI_PAR/CE_PF[11]	D28	I/O	OV _{DD}	—
PCI_FRAME/CE_PF[12]	D26	I/O	OV _{DD}	5
PCI_TRDY/CE_PF[13]	C27	I/O	OV _{DD}	5
PCI_IRDY/CE_PF[14]	C28	I/O	OV _{DD}	5
PCI_STOP/CE_PF[15]	B28	I/O	OV _{DD}	5
PCI_DEVSEL/CE_PF[16]	E26	I/O	OV _{DD}	5
PCI_IDSEL/CE_PF[17]	F22	I/O	OV _{DD}	—
PCI_SERR/CE_PF[18]	B29	I/O	OV _{DD}	5
PCI_PERR/CE_PF[19]	A29	I/O	OV _{DD}	5
PCI_REQ[0]/CE_PF[20]	F19	I/O	LV _{DD} 2	—
PCI_REQ[1]/CPCI_HS_ES/ CE_PF[21]	A21	I/O	LV _{DD} 2	-
PCI_REQ[2]/CE_PF[22]	C21	I/O	LV _{DD} 2	—
PCI_GNT[0]/CE_PF[23]	E20	I/O	LV _{DD} 2	—
PCI_GNT[1]/CPCI1_HS_LED/ CE_PF[24]	B20	I/O	LV _{DD} 2	—
PCI_GNT[2]/CPCI1_HS_ENUM/ CE_PF[25]	C20	I/O	LV _{DD} 2	_



Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_MODE	D36	I	OV _{DD}	
M66EN/CE_PF[4]	B37	I/O	OV _{DD}	
	Local Bus Controller Interface			
LAD[0:31]	N32, N33, N35, N36, P37, P32, P34, R36, R35, R34, R33, T37, T35, T34, T33, U37, T32, U36, U34, V36, V35, W37, W35, V33, V32, W34, Y36, W32, AA37, Y33, AA35, AA34	I/O	OV _{DD}	_
LDP[0]/CKSTOP_OUT	AB37	I/O	OV _{DD}	_
LDP[1]/CKSTOP_IN	AB36	I/O	OV _{DD}	_
LDP[2]/LCS[6]	AB35	I/O	OV _{DD}	_
LDP[3]/LCS[7]	AA33	I/O	OV _{DD}	
LA[27:31]	AC37, AA32, AC36, AC34, AD36	0	OV _{DD}	
LCS[0:5]	AD33, AG37, AF34, AE33, AD32, AH37	0	OV _{DD}	
LWE[0:3]/LSDDQM[0:3]/LBS[0:3]	AG35, AG34, AH36, AE32	0	OV _{DD}	
LBCTL	AD35	0	OV _{DD}	
LALE	M37	0	OV _{DD}	
LGPL0/LSDA10/cfg_reset_source0	AB32	I/O	OV _{DD}	
LGPL1/LSDWE/cfg_reset_source1	AE37	I/O	OV _{DD}	
LGPL2/LSDRAS/LOE	AC33	0	OV _{DD}	
LGPL3/LSDCAS/cfg_reset_source2	AD34	I/O	OV _{DD}	
LGPL4/LGTA/LUPWAIT/LPBSE	AE35	I/O	OV _{DD}	_
LGPL5/cfg_clkin_div	AF36	I/O	OV _{DD}	_
LCKE	G36	0	OV _{DD}	
LCLK[0]	J33	0	OV _{DD}	_
LCLK[1]/LCS[6]	J34	0	OV _{DD}	_
LCLK[2]/LCS[7]	G37	0	OV _{DD}	
LSYNC_OUT	F34	0	OV _{DD}	
LSYNC_IN	G35	I	OV _{DD}	
	Programmable Interrupt Controller			
MCP_OUT	E34	0	OV _{DD}	2
IRQ0/MCP_IN	C37	I	OV _{DD}	_
IRQ[1]/M1SRCID[4]/M2SRCID[4]/ LSRCID[4]	F35	I/O	OV_{DD}	
IRQ[2]/M1DVAL/M2DVAL/LDVAL	F36	I/O	OV _{DD}	_
IRQ[3]/CORE_SRESET	H34	I/O	OV_{DD}	



Pinout Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV _{DD} 1	C17, D16	Power for UCC2 Ethernet interface option 1 (2.5 V, 3.3 V)	LV _{DD} 1	9
LV _{DD} 2	B18, E21	Power for UCC2 Ethernet interface option 2 (2.5 V, 3.3 V)	LV _{DD} 2	9
V _{DD}	C36, D29, D35, E16, F9, F12, F15, F17, F18, F20, F21, F23, F25, F26, F29, F31, F32, F33, G6, J6, K32, M32, N6, P33, R6, R32, U32, V6, Y5, Y32, AB6, AB33, AD6, AF32, AK6, AL6, AM7, AM9, AM10, AM11, AM12, AM13, AM14, AM15, AM18, AM21, AM25, AM28, AM32, AN15, AN21, AN26, AU9, AU17	Power for core (1.2 V)	V _{DD}	_
OV _{DD}	A10, B9, B15, B32, C1, C12, C22, C29, D24, E3, E10, E27, G4, H35, J1, J35, K2, M4, N3, N34, R2, R37, T36, U2, U33, V4, V34, W3, Y35, Y37, AA1, AA36, AB2, AB34	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV _{DD}	
MVREF1	AN20	I	DDR reference voltage	_
MVREF2	AU32	I	DDR reference voltage	
			Г	
SPARE1	B11	I/O	OV _{DD}	8
SPARE3	AH32		GV _{DD}	8
SPARE4	AU18	—	GV _{DD}	7
SPARE5	AP1	—	GV _{DD}	8

Table 67. MPC8358E TBGA Pinout Listing (continued)



Pinout Listings

clock. When the device is configured as a PCI agent device the CLKIN and the CFG_CLKIN_DIV signals should be tied to GND.

When the device is configured as a PCI host device (RCWH[PCIHOST] = 1) and PCI clock output is disabled (RCWH[PCICKDRV] = 0), clock distribution and balancing done externally on the board. Therefore, PCI_SYNC_IN is the primary input clock.

As shown in Figure 54 and Figure 55, the primary clock input (frequency) is multiplied by the QUICC Engine block phase-locked loop (PLL), the system PLL, and the clock unit to create the QUICC Engine clock (ce_clk), the coherent system bus clock (csb_clk), the internal DDRC1 controller clock ($ddr1_clk$), and the internal clock for the local bus interface unit and DDR2 memory controller (lb_clk).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb_clk = \{PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)\} \times SPMF$$

In PCI host mode, PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV) is the CLKIN frequency; in PCI agent mode, CFG_CLKIN_DIV must be pulled down (low), so PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV) is the PCI_CLK frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, "Reset, Clocking, and Initialization," in the *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* for more information on the clock subsystem.

The *ce_clk* frequency is determined by the QUICC Engine PLL multiplication factor (RCWL[CEPMF) and the QUICC Engine PLL division factor (RCWL[CEPDF]) according to the following equation:

 $ce_clk = (primary clock input \times CEPMF) \div (1 + CEPDF)$

The internal *ddr1_clk* frequency is determined by the following equation:

 $ddr1_clk = csb_clk \times (1 + RCWL[DDR1CM])$

Note that the lb_clk clock frequency (for DDRC2) is determined by RCWL[LBCM]. The *internal ddr1_clk* frequency is not the external memory bus frequency; *ddr1_clk* passes through the DDRC1 clock divider (\div 2) to create the differential DDRC1 memory bus clock outputs (MEMC1_MCK and MEMC1_MCK). However, the data rate is the same frequency as *ddr1_clk*.

The internal *lb_clk* frequency is determined by the following equation:

 $lb_clk = csb_clk \times (1 + \text{RCWL[LBCM]})$

Note that *lb_clk* is not the external local bus or DDRC2 frequency; *lb_clk* passes through the a LB clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LB clock divider ratio is controlled by LCRR[CLKDIV].

Additionally, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. This table specifies which units have a configurable clock frequency.

Unit	Default Frequency	Options
Security core	csb_clk/3	Off, <i>csb_clk</i> ¹ , <i>csb_clk</i> /2, <i>csb_clk</i> /3
PCI and DMA complex	csb_clk	Off, <i>csb_clk</i>

Table 68	Configurable	Clock	Units
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¹ With limitation, only for slow csb_clk rates, up to 166 MHz.

This table provides the operating frequencies for the TBGA package under recommended operating conditions (see Table 2). All frequency combinations shown in the table below may not be available. Maximum operating frequencies depend on the part



Configuration Pin Muxing



Figure 57. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term} . The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD} , nominal OV_{DD} , 105° C.

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R _N	42 Target	25 Target	20 Target	Z ₀	W
R _P	42 Target	25 Target	20 Target	Z ₀	W
Differential	NA	NA	NA	Z _{DIFF}	W

Table 79. Impedance Characteristics

Note: Nominal supply voltages. See Table 1, $T_J = 105^{\circ}$ C.

23.6 Configuration Pin Muxing

The device provides the user with power-on configuration options that can be set through the use of external pull-up or pull-down resistors of 4.7 k Ω on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While HRESET is asserted however, these pins are treated as inputs. The value presented on these pins while HRESET is asserted, is latched when HRESET deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

Part Numbers Fully Addressed by this Document

Device	Package	SVR (Rev. 2.0)	SVR (Rev. 2.1)
MPC8358E	TBGA	0x804A_0020	0x804A_0021
MPC8358	TBGA	0x804B_0020	0x804B_0021

25 Document Revision History

This table provides a revision history for this document.

Table 82. Revision History

Rev. Number	Date	Substantive Change(s)
5	09/2011	 Section 2.2.1, "Power-Up Sequencing", added the current limitation "3A to 5A" for the excessive current. Section 2.1.2, "Power Supply Voltage Specification, Updated the Characteristic for TBGA (MPC8358 & MPC8360 Device) with specific frequency for Core and PLL voltages. Added table footnote 3 to Table 2. Applied table footnotes 1 and 2 to Table 10. Removed table footnotes from Table 19. Applied table footnotes 8 and 9 to Table 40. Applied table footnotes 2 and 3 to Table 41. Applied table footnotes from Table 46. Applied table footnote to last three rows of Table 65.
4	01/2011	 Updated references to the LCRR register throughout Removed references to DDR DLL mode in Section 6.2.2, "DDR and DDR2 SDRAM Output AC Timing Specifications." Changed "Junction-to-Case" to "Junction-to-Ambient" in Section 22.2.4, "Heat Sinks and Junction-to-Ambient Thermal Resistance," and Table 78, "Heat Sinks and Junction-to-Ambient Thermal Resistance of TBGA Package," titles.