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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8360vvajdga

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Power Sequencing

This figure shows the undershoot and overshoot voltage of the PCI interface of the device for the 3.3-V signals, respectively.



Figure 4. Maximum AC Waveforms on PCI interface for 3.3-V Signaling

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	42	OV _{DD} = 3.3 V
PCI signals	25	
PCI output clocks (including PCI_SYNC_OUT)	42	
DDR signal	20 36 (half-strength mode) ¹	GV _{DD} = 2.5 V
DDR2 signal	18 36 (half-strength mode) ¹	GV _{DD} = 1.8 V
10/100/1000 Ethernet signals	42	LV _{DD} = 2.5/3.3 V
DUART, system control, I ² C, SPI, JTAG	42	OV _{DD} = 3.3 V
GPIO signals	42	OV _{DD} = 3.3 V LV _{DD} = 2.5/3.3 V

Note:

1. DDR output impedance values for half strength mode are verified by design and not tested.

2.2 Power Sequencing

This section details the power sequencing considerations for the MPC8360E/58E.





Table 4. MPC8360E TBGA Core Power Dissipation ¹	(continued)
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Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
667	333	500	6.1	6.8	W	2, 3, 5, 9

Notes:

- 1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 6.
- 2. Typical power is based on a voltage of V_{DD} = 1.2 V or 1.3 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.
- 3. Thermal solutions need to design to a value higher than typical power on the end application, T_A target, and I/O power.
- 4. Maximum power is based on a voltage of V_{DD} = 1.2 V, WC process, a junction T_J = 105°C, and an artificial smoke test.
- Maximum power is based on a voltage of V_{DD} = 1.3 V for applications that use 667 MHz (CPU)/500 (QE) with WC process, a junction T₁ = 105° C, and an artificial smoke test.
- 6. Typical power is based on a voltage of V_{DD} = 1.3 V, a junction temperature of T_J = 70° C, and a Dhrystone benchmark application.
- Maximum power is based on a voltage of V_{DD} = 1.3 V for applications that use 667 MHz (CPU) or 500 (QE) with WC process, a junction T_J = 70° C, and an artificial smoke test.
- 8. This frequency combination is only available for rev. 2.0 silicon.
- 9. This frequency combination is not available for rev. 2.0 silicon.

Table 5. MPC8358E TBGA Core Power Dissipation¹

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	300	4.1	4.5	W	2, 3, 4
400	266	400	4.5	5.0	W	2, 3, 4

Notes:

- 1. The values do not include I/O supply power (OV_{DD}, LV_{DD} , GV_{DD}) or AV_{DD} . For I/O power values, see Table 6.
- Typical power is based on a voltage of V_{DD} = 1.2 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.
- 3. Thermal solutions need to design to a value higher than typical power on the end application, T_A target, and I/O power.
- 4. Maximum power is based on a voltage of V_{DD} = 1.2 V, WC process, a junction T_J = 105°C, and an artificial smoke test.



Power Sequencing

This table shows the estimated typical I/O power dissipation for the device.

Interface	Parameter	GV _{DD} (1.8 V)	GV _{DD} (2.5 V)	OV _{DD} (3.3 V)	LV _{DD} (3.3 V)	LV _{DD} (2.5 V)	Unit	Comments
DDR I/O	200 MHz, 1 \times 32 bits	0.3	0.46	_	_	—	W	—
65% utilization R _s = 20 Ω	200 MHz, 1 \times 64 bits	0.4	0.58			—	W	—
$R_t = 50 \Omega$	200 MHz, 2×32 bits	0.6	0.92	_	_	—	W	_
	266 MHz, 1 \times 32 bits	0.35	0.56	_	_	—	W	_
	266 MHz, 1 \times 64 bits	0.46	0.7	_	_	—	W	_
	266 MHz, 2×32 bits	0.7	1.11		—	—	W	_
	333 MHz, 1 \times 32 bits	0.4	0.65	_	_	—	W	_
	333 MHz, 1 \times 64 bits	0.53	0.82		—	—	W	_
	333 MHz, 2×32 bits	0.81	1.3		—	—	W	_
Local Bus I/O	133 MHz, 32 bits	—	—	0.22	_	_	W	_
3 pairs of clocks	83 MHz, 32 bits	—	—	0.14	—	—	W	—
	66 MHz, 32 bits	—	—	0.12	—	—	W	_
	50 MHz, 32 bits	—	—	0.09	—	—	W	_
PCI I/O	33 MHz, 32 bits	—	—	0.05	—	—	W	_
Load = 30 pF	66 MHz, 32 bits	—	—	0.07	—	—	W	—
10/100/1000 Ethernet I/O Load = 20 pF	MII or RMII	—	—	_	0.01	—	W	Multiply by
	GMII or TBI	—	—	_	0.04	—	W	interfaces used.
	RGMII or RTBI	—	—	—	—	0.04	W	
Other I/O	_	—	_	0.1	—	—	W	_

Table 6. Estimated Typical I/O Power Dissipation

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8360E/58E.

NOTE

The rise/fall time on QUICC Engine block input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of V_{DD} ; fall time refers to transitions from 90% to 10% of V_{DD} .



DDR and DDR2 SDRAM AC Electrical Characteristics

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input high voltage	V _{IH}	MV _{REF} + 0.18	GV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.18	V	—
Output leakage current	I _{OZ}	—	±10	μA	4
Output high current (V _{OUT} = 1.95 V)	I _{ОН}	-15.2	-	mA	—
Output low current (V _{OUT} = 0.35 V)	I _{OL}	15.2	_	mA	—
MV _{REF} input leakage current	I _{VREF}	—	±10	μA	—
Input current (0 V ≰⁄ _{IN} ≤OV _{DD})	I _{IN}	—	±10	μA	_

Table 16. DDR SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 2.5 V (continued)

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.

- 2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
- 3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
- 4. Output leakage is measured with all outputs disabled, 0 V \leq V_{OUT} \leq GV_{DD}.

This table provides the DDR capacitance when $GV_{DD}(typ) = 2.5$ V.

Table 17. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C _{DIO}	_	0.5	pF	1

Note:

1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25° C, V_{OUT} = $GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM interface when $GV_{DD}(typ) = 1.8 V$.

Table 18. DDR2 SDRAM Input AC Timing Specifications for GV_{DD}(typ) = 1.8 V

At recommended operating conditions with GV_{DD} of 1.8 V ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V _{IL}	—	MV _{REF} – 0.25	V	—
AC input high voltage	V _{IH}	MV _{REF} + 0.25	_	V	_



DDR and DDR2 SDRAM AC Electrical Characteristics

This table provides the input AC timing specifications for the DDR SDRAM interface when $GV_{DD}(typ) = 2.5 \text{ V}$.

Table 19. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 2.5 V ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V _{IL}	—	MV _{REF} – 0.31	V	—
AC input high voltage	V _{IH}	MV _{REF} + 0.31	_	V	_

Table 20. DDR and DDR2 SDRAM Input AC Timing Specifications Mode

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
MDQS—MDQ/MECC input skew per byte 333 MHz 266 MHz 200 MHz	t _{DISKEW}	-750 -1125 -1250	750 1125 1250	ps	1, 2

Notes:

1. AC timing values are based on the DDR data rate, which is twice the DDR memory bus frequency.

Maximum possible skew between a data strobe (MDQS[n]) and any corresponding bit of data (MDQ[8n + {0...7}] if 0 ≤n ≤7) or ECC (MECC[{0...7}] if n = 8).

This figure shows the input timing diagram for the DDR controller.



Figure 6. DDR Input Timing Diagram



GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

Table 32. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with $\text{LV}_{\text{DD}}/\text{OV}_{\text{DD}}$ of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	t _{RMRDVKH}	4.0	_	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	t _{RMRDXKH}	2.0	_	—	ns
REF_CLK clock rise time	t _{RMXR}	1.0	_	4.0	ns
REF_CLK clock fall time	t _{RMXF}	1.0	_	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first three letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{RMRDVKH} symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, t_{RMRDXKL} symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}

This figure provides the AC test load.



Figure 16. AC Test Load

This figure shows the RMII receive AC timing diagram.



Figure 17. RMII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.



Ethernet Management Interface Electrical Characteristics

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.



Figure 20. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, TBI, and RTBI are specified in Section 8.1, "Three-Speed Ethernet Controller (10/100/1000 Mbps)— GMII/MII/RMII/TBI/RGMII/RTBI Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage (3.3 V)	OV _{DD}	—		2.97	3.63	V
Output high voltage	V _{OH}	$I_{OH} = -1.0 \text{ mA}$	$OV_{DD} = Min$	2.10	OV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	$OV_{DD} = Min$	GND	0.50	V
Input high voltage	V _{IH}	—		2.00	—	V
Input low voltage	V _{IL}	—		—	0.80	V
Input current	I _{IN}	0 V ≤V _{IN} ≤OV _{DD}		—	±10	μA

Table 36. MII Management DC Electrica	I Characteristics When Powered at 3.3 V
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Local Bus AC Electrical Specifications

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to output valid	t _{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ}		4	ns	8

Table 41. Local Bus General Timing Parameters—DLL Bypass Mode⁹ (continued)

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the to the output (O) going invalid (X) or output hold time.
 </sub>
- 2. All timings are in reference to falling edge of LCLK0 (for all outputs and for LGTA and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
- 3. All signals are measured from OV_{DD}/2 of the rising/falling edge of LCLK0 to 0.4 × OV_{DD} of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. t_{LBOTOT1} should be used when RCWH[LALE] is not set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- t_{LBOTOT2} should be used when RCWH[LALE] is set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
- 7. t_{LBOTOT3} should be used when RCWH[LALE] is set and when the load on LALE output pin equals to the load on LAD output pins.
- 8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 9. DLL bypass mode is not recommended for use at frequencies above 66 MHz.

This figure provides the AC test load for the local bus.



Figure 22. Local Bus C Test Load



HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

This figure shows the UTOPIA timing with internal clock.





18 HDLC, BISYNC, Transparent, and Synchronous UART

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent, and synchronous UART protocols of the MPC8360E/58E.

18.1 HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

This table provides the DC electrical characteristics for the device HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 61. HDLC, BISYNC,	Transparent, and Synchronous UART DC Electrical Characteristics
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Characteristic	Symbol	Condition	Min	Мах	Unit
Output high voltage	V _{OH}	I _{OH} = -2.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.5	V
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	0 V ≤V _{IN} ≤OV _{DD}	—	±10	μA

18.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

These tables provide the input and output AC timing specifications for HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 62. HDLC, BISYNC, and Transparent AC Timing Specifications¹

Characteristic	Symbol ²	Min	Мах	Unit
Outputs—Internal clock delay	t _{HIKHOV}	0	11.2	ns
Outputs—External clock delay	t _{HEKHOV}	1	10.8	ns



HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

Characteristic	Symbol ²	Min	Мах	Unit
Outputs—Internal clock high impedance	t _{нікнох}	-0.5	5.5	ns
Outputs—External clock high impedance	t _{НЕКНОХ}	1	8	ns
Inputs—Internal clock input setup time	t _{HIIVKH}	8.5	_	ns
Inputs—External clock input setup time	t _{HEIVKH}	4	-	ns
Inputs—Internal clock input hold time	t _{HIIXKH}	1.4	_	ns
Inputs—External clock input hold time	t _{HEIXKH}	1	_	ns

Table 62. HDLC, BISYNC, and Transparent AC Timing Specifications¹ (continued)

Notes:

- 1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
 </sub>

Characteristic	Symbol ²	Min	Мах	Unit
Outputs—Internal clock delay	t _{UAIKHOV}	0	11.3	ns
Outputs—External clock delay	t _{UAEKHOV}	1	14	ns
Outputs—Internal clock high impedance	t _{UAIKHOX}	0	11	ns
Outputs—External clock high impedance	t _{UAEKHOX}	1	14	ns
Inputs—Internal clock input setup time	t _{UAIIVKH}	6	—	ns
Inputs—External clock input setup time	t _{UAEIVKH}	8	—	ns
Inputs—Internal clock input hold time	t _{UAIIXKH}	1	—	ns
Inputs—External clock input hold time	t _{UAEIXKH}	1	—	ns

Notes:

- 1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
 </sub></sub>

This figure provides the AC test load.



Figure 49. AC Test Load



Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_DEVSEL/CE_PF[16]	E26	I/O	OV _{DD}	5
PCI_IDSEL/CE_PF[17]	F22	I/O	OV _{DD}	
PCI_SERR/CE_PF[18]	B29	I/O	OV _{DD}	5
PCI_PERR/CE_PF[19]	A29	I/O	OV _{DD}	5
PCI_REQ[0]/CE_PF[20]	F19	I/O	LV _{DD} 2	—
PCI_REQ[1]/CPCI_HS_ES/ CE_PF[21]	A21	I/O	LV _{DD} 2	—
PCI_REQ[2]/CE_PF[22]	C21	I/O	LV _{DD} 2	
PCI_GNT[0]/CE_PF[23]	E20	I/O	LV _{DD} 2	
PCI_GNT[1]/CPCI1_HS_LED/ CE_PF[24]	B20	I/O	LV _{DD} 2	_
PCI_GNT[2]/CPCI1_HS_ENUM/ CE_PF[25]	C20	I/O	LV _{DD} 2	
PCI_MODE	D36	Ι	OV _{DD}	—
M66EN/CE_PF[4]	B37	I/O	OV _{DD}	
	Local Bus Controller Interface			
LAD[0:31]	N32, N33, N35, N36, P37, P32, P34, R36, R35, R34, R33, T37, T35, T34, T33, U37, T32, U36, U34, V36, V35, W37, W35, V33, V32, W34, Y36, W32, AA37, Y33, AA35, AA34	I/O	OV _{DD}	_
LDP[0]/CKSTOP_OUT	AB37	I/O	OV _{DD}	
LDP[1]/CKSTOP_IN	AB36	I/O	OV _{DD}	
LDP[2]/LCS[6]	AB35	I/O	OV _{DD}	
LDP[3]/LCS[7]	AA33	I/O	OV _{DD}	
LA[27:31]	AC37, AA32, AC36, AC34, AD36	0	OV _{DD}	
LCS[0:5]	AD33, AG37, AF34, AE33, AD32, AH37	0	OV_{DD}	
LWE[0:3]/LSDDQM[0:3]/LBS[0:3]	AG35, AG34, AH36, AE32	0	OV_{DD}	
LBCTL	AD35	0	OV_{DD}	
LALE	M37	0	OV_{DD}	
LGPL0/LSDA10/cfg_reset_source0	AB32	I/O	OV_{DD}	
LGPL1/LSDWE/cfg_reset_source1	AE37	I/O	OV_{DD}	
LGPL2/LSDRAS/LOE	AC33	0	OV_{DD}	
LGPL3/LSDCAS/cfg_reset_source2	AD34	I/O	OV_{DD}	
LGPL4/LGTA/LUPWAIT/LPBSE	AE35	I/O	OV_{DD}	
LGPL5/cfg_clkin_div	AF36	I/O	OV_{DD}	
LCKE	G36	0	OV _{DD}	—
LCLK[0]	J33	0	OV _{DD}	—
LCLK[1]/LCS[6]	J34	0	OV _{DD}	—



Pinout Listings

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LCLK[2]/LCS[7]	G37	0	OV _{DD}	—
LSYNC_OUT	F34	0	OV _{DD}	—
LSYNC_IN	G35	I	OV _{DD}	—
	Programmable Interrupt Controller			•
MCP_OUT	E34	0	OV _{DD}	2
IRQ0/MCP_IN	C37	I	OV _{DD}	—
IRQ[1]/M1SRCID[4]/M2SRCID[4]/ LSRCID[4]	F35	I/O	OV _{DD}	
IRQ[2]/M1DVAL/M2DVAL/LDVAL	F36	I/O	OV _{DD}	—
IRQ[3]/CORE_SRESET	H34	I/O	OV _{DD}	—
IRQ[4:5]	G33, G32	I/O	OV _{DD}	—
IRQ[6]/LCS[6]/CKSTOP_OUT	E35	I/O	OV _{DD}	—
IRQ[7]/LCS[7]/CKSTOP_IN	H36	I/O	OV _{DD}	—
	DUART			•
UART1_SOUT/M1SRCID[0]/ M2SRCID[0]/LSRCID[0]	E32	0	OV _{DD}	_
UART1_SIN/M1SRCID[1]/ M2SRCID[1]/LSRCID[1]	B34	I/O	OV _{DD}	_
UART1_CTS/M1SRCID[2]/ M2SRCID[2]/LSRCID[2]	C34	I/O	OV _{DD}	_
UART1_RTS/M1SRCID[3]/ M2SRCID[3]/LSRCID[3]	A35	0	OV _{DD}	—
	I ² C Interface			
IIC1_SDA	D34	I/O	OV _{DD}	2
IIC1_SCL	B35	I/O	OV _{DD}	2
IIC2_SDA	E33	I/O	OV _{DD}	2
IIC2_SCL	C35	I/O	OV _{DD}	2
	QUICC Engine Block			
CE_PA[0]	F8	I/O	LV _{DD0}	—
CE_PA[1:2]	AH1, AG5	I/O	OV _{DD}	_
CE_PA[3:7]	F6, D4, C3, E5, A3	I/O	LV _{DD} 0	
CE_PA[8]	AG3	I/O	OV _{DD}	—
CE_PA[9:12]	F7, B3, E6, B4	I/O	LV _{DD} 0	—
CE_PA[13:14]	AG1, AF6	I/O	OV _{DD}	—
CE_PA[15]	B2	I/O	LV _{DD} 0	_
CE_PA[16]	AF4	I/O	OV _{DD}	_
CE_PA[17:21]	B16, A16, E17, A17, B17	I/O	LV _{DD} 1	



Signal	Pin Type	Power Supply	Notes	
LV _{DD} 0	D5, D6	Power for UCC1 Ethernet interface (2.5 V, 3.3 V)	LV _{DD} 0	
LV _{DD} 1	C17, D16	Power for UCC2 Ethernet interface option 1 (2.5 V, 3.3 V)	LV _{DD} 1	9
LV _{DD} 2	B18, E21	Power for UCC2 Ethernet interface option 2 (2.5 V, 3.3 V)	LV _{DD} 2	9
V _{DD}	C36, D29, D35, E16, F9, F12, F15, F17, F18, F20, F21, F23, F25, F26, F29, F31, F32, F33, G6, J6, K32, M32, N6, P33, R6, R32, U32, V6, Y5, Y32, AB6, AB33, AD6, AF32, AK6, AL6, AM7, AM9, AM10, AM11, AM12, AM13, AM14, AM15, AM18, AM21, AM25, AM28, AM32, AN15, AN21, AN26, AU9, AU17	Power for core (1.2 V)	V _{DD}	_
OV _{DD}	A10, B9, B15, B32, C1, C12, C22, C29, D24, E3, E10, E27, G4, H35, J1, J35, K2, M4, N3, N34, R2, R37, T36, U2, U33, V4, V34, W3, Y35, Y37, AA1, AA36, AB2, AB34	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV _{DD}	_
MVREF1	AN20	I	DDR reference voltage	—
MVREF2	AU32	I	DDR reference voltage	_
SPARE1	B11	I/O	OV _{DD}	8
SPARE3	AH32		GV _{DD}	8
SPARE4	AU18	_	GV _{DD}	7
SPARE5	AP1	_	GV _{DD}	8

Table 66. MPC8360E TBGA Pinout Listing (continued)



Pinout Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes		
CE_PB[0:27]	AE2, AE1, AD5, AD3, AD2, AC6, AC5, AC4, AC2, AC1, AB5, AB4, AB3, AB1, AA6, AA4, AA2, Y6, Y4, Y3, Y2, Y1, W6, W5, W2, V5, V3, V2	I/O	OV _{DD}	_		
CE_PC[0:1]	V1, U6	I/O	OV _{DD}			
CE_PC[2:3]	C16, A15	I/O	LV _{DD} 1	—		
CE_PC[4:6]	U4, U3, T6	I/O	OV _{DD}	—		
CE_PC[7]	C19	I/O	LV _{DD} 2	—		
CE_PC[8:9]	A4, C5	I/O	LV _{DD} 0	—		
CE_PC[10:30]	T5, T4, T2, T1, R5, R3, R1, C11, D12, F13, B10, C10, E12, A9, B8, D10, A14, E15, B14, D15, AH2	I/O	OV _{DD}	_		
CE_PD[0:27]	E11, D9, C8, F11, A7, E9, C7, A6, F10, B6, D7, E8, B5, A5, C2, E4, F5, B1, D2, G5, D1, E2, H6, F3, E1, F2, G3, H4	I/O	OV _{DD}	—		
CE_PE[0:31]	K3, J2, F1, G2, J5, H3, G1, H2, K6, J3, K5, K4, L6, P6, P4, P3, P1, N4, N5, N2, N1, M2, M3, M5, M6, L1, L2, L4, E14, C13, C14, B13	I/O	OV _{DD}	—		
CE_PF[0:3]	F14, D13, A12, A11	I/O	OV _{DD}	—		
	Clocks					
PCI_CLK_OUT[0]/CE_PF[26]	B22	I/O	LV _{DD} 2	—		
PCI_CLK_OUT[1:2]/CE_PF[27:28]	F[27:28] D22, A23		OV _{DD}	—		
CLKIN E37		I	OV _{DD}	—		
PCI_CLOCK/PCI_SYNC_IN M36		I	OV _{DD}	—		
PCI_SYNC_OUT/CE_PF[29]	D37	I/O	OV _{DD}	3		
	JTAG					
ТСК	K33	I	OV _{DD}	_		
TDI	К34	I	OV _{DD}	4		
TDO	H37	0	OV _{DD}	3		
TMS	J36	I	OV _{DD}	4		
TRST	L32	I	OV _{DD}	4		
Test						
TEST	L35	I	OV _{DD}	7		
TEST_SEL	AU34	I	GV _{DD}	10		
	PMC					
QUIESCE	B36	0	OV _{DD}	—		
System Control						

Table 67. MPC8358E TBGA Pinout Listing (continued)

System PLL Configuration

RCWL[SPMF]	System PLL Multiplication Factor
1100	× 12
1101	× 13
1110	× 14
1111	× 15

The RCWL[SVCOD] denotes the system PLL VCO internal frequency as shown in this table.

-	
RCWL[SVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

Table 71. System PLL VCO Divider

NOTE

The VCO divider must be set properly so that the system VCO frequency is in the range of 600-1400 MHz.

The system VCO frequency is derived from the following equations:

- $csb_clk = \{PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)\} \times SPMF$
- System VCO Frequency = *csb_clk* × VCO divider (if both RCWL[DDRCM] and RCWL[LBCM] are cleared) OR
- System VCO frequency = $2 \times csb_clk \times$ VCO divider (if either RCWL[DDRCM] or RCWL[LBCM] are set).

As described in Section 21, "Clocking," the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). This table shows the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

			Input Clock Frequency (MHz) ²			
CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2:1				133
Low	0011	3:1			100	200
Low	0100	4:1		100	133	266
Low	0101	5:1		125	166	333

Table 72. CSB Frequency Options



System PLL Configuration

			Ir	Input Clock Frequency (MHz) ²				
CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	16.67	25	33.33	66.67		
				csb_clk Freq	juency (MHz)			
Low	0110	6:1	100	150	200			
Low	0111	7:1	116	175	233			
Low	1000	8:1	133	200	266			
Low	1001	9:1	150	225	300			
Low	1010	10:1	166	250	333			
Low	1011	11:1	183	275				
Low	1100	12:1	200	300				
Low	1101	13:1	216	325				
Low	1110	14:1	233		-			
Low	1111	15:1	250					
Low	0000	16:1	266					
High	0010	2:1		-		133		
High	0011	3:1			100	200		
High	0100	4:1			133	266		
High	0101	5:1			166	333		
High	0110	6:1			200			
High	0111	7:1			233			
High	1000	8:1						
High	1001	9:1						
High	1010	10:1						
High	1011	11:1						
High	1100	12:1						
High	1101	13:1						
High	1110	14:1						
High	1111	15:1						
High	0000	16:1						

Table 72. CSB Frequency Options (continued)

¹ CFG_CLKIN_DIV is only used for host mode; CLKIN must be tied low and CFG_CLKIN_DIV must be pulled down (low) in agent mode.

 $^2\,$ CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.



The QUICC Engine block VCO frequency is derived from the following equations:

 $ce_clk = (primary clock input \times CEPMF) \div (1 + CEPDF)$

QE VCO Frequency = $ce_clk \times VCO$ divider $\times (1 + CEPDF)$

21.4 Suggested PLL Configurations

To simplify the PLL configurations, the device might be separated into two clock domains. The first domain contains the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine block PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. This table shows suggested PLL configurations for 33 and 66 MHz input clocks and illustrates each of the clock domains separately. Any combination of clock domains setting with same input clock are valid. Refer to Section 21, "Clocking," for the appropriate operating frequencies for your device.

Conf No. ¹	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock Freq (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
				33 MH:	z CLKIN/PCI	SYNC_IN	Options				
s1	0100	0000100	æ	æ	33	133	266	—	8	8	8
s2	0100	0000101	æ	æ	33	133	333	_	8	∞	8
s3	0101	0000100	æ	æ	33	166	333	_	8	8	8
s4	0101	0000101	æ	æ	33	166	416			8	8
s5	0110	0000100	æ	æ	33	200	400		8	8	8
s6	0110	0000110	æ	æ	33	200	600			—	8
s7	0111	0000011	æ	æ	33	233	350		8	8	8
s8	0111	0000100	æ	æ	33	233	466			8	8
s9	0111	0000101	æ	æ	33	233	583			_	8
s10	1000	0000011	æ	æ	33	266	400		8	8	8
s11	1000	0000100	æ	æ	33	266	533			8	8
s12	1000	0000101	æ	æ	33	266	667			_	8
s13	1001	0000010	æ	æ	33	300	300		8	8	8
s14	1001	0000011	æ	æ	33	300	450	_		8	8
s15	1001	0000100	æ	æ	33	300	600	_		—	8
s16	1010	0000010	æ	æ	33	333	333	_	8	8	8
s17	1010	0000011	æ	æ	33	333	500	_		8	8
s18	1010	0000100	æ	æ	33	333	667	_		—	8
c1	æ	æ	01001	0	33			300	8	8	8
c2	æ	æ	01100	0	33	_	_	400	8	8	8
c3	æ	æ	01110	0	33	_	_	466	_	8	8
c4	æ	æ	01111	0	33			500	_	8	8

Table 76. Suggested PLL Configurations



22.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

 T_I = junction temperature (° C)

 T_C = case temperature of the package (° C)

 $R_{\theta JC}$ = junction to case thermal resistance (° C/W)

 P_D = power dissipation (W)

23 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8360E/58E. Additional information can be found in *MPC8360E/MPC8358E PowerQUICC Design Checklist* (AN3097).

23.1 System Clocking

The device includes two PLLs, as follows.

- The platform PLL (AV_{DD}1) generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in Section 21.1, "System PLL Configuration."
- The e300 core PLL (AV_{DD}2) generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 21.2, "Core PLL Configuration."

23.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD} 1, AV_{DD} 2, respectively). The AV_{DD} level should always be equivalent to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide five independent filter circuits as illustrated in Figure 56, one to each of the five AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.



Table 82.	Revision	History	(continued)
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Rev. Number	Date	Substantive Change(s)
3	03/2010	 Changed references to RCWH[PCICKEN] to RCWH[PCICKDRV]. In Table 2, added extended temperature characteristics. Added Figure 6, "DDR Input Timing Diagram." In Figure 53, "Mechanical Dimensions and Bottom Surface Nomenclature of the TBGA Package," removed watermark. Updated the title of Table 19,"DDR SDRAM Input AC Timing Specifications." In Table 20, "DDR and DDR2 SDRAM Input AC Timing Specifications Mode," changed table subtitle. In Table 20, "DDR and DDR2 SDRAM Input AC Timing Specifications Mode," changed table subtitle. In Table 27–Table 30, and Table 33—Table 34, changed the rise and fall time specifications to reference 20–80% and 80–20% of the voltage supply, respectively. In Table 38, "IEEE 1588 Timer AC Specifications," changed units to "ns" for t_{I2DVKH}. In Table 45, "I2C AC Electrical Specifications," changed units to "ns" for t_{I2DVKH}. In Table 66, "MPC8360E TBGA Pinout Listing," and Table 67 "MPC8358E TBGA Pinout Listing, added note 7: "This pin must always be tied to GND" to the TEST pin and added a note to SPARE1 stating: "This pin must always be left not connected." In Section 4, "Clock Input Timing," added note regarding rise/fall time on QUICC Engine block input pins. Added Section 4.1, "injol/100/1000 Ethernet DC Electrical Characteristics." In Section 2.1, "Pinout Listing," added sentence stating "Refer to AN3097, 'MPC8360/MPC8358E PowerQUICC Design Checklist,' for proper pin termination and usage." In Section 21, "Clocking," removed statement: "The OCCR[PCICDn] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUTn signals." In Section 21.1, "System PLL Configuration," updated the system VCO frequency conditions. In Table 80, added extended temperature characteristics.
2	12/2007	Initial release.

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