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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 1.x (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	740-LBGA
Supplier Device Package	740-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8360vvalfha

- 10/100 Mbps Ethernet/IEEE Std. 802.3™ CDMA/CS interface through a media-independent interface (MII, RMII, RGMII)¹
- 1000 Mbps Ethernet/IEEE 802.3 CDMA/CS interface through a media-independent interface (GMII, RGMII, TBI, RTBI) on UCC1 and UCC2
- 9.6-Kbyte jumbo frames
- ATM full-duplex SAR, up to 622 Mbps (OC-12/STM-4), AAL0, AAL1, and AAL5 in accordance ITU-T I.363.5
- ATM AAL2 CPS, SSSAR, and SSTED up to 155 Mbps (OC-3/STM-1) Mbps full duplex (with 4 CPS packets per cell) in accordance ITU-T I.366.1 and I.363.2
- ATM traffic shaping for CBR, VBR, UBR, and GFR traffic types compatible with ATM forum TM4.1 for up to 64-Kbyte simultaneous ATM channels
- ATM AAL1 structured and unstructured circuit emulation service (CES 2.0) in accordance with ITU-T I.163.1 and ATM Forum af-vtoa-00-0078.000
- IMA (Inverse Multiplexing over ATM) for up to 31 IMA links over 8 IMA groups in accordance with the ATM forum AF-PHY-0086.000 (Version 1.0) and AF-PHY-0086.001 (Version 1.1)
- ATM Transmission Convergence layer support in accordance with ITU-T I.432
- ATM OAM handling features compatible with ITU-T I.610
- PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686, and 3153
- IP support for IPv4 packets including TOS, TTL, and header checksum processing
- Ethernet over first mile IEEE 802.3ah
- Shim header
- Ethernet-to-Ethernet/AAL5/AAL2 inter-working
- L2 Ethernet switching using MAC address or IEEE Std. 802.1P/Q™ VLAN tags
- ATM (AAL2/AAL5) to Ethernet (IP) interworking in accordance with RFC2684 including bridging of ATM ports to Ethernet ports
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics
- AAL2 protocol rate up to 4 CPS at OC-3/STM-1 rate
- Packet over Sonet (POS) up to 622-Mbps full-duplex 124 MultiPHY
- POS hardware; microcode must be loaded as an IRAM package
- Transparent up to 70-Mbps full-duplex
- HDLC up to 70-Mbps full-duplex
- HDLC BUS up to 10 Mbps
- Asynchronous HDLC
- UART
- BISYNC up to 2 Mbps
- User-programmable Virtual FIFO size
- QUICC multichannel controller (QMC) for 64 TDM channels
- One multichannel communication controller (MCC) only on the MPC8360E supporting the following:
 - 256 HDLC or transparent channels
 - 128 SS7 channels
 - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces
- Two UTOPIA/POS interfaces on the MPC8360E supporting 124 MultiPHY each (optional 2*128 MultiPHY with extended address) and one UTOPIA/POS interface on the MPC8358E supporting 31/124 MultiPHY
- Two serial peripheral interfaces (SPI); SPI2 is dedicated to Ethernet PHY management

¹.SMII or SGMII media-independent interface is not currently supported.

- Programmable highest priority request
- Four groups of interrupts with programmable priority
- External and internal interrupts directed to communication processor
- Redirects interrupts to external $\overline{\text{INTA}}$ pin when in core disable mode
- Unique vector number for each interrupt source
- Dual industry-standard I²C interfaces
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
 - System initialization data is optionally loaded from I²C-1 EPROM by boot sequencer embedded hardware
- DMA controller
 - Four independent virtual channels
 - Concurrent execution across multiple channels with programmable bandwidth control
 - All channels accessible by local core and remote PCI masters
 - Misaligned transfer capability
 - Data chaining and direct mode
 - Interrupt on completed segment and chain
 - DMA external handshake signals: $\overline{\text{DMA_DREQ}}[0:3]/\overline{\text{DMA_DACK}}[0:3]/\overline{\text{DMA_DONE}}[0:3]$. There is one set for each DMA channel. The pins are multiplexed to the parallel IO pins with other QE functions.
- DUART
 - Two 4-wire interfaces (Rx/D, Tx/D, RTS, CTS)
 - Programming model compatible with the original 16450 UART and the PC16550D
- System timers
 - Periodic interrupt timer
 - Real-time clock
 - Software watchdog timer
 - Eight general-purpose timers
- IEEE Std. 1149.1TM-compliant, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8360E/58E. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

Table 2. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value	Unit	Notes
PCI, local bus, DUART, system control and power management, I ² C, SPI, and JTAG I/O voltage	OV _{DD}	3.3 V ± 330 mV	V	—
Junction temperature	T _J	0 to 105 –40 to 105	°C	2

Notes:

1. GV_{DD}, LV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. The operating conditions for junction temperature, T_J, on the 600/333/400 MHz and 500/333/500 MHz on rev. 2.0 silicon is 0° to 70 °C. Refer to Errata General9 in *Chip Errata for the MPC8360E, Rev. 1*.
3. For more information on Part Numbering, refer to [Table 80](#).

This figure shows the undershoot and overshoot voltages at the interfaces of the device.

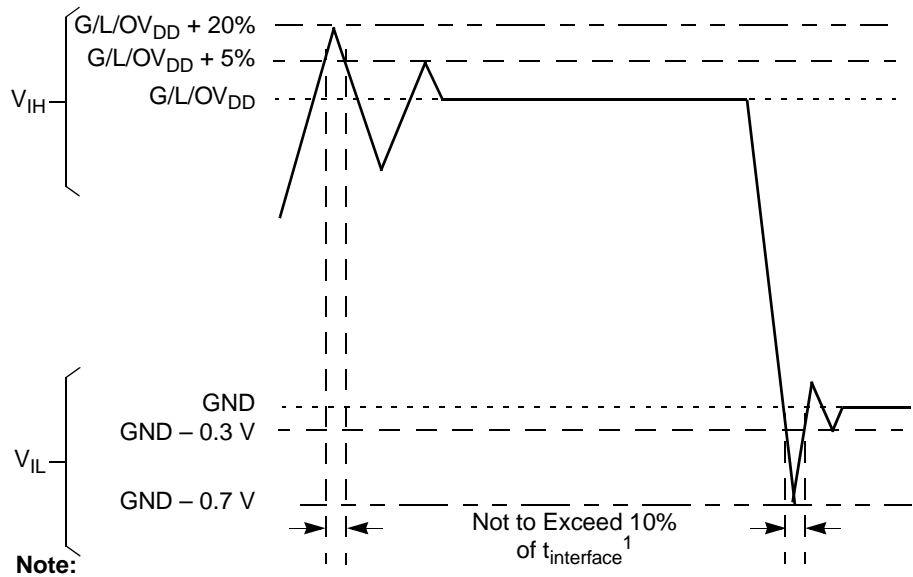

Figure 3. Overshoot/Undershoot Voltage for GV_{DD}/OV_{DD}/LV_{DD}

Table 4. MPC8360E TBGA Core Power Dissipation¹ (continued)

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
667	333	500	6.1	6.8	W	2, 3, 5, 9

Notes:

1. The values do not include I/O supply power (OV_{DD} , LV_{DD} , GV_{DD}) or AV_{DD} . For I/O power values, see [Table 6](#).
2. Typical power is based on a voltage of $V_{DD} = 1.2$ V or 1.3 V, a junction temperature of $T_J = 105^\circ\text{C}$, and a Dhrystone benchmark application.
3. Thermal solutions need to design to a value higher than typical power on the end application, T_A target, and I/O power.
4. Maximum power is based on a voltage of $V_{DD} = 1.2$ V, WC process, a junction $T_J = 105^\circ\text{C}$, and an artificial smoke test.
5. Maximum power is based on a voltage of $V_{DD} = 1.3$ V for applications that use 667 MHz (CPU)/500 (QE) with WC process, a junction $T_J = 105^\circ\text{C}$, and an artificial smoke test.
6. Typical power is based on a voltage of $V_{DD} = 1.3$ V, a junction temperature of $T_J = 70^\circ\text{C}$, and a Dhrystone benchmark application.
7. Maximum power is based on a voltage of $V_{DD} = 1.3$ V for applications that use 667 MHz (CPU) or 500 (QE) with WC process, a junction $T_J = 70^\circ\text{C}$, and an artificial smoke test.
8. This frequency combination is only available for rev. 2.0 silicon.
9. This frequency combination is not available for rev. 2.0 silicon.

Table 5. MPC8358E TBGA Core Power Dissipation¹

Core Frequency (MHz)	CSB Frequency (MHz)	QUICC Engine Frequency (MHz)	Typical	Maximum	Unit	Notes
266	266	300	4.1	4.5	W	2, 3, 4
400	266	400	4.5	5.0	W	2, 3, 4

Notes:

1. The values do not include I/O supply power (OV_{DD} , LV_{DD} , GV_{DD}) or AV_{DD} . For I/O power values, see [Table 6](#).
2. Typical power is based on a voltage of $V_{DD} = 1.2$ V, a junction temperature of $T_J = 105^\circ\text{C}$, and a Dhrystone benchmark application.
3. Thermal solutions need to design to a value higher than typical power on the end application, T_A target, and I/O power.
4. Maximum power is based on a voltage of $V_{DD} = 1.2$ V, WC process, a junction $T_J = 105^\circ\text{C}$, and an artificial smoke test.

5.3 QUICC Engine Block Operating Frequency Limitations

This section specifies the limits of the AC electrical characteristics for the operation of the QUICC Engine block's communication interfaces.

NOTE

The settings listed below are required for correct hardware interface operation. Each protocol by itself requires a minimal QUICC Engine block operating frequency setting for meeting the performance target. Because the performance is a complex function of all the QUICC Engine block settings, the user should make use of the QUICC Engine block performance utility tool provided by Freescale to validate their system.

This table lists the maximal QUICC Engine block I/O frequencies and the minimal QUICC Engine block core frequency for each interface.

Table 13. QUICC Engine Block Operating Frequency Limitations

Interface	Interface Operating Frequency (MHz)	Max Interface Bit Rate (Mbps)	Min QUICC Engine Operating Frequency ¹ (MHz)	Notes
Ethernet Management: MDC/MDIO	10 (max)	10	20	—
MII	25 (typ)	100	50	—
RMII	50 (typ)	100	50	—
GMII/RGMII/TBI/RTBI	125 (typ)	1000	250	—
SPI (master/slave)	10 (max)	10	20	—
UCC through TDM	50 (max)	70	$8 \times F$	2
MCC	25 (max)	16.67	$16 \times F$	2, 4
UTOPIA L2	50 (max)	800	$2 \times F$	2
POS-PHY L2	50 (max)	800	$2 \times F$	2
HDLC bus	10 (max)	10	20	—
HDLC/transparent	50 (max)	50	$8/3 \times F$	2, 3
UART/asynch HDLC	3.68 (max internal ref clock)	115 (Kbps)	20	—
BISYNC	2 (max)	2	20	—
USB	48 (ref clock)	12	96	—

Notes:

1. The QUICC Engine module needs to run at a frequency higher than or equal to what is listed in this table.
2. 'F' is the actual interface operating frequency.
3. The bit rate limit is independent of the data bus width (that is, the same for serial, nibble, or octal interfaces).
4. TDM in high-speed mode for serial data interface.

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR and DDR2 SDRAM interface of the MPC8360E/58E.

Table 16. DDR SDRAM DC Electrical Characteristics for $GV_{DD}(typ) = 2.5\text{ V}$ (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.18$	V	—
Output leakage current	I_{OZ}	—	± 10	μA	4
Output high current ($V_{OUT} = 1.95\text{ V}$)	I_{OH}	-15.2	—	mA	—
Output low current ($V_{OUT} = 0.35\text{ V}$)	I_{OL}	15.2	—	mA	—
MV_{REF} input leakage current	I_{VREF}	—	± 10	μA	—
Input current ($0\text{ V} \leq V_{IN} \leq OV_{DD}$)	I_{IN}	—	± 10	μA	—

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} . This rail should track variations in the DC level of MV_{REF} .
4. Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.

This table provides the DDR capacitance when $GV_{DD}(typ) = 2.5\text{ V}$.

Table 17. DDR SDRAM Capacitance for $GV_{DD}(typ) = 2.5\text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 2.5\text{ V} \pm 0.125\text{ V}$, $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM interface when $GV_{DD}(typ) = 1.8\text{ V}$.

Table 18. DDR2 SDRAM Input AC Timing Specifications for $GV_{DD}(typ) = 1.8\text{ V}$

At recommended operating conditions with GV_{DD} of $1.8\text{ V} \pm 5\%$.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	$MV_{REF} - 0.25$	V	—
AC input high voltage	V_{IH}	$MV_{REF} + 0.25$	—	V	—

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 21 and Table 22 provide the output AC timing specifications and measurement conditions for the DDR and DDR2 SDRAM interface.

Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode

At recommended operating conditions with GV_{DD} of (1.8 V or 2.5 V) \pm 5%.

Parameter ⁸	Symbol ¹	Min	Max	Unit	Notes
MCK[n] cycle time, (MCK[n]/ $\overline{MCK[n]}$ crossing)	t_{MCK}	6	10	ns	2
Skew between any MCK to ADDR/CMD 333 MHz 266 MHz 200 MHz	t_{AOSKEW}	-1.0 -1.1 -1.2	0.2 0.3 0.4	ns	3
ADDR/CMD output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHAS}	2.1 2.8 3.5	—	ns	4
ADDR/CMD output hold with respect to MCK 333 MHz 266 MHz—DDR1 266 MHz—DDR2 200 MHz	t_{DDKHAX}	2.0 2.7 2.8 3.5	—	ns	4
$\overline{MCS}(n)$ output setup with respect to MCK 333 MHz 266 MHz 200 MHz	t_{DDKHCS}	2.1 2.8 3.5	—	ns	4
$\overline{MCS}(n)$ output hold with respect to MCK 333 MHz 266 MHz 200 MHz	$t_{DDKHCSX}$	2.0 2.7 3.5	—	ns	4
MCK to MDQS	t_{DDKMHM}	-0.8	0.7	ns	5, 9
MDQ/MECC/MDM output setup with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDS} , t_{DDKLDS}	0.7 1.0 1.2	—	ns	6
MDQ/MECC/MDM output hold with respect to MDQS 333 MHz 266 MHz 200 MHz	t_{DDKHDX} , t_{DDKLDX}	0.7 1.0 1.2	—	ns	6
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	7

8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.2.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 29. MII Transmit AC Timing Specifications

At recommended operating conditions with V_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX} $t_{MTKHDXV}$	1 —	5	— 15	ns
TX_CLK data clock rise time, (20% to 80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall time, (80% to 20%)	t_{MTXF}	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the MII transmit AC timing diagram.

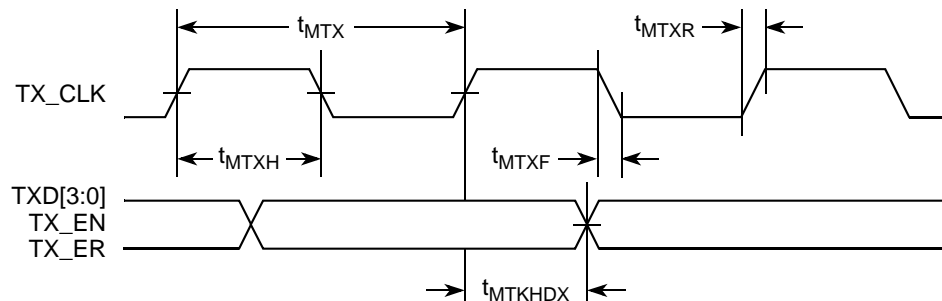


Figure 12. MII Transmit AC Timing Diagram

8.2.3 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.3.1 RMII Transmit AC Timing Specifications

This table provides the RMII transmit AC timing specifications.

Table 31. RMII Transmit AC Timing Specifications

At recommended operating conditions with V_{DD}/OV_{DD} of 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$ $t_{RMTKHDXV}$	2 —	—	— 10	ns
REF_CLK data clock rise time	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall time	t_{RMXF}	1.0	—	4.0	ns

Note:

- The symbols used for timing specifications follow the pattern of $t_{(first\ three\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

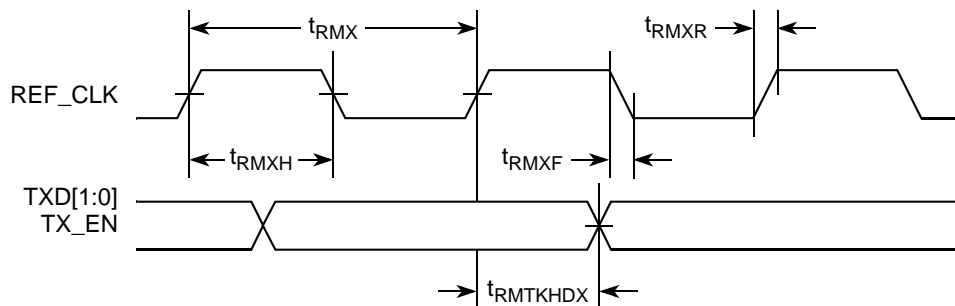


Figure 15. RMII Transmit AC Timing Diagram

8.2.3.2 RMII Receive AC Timing Specifications

This table provides the RMII receive AC timing specifications.

Table 32. RMII Receive AC Timing Specifications

At recommended operating conditions with V_{DD}/OV_{DD} of 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%

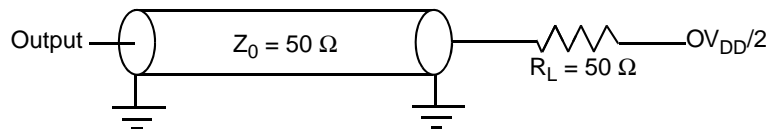
Table 41. Local Bus General Timing Parameters—DLL Bypass Mode⁹ (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	8

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for \overline{LGTA} and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
9. DLL bypass mode is not recommended for use at frequencies above 66 MHz.

This figure provides the AC test load for the local bus.


Figure 22. Local Bus C Test Load

15.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 54. IPIC Input AC Timing Specifications¹

Characteristic	Symbol ²	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

- Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
- IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

16 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8360E/58E.

16.1 SPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the device SPI.

Table 55. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	$I_{OH} = -6.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 6.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 10	μA

16.2 SPI AC Timing Specifications

This table and provide the SPI input and output AC timing specifications.

Table 56. SPI AC Timing Specifications¹

Characteristic	Symbol ²	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHox} t_{NIKHov}	0.3 —	— 8	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHox} t_{NEKHov}	2 —	— 8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	8	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns

17 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8360E/58E.

17.1 TDM/SI DC Electrical Characteristics

This table provides the DC electrical characteristics for the device TDM/SI.

Table 57. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	$I_{OH} = -2.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.5	V
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 10	μA

17.2 TDM/SI AC Timing Specifications

This table provides the TDM/SI input and output AC timing specifications.

Table 58. TDM/SI AC Timing Specifications¹

Characteristic	Symbol ²	Min	Max ³	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	10	ns
TDM/SI outputs—External clock high impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:

- Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
- Timings are measured from the positive or negative edge of the clock, according to SIxMR [CE] and SITXCEI[TXCEIx]. Refer *MPC8360E Integrated Communications Processor Reference Manual* for more details.

This figure provides the AC test load for the TDM/SI.

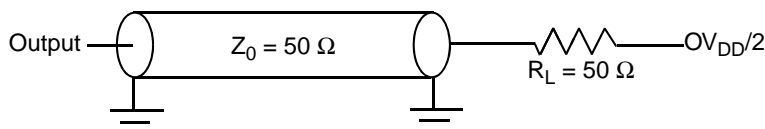


Figure 44. TDM/SI AC Test Load

Figure 45 represents the AC timing from Table 56. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

This figure shows the UTOPIA timing with internal clock.

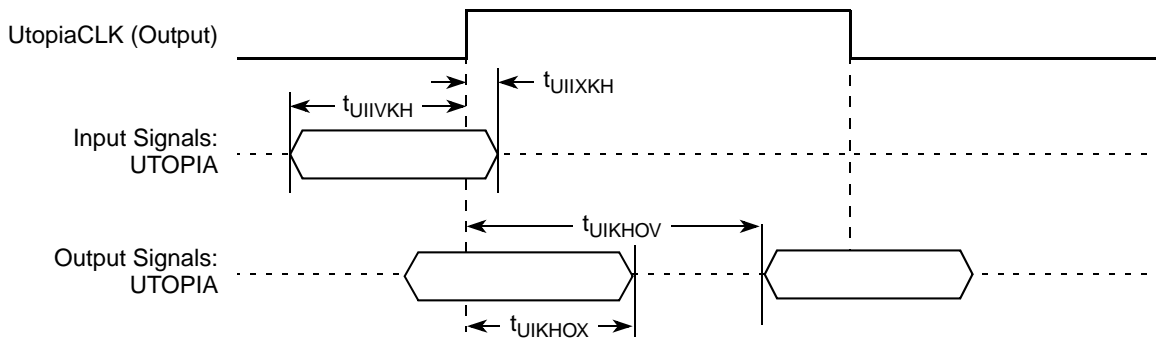


Figure 48. UTOPIA AC Timing (Internal Clock) Diagram

18 HDLC, BISYNC, Transparent, and Synchronous UART

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent, and synchronous UART protocols of the MPC8360E/58E.

18.1 HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

This table provides the DC electrical characteristics for the device HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 61. HDLC, BISYNC, Transparent, and Synchronous UART DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	$I_{OH} = -2.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.5	V
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 \text{ V} \leq V_{IN} \leq OV_{DD}$	—	± 10	μA

18.2 HDLC, BISYNC, Transparent, and Synchronous UART AC Timing Specifications

These tables provide the input and output AC timing specifications for HDLC, BISYNC, transparent, and synchronous UART protocols.

Table 62. HDLC, BISYNC, and Transparent AC Timing Specifications¹

Characteristic	Symbol ²	Min	Max	Unit
Outputs—Internal clock delay	t_{HIKHOV}	0	11.2	ns
Outputs—External clock delay	t_{HEKHOV}	1	10.8	ns

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LCLK[2]/LCS[7]	G37	O	OV _{DD}	—
LSYNC_OUT	F34	O	OV _{DD}	—
LSYNC_IN	G35	I	OV _{DD}	—
Programmable Interrupt Controller				
MCP_OUT	E34	O	OV _{DD}	2
IRQ0/MCP_IN	C37	I	OV _{DD}	—
IRQ[1]/M1SRCID[4]/M2SRCID[4]/LSRCID[4]	F35	I/O	OV _{DD}	—
IRQ[2]/M1DVAL/M2DVAL/LDVAL	F36	I/O	OV _{DD}	—
IRQ[3]/CORE_SRESET	H34	I/O	OV _{DD}	—
IRQ[4:5]	G33, G32	I/O	OV _{DD}	—
IRQ[6]/LCS[6]/CKSTOP_OUT	E35	I/O	OV _{DD}	—
IRQ[7]/LCS[7]/CKSTOP_IN	H36	I/O	OV _{DD}	—
DUART				
UART1_SOUT/M1SRCID[0]/M2SRCID[0]/LSRCID[0]	E32	O	OV _{DD}	—
UART1_SIN/M1SRCID[1]/M2SRCID[1]/LSRCID[1]	B34	I/O	OV _{DD}	—
UART1_CTS/M1SRCID[2]/M2SRCID[2]/LSRCID[2]	C34	I/O	OV _{DD}	—
UART1_RTS/M1SRCID[3]/M2SRCID[3]/LSRCID[3]	A35	O	OV _{DD}	—
I²C Interface				
IIC1_SDA	D34	I/O	OV _{DD}	2
IIC1_SCL	B35	I/O	OV _{DD}	2
IIC2_SDA	E33	I/O	OV _{DD}	2
IIC2_SCL	C35	I/O	OV _{DD}	2
QUICC Engine Block				
CE_PA[0]	F8	I/O	LV _{DD0}	—
CE_PA[1:2]	AH1, AG5	I/O	OV _{DD}	—
CE_PA[3:7]	F6, D4, C3, E5, A3	I/O	LV _{DD0}	—
CE_PA[8]	AG3	I/O	OV _{DD}	—
CE_PA[9:12]	F7, B3, E6, B4	I/O	LV _{DD0}	—
CE_PA[13:14]	AG1, AF6	I/O	OV _{DD}	—
CE_PA[15]	B2	I/O	LV _{DD0}	—
CE_PA[16]	AF4	I/O	OV _{DD}	—
CE_PA[17:21]	B16, A16, E17, A17, B17	I/O	LV _{DD1}	—

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LV _{DD0}	D5, D6	Power for UCC1 Ethernet interface (2.5 V, 3.3 V)	LV _{DD0}	—
LV _{DD1}	C17, D16	Power for UCC2 Ethernet interface option 1 (2.5 V, 3.3 V)	LV _{DD1}	9
LV _{DD2}	B18, E21	Power for UCC2 Ethernet interface option 2 (2.5 V, 3.3 V)	LV _{DD2}	9
V _{DD}	C36, D29, D35, E16, F9, F12, F15, F17, F18, F20, F21, F23, F25, F26, F29, F31, F32, F33, G6, J6, K32, M32, N6, P33, R6, R32, U32, V6, Y5, Y32, AB6, AB33, AD6, AF32, AK6, AL6, AM7, AM9, AM10, AM11, AM12, AM13, AM14, AM15, AM18, AM21, AM25, AM28, AM32, AN15, AN21, AN26, AU9, AU17	Power for core (1.2 V)	V _{DD}	—
OV _{DD}	A10, B9, B15, B32, C1, C12, C22, C29, D24, E3, E10, E27, G4, H35, J1, J35, K2, M4, N3, N34, R2, R37, T36, U2, U33, V4, V34, W3, Y35, Y37, AA1, AA36, AB2, AB34	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV _{DD}	—
MVREF1	AN20	I	DDR reference voltage	—
MVREF2	AU32	I	DDR reference voltage	—
SPARE1	B11	I/O	OV _{DD}	8
SPARE3	AH32	—	GV _{DD}	8
SPARE4	AU18	—	GV _{DD}	7
SPARE5	AP1	—	GV _{DD}	8

Table 67. MPC8358E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MWE	AT26	O	GV _{DD}	—
MEMC_MRAS	AT29	O	GV _{DD}	—
MEMC_MCAS	AT24	O	GV _{DD}	—
MEMC_MCS[0:3]	AU27, AT27, AU8, AU7	O	GV _{DD}	—
MEMC_MCKE[0:1]	AL32, AU33	O	GV _{DD}	3
MEMC_MCK[0:5]	AK37, AT37, AN1, AR2, AN25, AK1	O	GV _{DD}	—
MEMC_MCK[0:5]	AL37, AT36, AP2, AT2, AN24, AL1	O	GV _{DD}	—
MDIC[0:1]	AH6, AP30	I/O	GV _{DD}	11
PCI				
PCI_INTA/IRQ_OUT/CE_PF[5]	A20	I/O	LV _{DD2}	2
PCI_RESET_OUT/CE_PF[6]	E19	I/O	LV _{DD2}	—
PCI_AD[31:30]/CE_PG[31:30]	D20, D21	I/O	LV _{DD2}	—
PCI_AD[29:25]/CE_PG[29:25]	A24, B23, C23, E23, A26	I/O	OV _{DD}	—
PCI_AD[24]/CE_PG[24]	B21	I/O	LV _{DD2}	—
PCI_AD[23:0]/CE_PG[23:0]	C24, C25, D25, B25, E24, F24, A27, A28, F27, A30, C30, D30, E29, B31, C31, D31, D32, A32, C33, B33, F30, E31, A34, D33	I/O	OV _{DD}	—
PCI_C/BE[3:0]/CE_PF[10:7]	E22, B26, E28, F28	I/O	OV _{DD}	—
PCI_PAR/CE_PF[11]	D28	I/O	OV _{DD}	—
PCI_FRAME/CE_PF[12]	D26	I/O	OV _{DD}	5
PCI_TRDY/CE_PF[13]	C27	I/O	OV _{DD}	5
PCI_IRDY/CE_PF[14]	C28	I/O	OV _{DD}	5
PCI_STOP/CE_PF[15]	B28	I/O	OV _{DD}	5
PCI_DEVSEL/CE_PF[16]	E26	I/O	OV _{DD}	5
PCI_IDSEL/CE_PF[17]	F22	I/O	OV _{DD}	—
PCI_SERR/CE_PF[18]	B29	I/O	OV _{DD}	5
PCI_PERR/CE_PF[19]	A29	I/O	OV _{DD}	5
PCI_REQ[0]/CE_PF[20]	F19	I/O	LV _{DD2}	—
PCI_REQ[1]/CPCI_HS_ES/ CE_PF[21]	A21	I/O	LV _{DD2}	—
PCI_REQ[2]/CE_PF[22]	C21	I/O	LV _{DD2}	—
PCI_GNT[0]/CE_PF[23]	E20	I/O	LV _{DD2}	—
PCI_GNT[1]/CPCI1_HS_LED/ CE_PF[24]	B20	I/O	LV _{DD2}	—
PCI_GNT[2]/CPCI1_HS_ENUM/ CE_PF[25]	C20	I/O	LV _{DD2}	—

Table 70. System PLL Multiplication Factors (continued)

RCWL[SPMF]	System PLL Multiplication Factor
1100	× 12
1101	× 13
1110	× 14
1111	× 15

The RCWL[SVCOD] denotes the system PLL VCO internal frequency as shown in this table.

Table 71. System PLL VCO Divider

RCWL[SVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider must be set properly so that the system VCO frequency is in the range of 600–1400 MHz.

The system VCO frequency is derived from the following equations:

- $csb_clk = \{PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)\} \times SPMF$
- System VCO Frequency = $csb_clk \times$ VCO divider (if both RCWL[DDRCM] and RCWL[LBCM] are cleared)
OR
- System VCO frequency = $2 \times csb_clk \times$ VCO divider (if either RCWL[DDRCM] or RCWL[LBCM] are set).

As described in [Section 21, “Clocking,”](#) the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (csb_clk). This table shows the expected frequency values for the CSB frequency for select csb_clk to CLKIN/PCI_SYNC_IN ratios.

Table 72. CSB Frequency Options

CFG_CLKIN_DIV at Reset ¹	SPMF	csb_clk : Input Clock Ratio ²	Input Clock Frequency (MHz) ²			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2:1				133
Low	0011	3:1				200
Low	0100	4:1				266
Low	0101	5:1				333

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JA}$ = junction to board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

22.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

22.2.4 Heat Sinks and Junction-to-Ambient Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the airflow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, airflow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

This table shows heat sinks and junction-to-ambient thermal resistance for TBGA package.

Table 78. Heat Sinks and Junction-to-Ambient Thermal Resistance of TBGA Package

Heat Sink Assuming Thermal Grease	Airflow	35 × 35 mm TBGA
		Junction-to-Ambient Thermal Resistance
AAVID 30 × 30 × 9.4 mm pin fin	Natural convention	10.7
AAVID 30 × 30 × 9.4 mm pin fin	1 m/s	6.2
AAVID 30 × 30 × 9.4 mm pin fin	2 m/s	5.3
AAVID 31 × 35 × 23 mm pin fin	Natural convention	8.1
AAVID 31 × 35 × 23 mm pin fin	1 m/s	4.4
AAVID 31 × 35 × 23 mm pin fin	2 m/s	3.7
Wakefield, 53 × 53 × 25 mm pin fin	Natural convention	5.4
Wakefield, 53 × 53 × 25 mm pin fin	1 m/s	3.2
Wakefield, 53 × 53 × 25 mm pin fin	2 m/s	2.4
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural convention	6.4
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	3.8
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	2.5
MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass	1 m/s	2.8

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following:

Aavid Thermalloy 603-224-9988
 80 Commercial St.
 Concord, NH 03301
 Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
 473 Sapena Ct. #15
 Santa Clara, CA 95054
 Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
 413 North Moss St.
 Burbank, CA 91502
 Internet: www.ctscorp.com

23.7 Pull-Up Resistor Requirements

The device requires high resistance pull-up resistors (10 k Ω is recommended) on open drain type pins including I²C pins, Ethernet Management MDIO pin, and EPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, see *MPC8360E/MPC8358E PowerQUICC Design Checklist* (AN3097).

24 Ordering Information

24.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the MPC8360E/58E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. Additionally to the processor frequency, the part numbering scheme also includes an application modifier, which may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number.

Table 80. Part Numbering Nomenclature¹

<i>MPC</i>	<i>nnnn</i>	<i>e</i>	<i>t</i>	<i>pp</i>	<i>aa</i>	<i>a</i>	<i>a</i>	<i>A</i>
Product Code	Part Identifier	Encryption Acceleration	Temperature Range	Package ²	Processor Frequency ³	Platform Frequency	QUICC Engine Frequency	Die Revision
MPC	8358	Blank = not included E = included	Blank = 0° C T _A to 105° C T _J C = -40° C T _A to 105° C T _J	ZU = TBGA VV = TBGA (no lead)	e300 core speed AD = 266 MHz AG = 400 MHz	D = 266 MHz	E = 300 MHz G = 400 MHz	A = rev. 2.1 silicon
	8360				e300 core speed AG = 400 MHz AJ = 533 MHz AL = 667 MHz	D = 266 MHz F = 333 MHz	G = 400 MHz H = 500 MHz	A = rev. 2.1 silicon
MPC (rev. 2.0 silicon only)	8360	Blank = not included E = included	0° C T _A to 70° C T _J	ZU = TBGA VV = TBGA (no lead)	e300 core speed AH = 500 MHz AL = 667 MHz	F = 333 MHz	G = 400 MHz H = 500 MHz	—

Notes:

1. Not all processor, platform, and QUICC Engine block frequency combinations are supported. For available frequency combinations, contact your local Freescale sales office or authorized distributor.
2. See [Section 20, "Package and Pin Listings,"](#) for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

This table shows the SVR settings by device and package type.

Table 81. SVR Settings

Device	Package	SVR (Rev. 2.0)	SVR (Rev. 2.1)
MPC8360E	TBGA	0x8048_0020	0x8048_0021
MPC8360	TBGA	0x8049_0020	0x8049_0021