
**Welcome to E-XFL.COM**

## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e300 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 667MHz |
| Co-Processors/DSP | Communications; QUICC Engine |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (1) |
| SATA | - |
| USB | USB 1.x (1) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 740-LBGA |
| Supplier Device Package | 740-TBGA (37.5x37.5) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8360zualfg |

# 2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

## 2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

**Table 1. Absolute Maximum Ratings[1]**

| Characteristic | | Symbol | Max Value | Unit | Notes |
|---|---|---|---|---|---|
| Core and PLL supply voltage for<br><br>MPC8358 Device Part Number with<br>Processor Frequency label of AD=266MHz and AG=400MHz &<br>QUICC Engine Frequency label of E=300MHz & G=400MHz<br><br>MPC8360 Device Part Number with<br>Processor Frequency label of AG=400MHz and AJ=533MHz &<br>QUICC Engine Frequency label of G=400MHz | | $V_{DD}$ & $AV_{DD}$ | –0.3 to 1.32 | V | — |
| Core and PLL supply voltage for<br><br>MPC8360 device Part Number with<br>Processor Frequency label of AL=667MHz and QUICC Engine<br>Frequency label of H=500MHz | | $V_{DD}$ & $AV_{DD}$ | –0.3 to 1.37 | V | — |
| DDR and DDR2 DRAM I/O voltage<br>DDR<br>DDR2 | | $GV_{DD}$ | <br>–0.3 to 2.75<br>–0.3 to 1.89 | V | — |
| Three-speed Ethernet I/O, MII management voltage | | $LV_{DD}$ | –0.3 to 3.63 | V | — |
| PCI, local bus, DUART, system control and power management, $I^2C$, SPI, and JTAG I/O voltage | | $OV_{DD}$ | –0.3 to 3.63 | V | — |
| Input voltage | DDR DRAM signals | $MV_{IN}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 2, 5 |
| | DDR DRAM reference | $MV_{REF}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 2, 5 |
| | Three-speed Ethernet signals | $LV_{IN}$ | –0.3 to ($LV_{DD}$ + 0.3) | V | 4, 5 |
| | Local bus, DUART, CLKIN, system control and power management, $I^2C$, SPI, and JTAG signals | $OV_{IN}$ | –0.3 to ($OV_{DD}$ + 0.3) | V | 3, 5 |
| | PCI | $OV_{IN}$ | –0.3 to ($OV_{DD}$ + 0.3) | V | 6 |

**Table 4. MPC8360E TBGA Core Power Dissipation[1] (continued)**

| Core Frequency (MHz) | CSB Frequency (MHz) | QUICC Engine Frequency (MHz) | Typical | Maximum | Unit | Notes |
|---|---|---|---|---|---|---|
| 667 | 333 | 500 | 6.1 | 6.8 | W | 2, 3, 5, 9 |

**Notes:**
1. The values do not include I/O supply power ($OV_{DD}$, $LV_{DD}$, $GV_{DD}$) or $AV_{DD}$. For I/O power values, see Table 6.
2. Typical power is based on a voltage of $V_{DD}$ = 1.2 V or 1.3 V, a junction temperature of $T_J$ = 105° C, and a Dhrystone benchmark application.
3. Thermal solutions need to design to a value higher than typical power on the end application, $T_A$ target, and I/O power.
4. Maximum power is based on a voltage of $V_{DD}$ = 1.2 V, WC process, a junction $T_J$ = 105° C, and an artificial smoke test.
5. Maximum power is based on a voltage of $V_{DD}$ = 1.3 V for applications that use 667 MHz (CPU)/500 (QE) with WC process, a junction $T_J$ = 105° C, and an artificial smoke test.
6. Typical power is based on a voltage of $V_{DD}$ = 1.3 V, a junction temperature of $T_J$ = 70° C, and a Dhrystone benchmark application.
7. Maximum power is based on a voltage of $V_{DD}$ = 1.3 V for applications that use 667 MHz (CPU) or 500 (QE) with WC process, a junction $T_J$ = 70° C, and an artificial smoke test.
8. This frequency combination is only available for rev. 2.0 silicon.
9. This frequency combination is not available for rev. 2.0 silicon.

**Table 5. MPC8358E TBGA Core Power Dissipation[1]**

| Core Frequency (MHz) | CSB Frequency (MHz) | QUICC Engine Frequency (MHz) | Typical | Maximum | Unit | Notes |
|---|---|---|---|---|---|---|
| 266 | 266 | 300 | 4.1 | 4.5 | W | 2, 3, 4 |
| 400 | 266 | 400 | 4.5 | 5.0 | W | 2, 3, 4 |

**Notes:**
1. The values do not include I/O supply power ($OV_{DD}$, $LV_{DD}$, $GV_{DD}$) or $AV_{DD}$. For I/O power values, see Table 6.
2. Typical power is based on a voltage of $V_{DD}$ = 1.2 V, a junction temperature of $T_J$ = 105° C, and a Dhrystone benchmark application.
3. Thermal solutions need to design to a value higher than typical power on the end application, $T_A$ target, and I/O power.
4. Maximum power is based on a voltage of $V_{DD}$ = 1.2 V, WC process, a junction $T_J$ = 105° C, and an artificial smoke test.

**Table 9. GTX_CLK125 AC Timing Specifications**

**At recommended operating conditions with $LV_{DD}$ = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV (continued)**

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| GTX_CLK rise and fall time<br>$LV_{DD}$ = 2.5 V<br>$LV_{DD}$ = 3.3 V | $t_{G125R}/t_{G125F}$ | — | — | <br>0.75<br>1.0 | ns | 1 |
| GTX_CLK125 duty cycle<br>GMII & TBI<br>1000Base-T for RGMII & RTBI | $t_{G125H}/t_{G125}$ | <br>45<br>47 | — | <br>55<br>53 | % | 2 |
| GTX_CLK125 jitter | — | — | — | ±150 | ps | 2 |

**Notes:**

1. Rise and fall times for GTX_CLK125 are measured from 0.5 and 2.0 V for $LV_{DD}$ = 2.5 V and from 0.6 and 2.7 V for $LV_{DD}$ = 3.3 V.
2. GTX_CLK125 is used to generate the GTX clock for the UCC Ethernet transmitter with 2% degradation. The GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by GTX_CLK. See Section 8.2.2, “MII AC Timing Specifications,” Section 8.2.3, “RMII AC Timing Specifications,” and Section 8.2.5, “RGMII and RTBI AC Timing Specifications” for the duty cycle for 10Base-T and 100Base-T reference clock.

# 5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8360E/58E.

## 5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins of the device.

**Table 10. RESET Pins DC Electrical Characteristics [1]**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | 2.0 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | — | — | ±10 | μA |
| Output high voltage | $V_{OH}$[2] | $I_{OH}$ = –8.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |

**Notes:**

1. This table applies for pins $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, and $\overline{\text{QUIESCE}}$.
2. $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are open drain pins, thus $V_{OH}$ is not relevant for those pins.

## 6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 21 and Table 22 provide the output AC timing specifications and measurement conditions for the DDR and DDR2 SDRAM interface.

**Table 21. DDR and DDR2 SDRAM Output AC Timing Specifications for Source Synchronous Mode**

At recommended operating conditions with $GV_{DD}$ of (1.8 V or 2.5 V) ± 5%.

| Parameter[8] | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| MCK[n] cycle time, (MCK[n]/$\overline{\text{MCK}}$[n] crossing) | $t_{MCK}$ | 6 | 10 | ns | 2 |
| Skew between any MCK to ADDR/CMD<br>333 MHz<br>266 MHz<br>200 MHz | $t_{AOSKEW}$ | <br>–1.0<br>–1.1<br>–1.2 | <br>0.2<br>0.3<br>0.4 | ns | 3 |
| ADDR/CMD output setup with respect to MCK<br>333 MHz<br>266 MHz<br>200 MHz | $t_{DDKHAS}$ | <br>2.1<br>2.8<br>3.5 | — | ns | 4 |
| ADDR/CMD output hold with respect to MCK<br>333 MHz<br>266 MHz—DDR1<br>266 MHz—DDR2<br>200 MHz | $t_{DDKHAX}$ | <br>2.0<br>2.7<br>2.8<br>3.5 | — | ns | 4 |
| $\overline{\text{MCS}}$(n) output setup with respect to MCK<br>333 MHz<br>266 MHz<br>200 MHz | $t_{DDKHCS}$ | <br>2.1<br>2.8<br>3.5 | — | ns | 4 |
| $\overline{\text{MCS}}$(n) output hold with respect to MCK<br>333 MHz<br>266 MHz<br>200 MHz | $t_{DDKHCX}$ | <br>2.0<br>2.7<br>3.5 | — | ns | 4 |
| MCK to MDQS | $t_{DDKHMH}$ | –0.8 | 0.7 | ns | 5, 9 |
| MDQ/MECC/MDM output setup with respect to MDQS<br>333 MHz<br>266 MHz<br>200 MHz | $t_{DDKHDS}$, $t_{DDKLDS}$ | <br>0.7<br>1.0<br>1.2 | — | ns | 6 |
| MDQ/MECC/MDM output hold with respect to MDQS<br>333 MHz<br>266 MHz<br>200 MHz | $t_{DDKHDX}$, $t_{DDKLDX}$ | <br>0.7<br>1.0<br>1.2 | — | ns | 6 |
| MDQS preamble start | $t_{DDKHMP}$ | $-0.5 \times t_{MCK} - 0.6$ | $-0.5 \times t_{MCK} + 0.6$ | ns | 7 |

This figure provides the AC test load for the DDR bus.

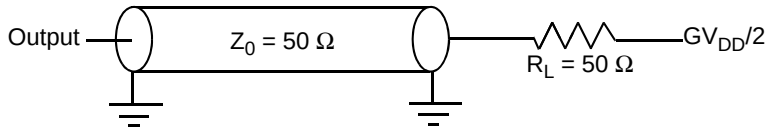


**Figure 8. DDR AC Test Load**

**Table 22. DDR and DDR2 SDRAM Measurement Conditions**

| Symbol | DDR | DDR2 | Unit | Notes |
|---|---|---|---|---|
| $V_{TH}$ | $MV_{REF}$ ± 0.31 V | $MV_{REF}$ ± 0.25 V | V | 1 |
| $V_{OUT}$ | 0.5 × $GV_{DD}$ | 0.5 × $GV_{DD}$ | V | 2 |

**Notes:**
1. Data input threshold measurement point.
2. Data output measurement point.

This figure shows the DDR SDRAM output timing diagram for source synchronous mode.

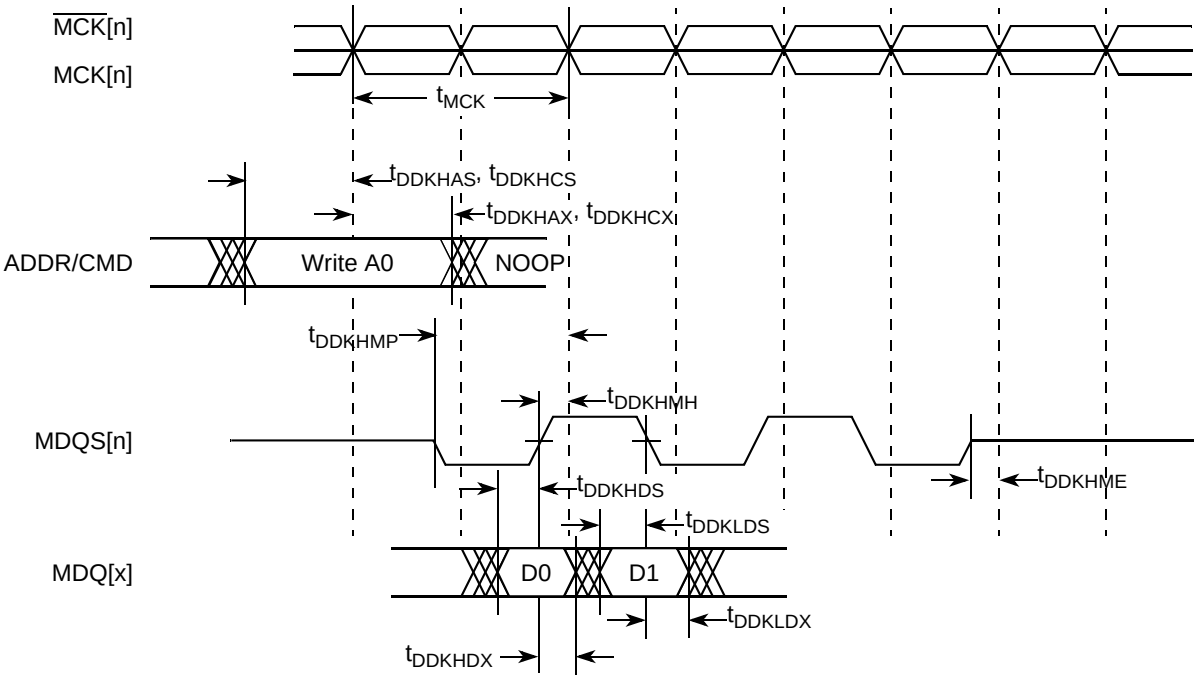


**Figure 9. DDR SDRAM Output Timing Diagram for Source Synchronous Mode**

## 8.3.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

**Table 37. MII Management AC Timing Specifications**

At recommended operating conditions with $LV_{DD}$ is 3.3 V ± 10%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| MDC frequency | $f_{MDC}$ | — | 2.5 | — | MHz | 2 |
| MDC period | $t_{MDC}$ | — | 400 | — | ns | — |
| MDC clock pulse width high | $t_{MDCH}$ | 32 | — | — | ns | — |
| MDC to MDIO delay | $t_{MDTKHDX}$<br>$t_{MDTKHDV}$ | 10<br>— | — | —<br>110 | ns | 3 |
| MDIO to MDC setup time | $t_{MDRDVKH}$ | 10 | — | — | ns | — |
| MDIO to MDC hold time | $t_{MDRDXKH}$ | 0 | — | — | ns | — |
| MDC rise time | $t_{MDCR}$ | — | — | 10 | ns | — |
| MDC fall time | $t_{MDHF}$ | — | — | 10 | ns | — |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MDKHDX}$ symbolizes management data timing (MD) for the time $t_{MDC}$ from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDRDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MDC}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
3. This parameter is dependent on the ce_clk speed (that is, for a ce_clk of 200 MHz, the delay is 90 ns and for a ce_clk of 300 MHz, the delay is 63 ns).

This figure shows the MII management AC timing diagram.

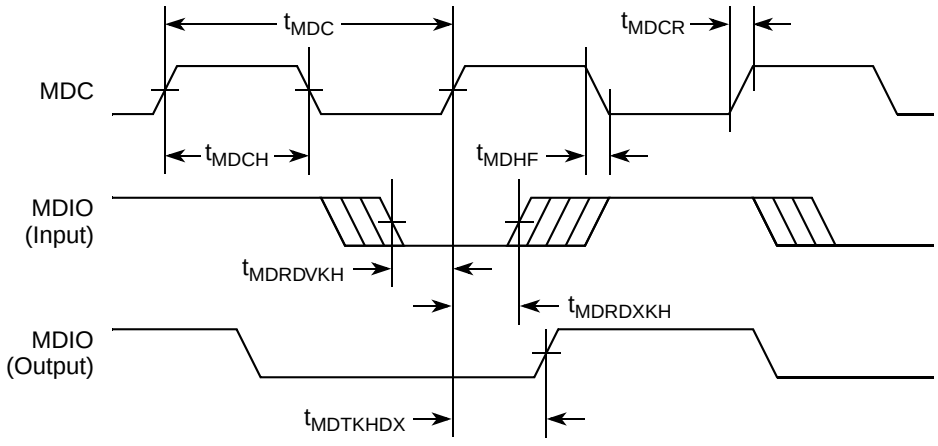


**Figure 21. MII Management Interface Timing Diagram**

These figures show the local bus signals.

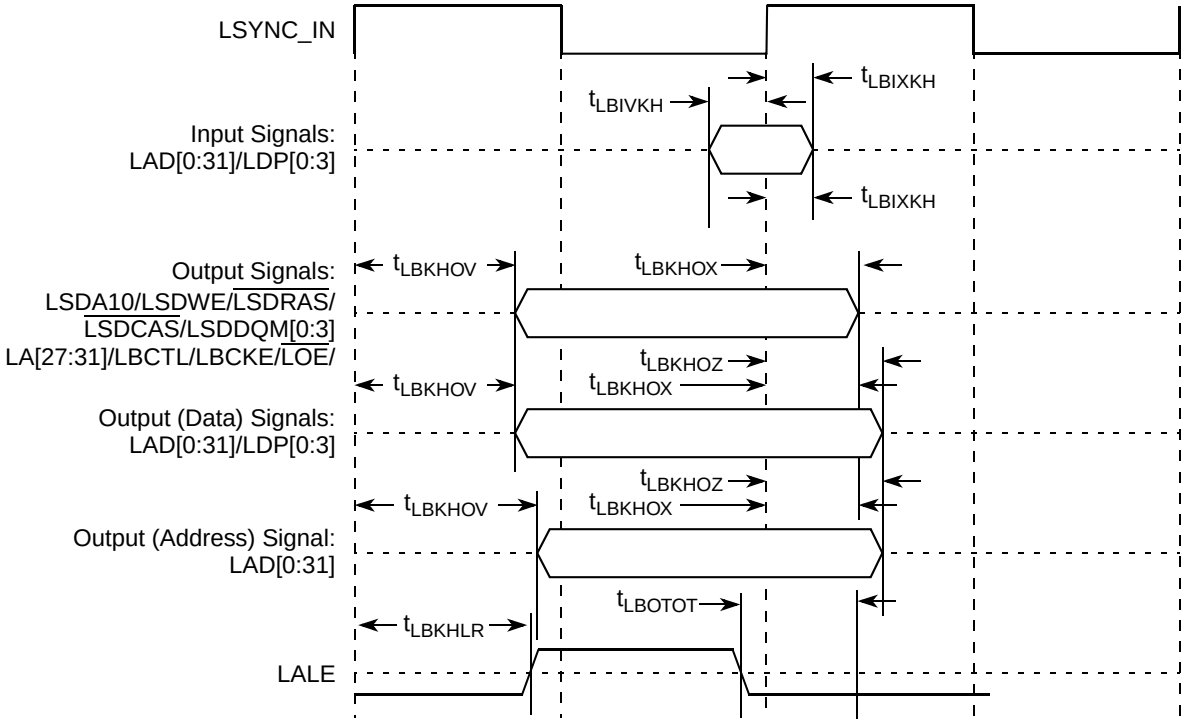


**Figure 23. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)**

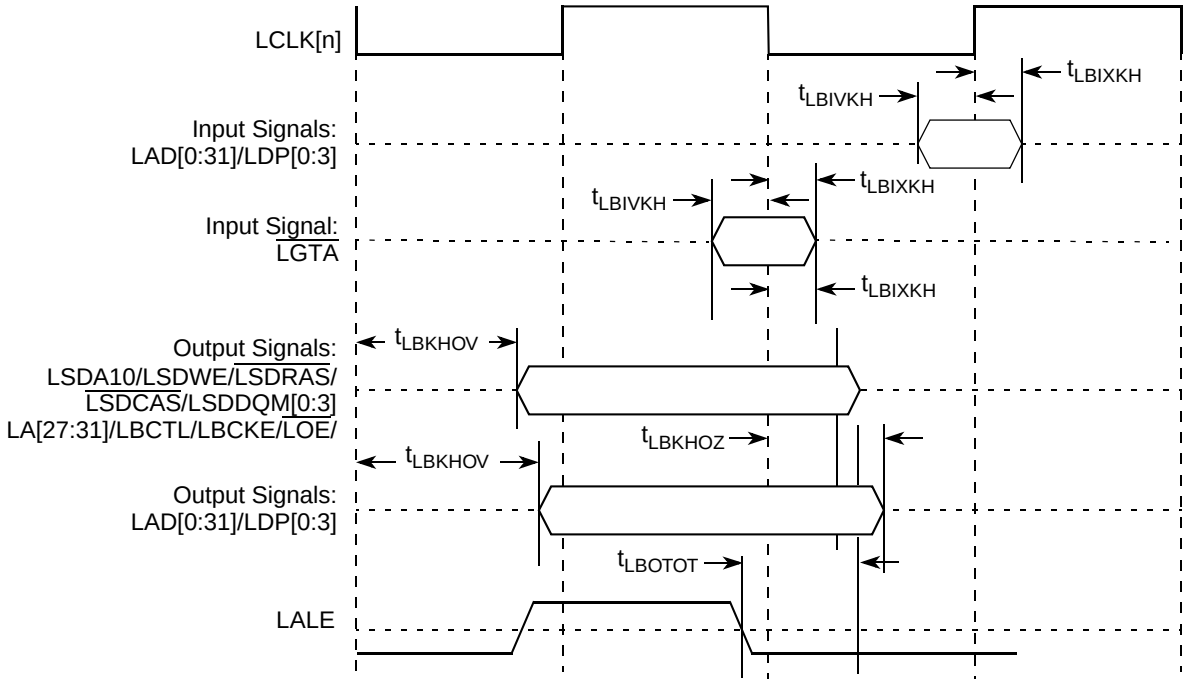


**Figure 24. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)**

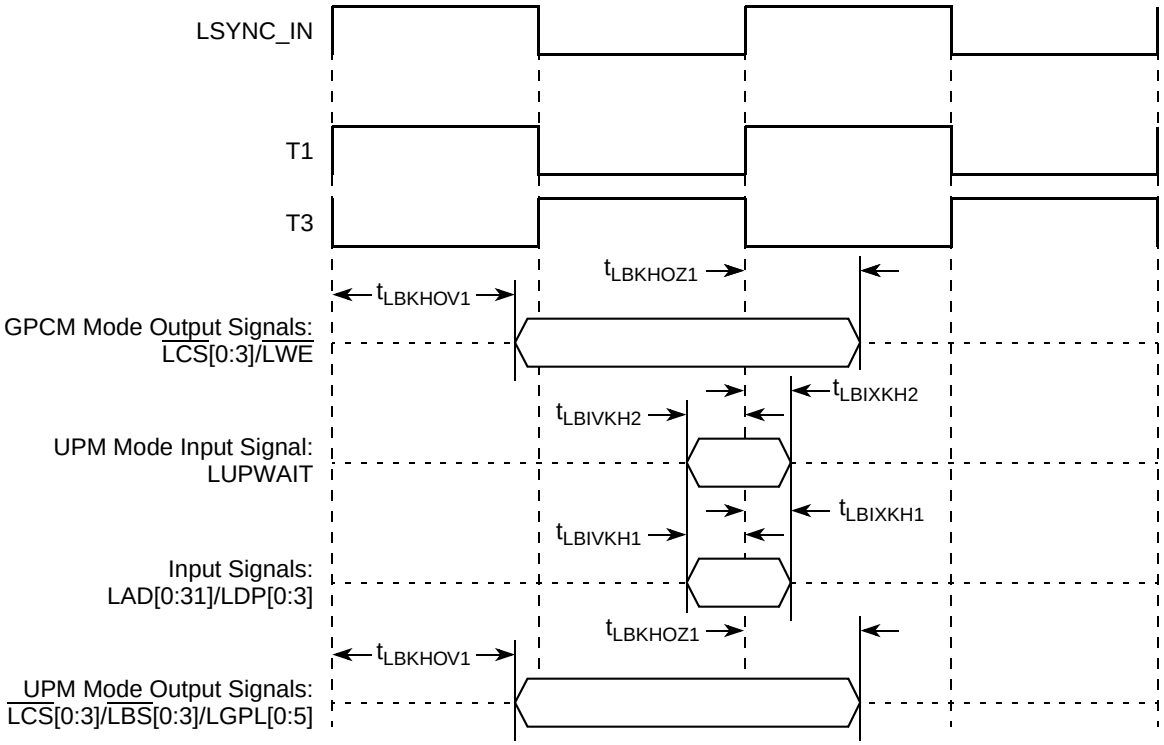


**Figure 25. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Enabled)**

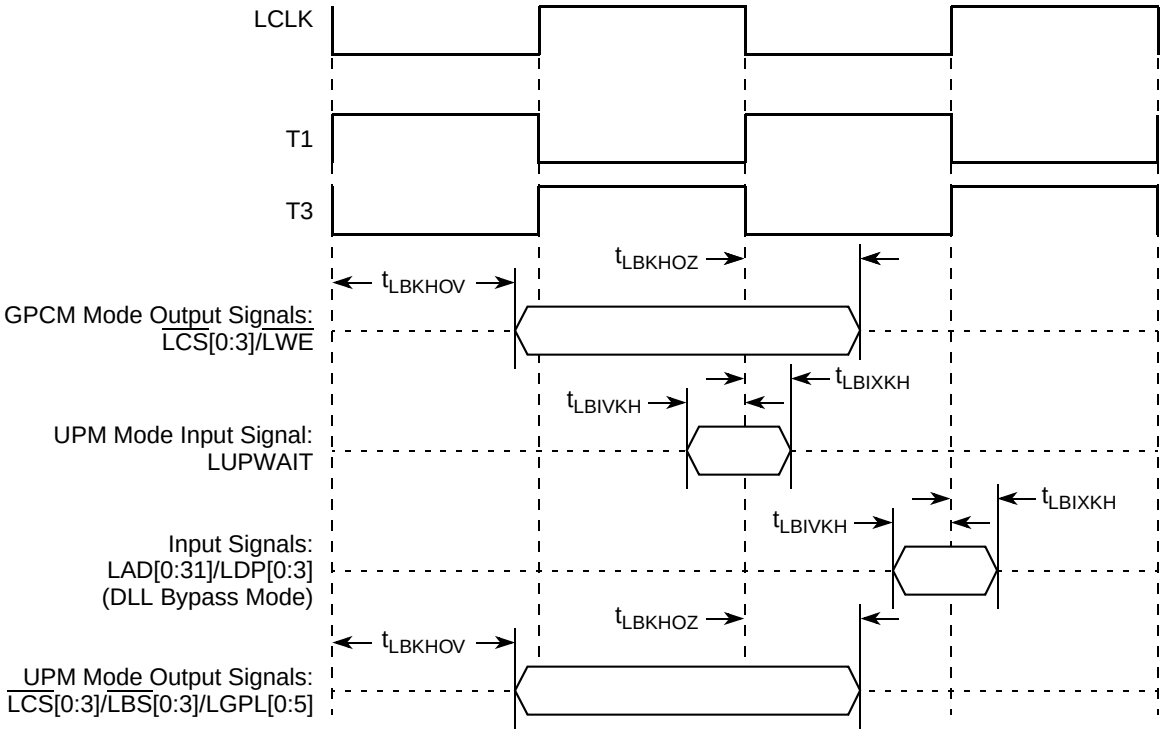


**Figure 26. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (DLL Bypass Mode)**

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.

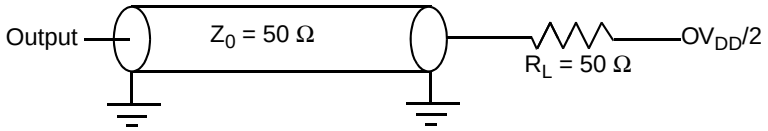


**Figure 29. AC Test Load for the JTAG Interface**

This figure provides the JTAG clock input timing diagram.

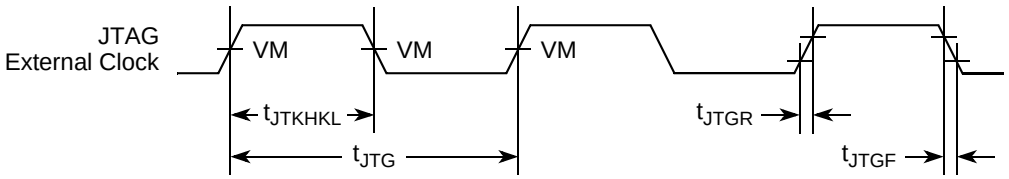


**Figure 30. JTAG Clock Input Timing Diagram**

This figure provides the $\overline{\text{TRST}}$ timing diagram.

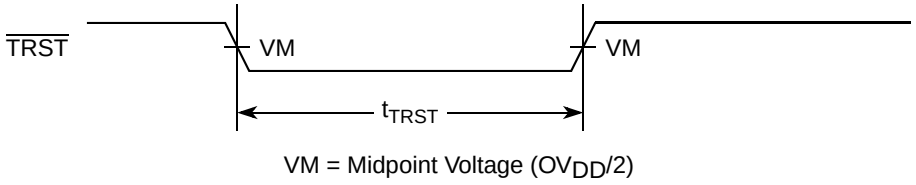


**Figure 31. $\overline{\text{TRST}}$ Timing Diagram**

This figure provides the boundary-scan timing diagram.

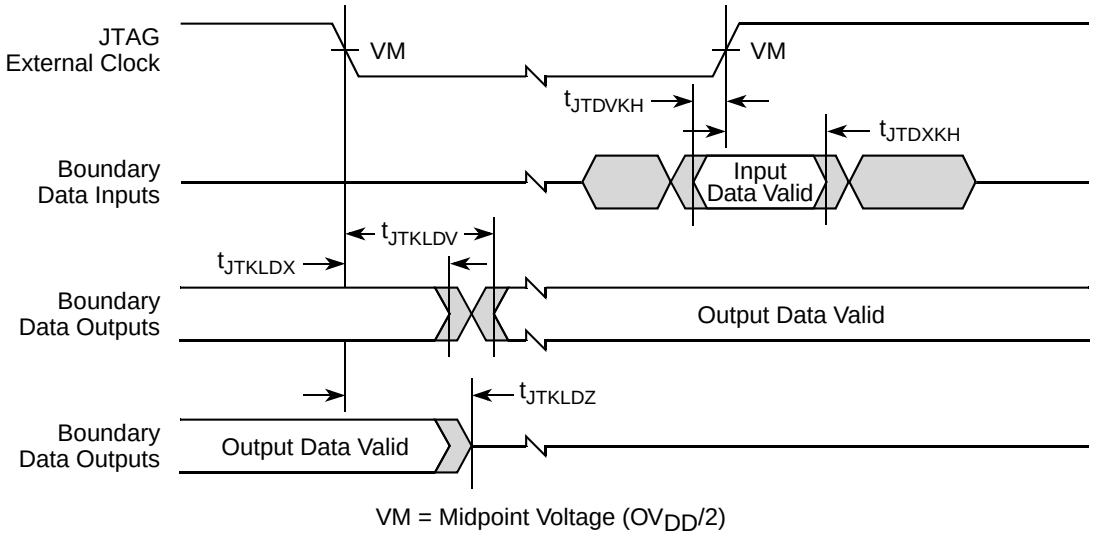


**Figure 32. Boundary-Scan Timing Diagram**

## 13.2 Timers AC Timing Specifications

This table provides the timer input and output AC timing specifications.

**Table 50. Timers Input AC Timing Specifications[1]**

| Characteristic | Symbol[2] | Typ | Unit |
|---|---|---|---|
| Timers inputs—minimum pulse width | $t_{TIWID}$ | 20 | ns |

**Notes:**
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least $t_{TIWID}$ ns to ensure proper operation.

This figure provides the AC test load for the timers.

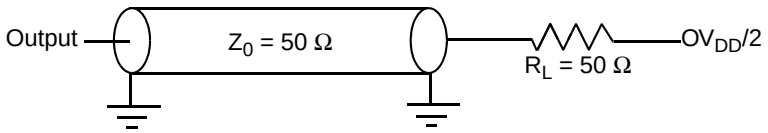


**Figure 39. Timers AC Test Load**

# 14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8360E/58E.

## 14.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the device GPIO.

**Table 51. GPIO DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –6.0 mA | 2.4 | — | V | 1 |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 6.0 mA | — | 0.5 | V | 1 |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V | 1 |
| Input high voltage | $V_{IH}$ | — | 2.0 | $OV_{DD}$ + 0.3 | V | 1 |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V | — |
| Input current | $I_{IN}$ | 0 V ≤$V_{IN}$ ≤$OV_{DD}$ | — | ±10 | μA | — |

**Note:**
1. This specification applies when operating from 3.3-V supply.

**Table 66. MPC8360E TBGA Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **No Connect** | | | | |
| NC | AM20, AU19 | — | — | — |

**Notes:**
1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to $OV_{DD}$
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to $OV_{DD}$.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. These are On Die Termination pins, used to control DDR2 memories internal termination resistance.
7. This pin must always be tied to GND.
8. This pin must always be left not connected.
9. Refer to *MPC8360E PowerQUICC II Pro Integrated Communications Processor Reference Manual* section on "RGMII Pins," for information about the two UCC2 Ethernet interface options.
10. It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor for DDR2.

This table shows the pin list of the MPC8358E TBGA package.

**Table 67. MPC8358E TBGA Pinout Listing**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **DDR SDRAM Memory Controller Interface** | | | | |
| MEMC1_MDQ[0:63] | AJ34, AK33, AL33, AL35, AJ33, AK34, AK32, AM36, AN37, AN35, AR34, AT34, AP37, AP36, AR36, AT35, AP34, AR32, AP32, AM31, AN33, AM34, AM33, AM30, AP31, AM27, AR30, AT32, AN29, AP29, AN27, AR29, AN8, AN7, AM8, AM6, AP9, AN9, AT7, AP7, AU6, AP6, AR4, AR3, AT6, AT5, AR5, AT3, AP4, AM5, AP3, AN3, AN5, AL5, AN4, AM2, AL2, AH5, AK3, AJ2, AJ3, AH4, AK4, AH3 | I/O | $GV_{DD}$ | — |
| MEMC_MECC[0:4]/MSRCID[0:4] | AP24, AN22, AM19, AN19, AM24 | I/O | $GV_{DD}$ | — |
| MEMC_MECC[5]/MDVAL | AM23 | I/O | $GV_{DD}$ | — |
| MEMC_MECC[6:7] | AM22, AN18 | I/O | $GV_{DD}$ | — |
| MEMC_MDM[0:8] | AL36, AN34, AP33, AN28,AT9, AU4, AM3, AJ6,AP27 | O | $GV_{DD}$ | — |
| MEMC_MDQS[0:8] | AK35, AP35, AN31, AM26,AT8, AU3, AL4, AJ5, AP26 | I/O | $GV_{DD}$ | — |
| MEMC_MBA[0:1] | AU29, AU30 | O | $GV_{DD}$ | |
| MEMC_MBA[2] | AT30 | O | $GV_{DD}$ | — |
| MEMC_MA[0:14] | AU21, AP22, AP21, AT21, AU25, AU26, AT23, AR26, AU24, AR23, AR28, AU23, AR22, AU20, AR18 | O | $GV_{DD}$ | — |
| MEMC_MODT[0:3] | AG33, AJ36, AT1, AK2 | O | $GV_{DD}$ | 6 |

**Table 67. MPC8358E TBGA Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| PCI_MODE | D36 | I | $OV_{DD}$ | — |
| M66EN/CE_PF[4] | B37 | I/O | $OV_{DD}$ | — |
| **Local Bus Controller Interface** | | | | |
| LAD[0:31] | N32, N33, N35, N36, P37, P32, P34, R36, R35, R34, R33, T37, T35, T34, T33, U37, T32, U36, U34, V36, V35, W37, W35, V33, V32, W34, Y36, W32, AA37, Y33, AA35, AA34 | I/O | $OV_{DD}$ | — |
| LDP[0]/CKSTOP_OUT | AB37 | I/O | $OV_{DD}$ | — |
| LDP[1]/CKSTOP_IN | AB36 | I/O | $OV_{DD}$ | — |
| LDP[2]/LCS[6] | AB35 | I/O | $OV_{DD}$ | — |
| LDP[3]/LCS[7] | AA33 | I/O | $OV_{DD}$ | — |
| LA[27:31] | AC37, AA32, AC36, AC34, AD36 | O | $OV_{DD}$ | — |
| LCS[0:5] | AD33, AG37, AF34, AE33, AD32, AH37 | O | $OV_{DD}$ | — |
| LWE[0:3]/LSDDQM[0:3]/LBS[0:3] | AG35, AG34, AH36, AE32 | O | $OV_{DD}$ | — |
| LBCTL | AD35 | O | $OV_{DD}$ | — |
| LALE | M37 | O | $OV_{DD}$ | — |
| LGPL0/LSDA10/cfg_reset_source0 | AB32 | I/O | $OV_{DD}$ | — |
| LGPL1/LSDWE/cfg_reset_source1 | AE37 | I/O | $OV_{DD}$ | — |
| LGPL2/LSDRAS/LOE | AC33 | O | $OV_{DD}$ | — |
| LGPL3/LSDCAS/cfg_reset_source2 | AD34 | I/O | $OV_{DD}$ | — |
| LGPL4/LGTA/LUPWAIT/LPBSE | AE35 | I/O | $OV_{DD}$ | — |
| LGPL5/cfg_clkin_div | AF36 | I/O | $OV_{DD}$ | — |
| LCKE | G36 | O | $OV_{DD}$ | — |
| LCLK[0] | J33 | O | $OV_{DD}$ | — |
| LCLK[1]/LCS[6] | J34 | O | $OV_{DD}$ | — |
| LCLK[2]/LCS[7] | G37 | O | $OV_{DD}$ | — |
| LSYNC_OUT | F34 | O | $OV_{DD}$ | — |
| LSYNC_IN | G35 | I | $OV_{DD}$ | — |
| **Programmable Interrupt Controller** | | | | |
| MCP_OUT | E34 | O | $OV_{DD}$ | 2 |
| IRQ0/MCP_IN | C37 | I | $OV_{DD}$ | — |
| IRQ[1]/M1SRCID[4]/M2SRCID[4]/ LSRCID[4] | F35 | I/O | $OV_{DD}$ | — |
| IRQ[2]/M1DVAL/M2DVAL/LDVAL | F36 | I/O | $OV_{DD}$ | — |
| IRQ[3]/CORE_SRESET | H34 | I/O | $OV_{DD}$ | — |

**Table 67. MPC8358E TBGA Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| CE_PB[0:27] | AE2, AE1, AD5, AD3, AD2, AC6, AC5, AC4, AC2, AC1, AB5, AB4, AB3, AB1, AA6, AA4, AA2, Y6, Y4, Y3, Y2, Y1, W6, W5, W2, V5, V3, V2 | I/O | $OV_{DD}$ | — |
| CE_PC[0:1] | V1, U6 | I/O | $OV_{DD}$ | |
| CE_PC[2:3] | C16, A15 | I/O | $LV_{DD}1$ | — |
| CE_PC[4:6] | U4, U3, T6 | I/O | $OV_{DD}$ | — |
| CE_PC[7] | C19 | I/O | $LV_{DD}2$ | — |
| CE_PC[8:9] | A4, C5 | I/O | $LV_{DD}0$ | — |
| CE_PC[10:30] | T5, T4, T2, T1, R5, R3, R1, C11, D12, F13, B10, C10, E12, A9, B8, D10, A14, E15, B14, D15, AH2 | I/O | $OV_{DD}$ | — |
| CE_PD[0:27] | E11, D9, C8, F11, A7, E9, C7, A6, F10, B6, D7, E8, B5, A5, C2, E4, F5, B1, D2, G5, D1, E2, H6, F3, E1, F2, G3, H4 | I/O | $OV_{DD}$ | — |
| CE_PE[0:31] | K3, J2, F1, G2, J5, H3, G1, H2, K6, J3, K5, K4, L6, P6, P4, P3, P1, N4, N5, N2, N1, M2, M3, M5, M6, L1, L2, L4, E14, C13, C14, B13 | I/O | $OV_{DD}$ | — |
| CE_PF[0:3] | F14, D13, A12, A11 | I/O | $OV_{DD}$ | — |
| **Clocks** | | | | |
| PCI_CLK_OUT[0]/CE_PF[26] | B22 | I/O | $LV_{DD}2$ | — |
| PCI_CLK_OUT[1:2]/CE_PF[27:28] | D22, A23 | I/O | $OV_{DD}$ | — |
| CLKIN | E37 | I | $OV_{DD}$ | — |
| PCI_CLOCK/PCI_SYNC_IN | M36 | I | $OV_{DD}$ | — |
| PCI_SYNC_OUT/CE_PF[29] | D37 | I/O | $OV_{DD}$ | 3 |
| **JTAG** | | | | |
| TCK | K33 | I | $OV_{DD}$ | — |
| TDI | K34 | I | $OV_{DD}$ | 4 |
| TDO | H37 | O | $OV_{DD}$ | 3 |
| TMS | J36 | I | $OV_{DD}$ | 4 |
| $\overline{\text{TRST}}$ | L32 | I | $OV_{DD}$ | 4 |
| **Test** | | | | |
| TEST | L35 | I | $OV_{DD}$ | 7 |
| $\overline{\text{TEST\_SEL}}$ | AU34 | I | $GV_{DD}$ | 10 |
| **PMC** | | | | |
| $\overline{\text{QUIESCE}}$ | B36 | O | $OV_{DD}$ | — |
| **System Control** | | | | |

**Table 67. MPC8358E TBGA Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $\overline{\text{PORESET}}$ | L37 | I | $OV_{DD}$ | — |
| $\overline{\text{HRESET}}$ | L36 | I/O | $OV_{DD}$ | 1 |
| $\overline{\text{SRESET}}$ | M33 | I/O | $OV_{DD}$ | 2 |
| **Thermal Management** | | | | |
| THERM0 | AP19 | I | $GV_{DD}$ | — |
| THERM1 | AT31 | I | $GV_{DD}$ | — |
| **Power and Ground Signals** | | | | |
| $AV_{DD}1$ | K35 | Power for LBIU DLL (1.2 V) | $AV_{DD}1$ | — |
| $AV_{DD}2$ | K36 | Power for CE PLL (1.2 V) | $AV_{DD}2$ | — |
| $AV_{DD}5$ | AM29 | Power for e300 PLL (1.2 V) | $AV_{DD}5$ | — |
| $AV_{DD}6$ | K37 | Power for system PLL (1.2 V) | $AV_{DD}6$ | — |
| GND | A2, A8, A13, A19, A22, A25, A31, A33, A36, B7, B12, B24, B27, B30, C4, C6, C9, C15, C26, C32, D3, D8, D11, D14, D17, D19, D23, D27, E7, E13, E25, E30, E36, F4, F37, G34, H1, H5, H32, H33, J4, J32, J37, K1, L3, L5, L33, L34, M1, M34, M35, N37, P2, P5, P35, P36, R4, T3, U1, U5, U35, V37, W1, W4, W33, W36, Y34, AA3, AA5, AC3, AC32, AC35, AD1, AD37, AE4, AE34, AE36, AF33, AG4, AG6, AG32, AH35, AJ1, AJ4, AJ32, AJ35, AJ37, AK36, AL3, AL34, AM4, AN6, AN23, AN30, AP8, AP12, AP14, AP16, AP17, AP20, AP25, AR6, AR8, AR9, AR19, AR24, AR31, AR35, AR37, AT4, AT10, AT19, AT20, AT25, AU14, AU22, AU28, AU35 | — | — | — |
| $GV_{DD}$ | AD4, AE3, AF1, AF5, AF35, AF37, AG2, AG36, AH33, AH34, AK5, AM1, AM35, AM37, AN2, AN10, AN11, AN12, AN14, AN32, AN36, AP5, AP23, AP28, AR1, AR7, AR10, AR12, AR21, AR25, AR27, AR33, AT15, AT22, AT28, AT33, AU2, AU5, AU16, AU31, AU36 | Power for DDR DRAM I/O voltage (2.5 or 1.8 V) | $GV_{DD}$ | — |
| $LV_{DD}0$ | D5, D6 | Power for UCC1 Ethernet interface (2.5 V, 3.3 V) | $LV_{DD}0$ | — |

**Table 67. MPC8358E TBGA Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $LV_{DD}1$ | C17, D16 | Power for UCC2 Ethernet interface option 1 (2.5 V, 3.3 V) | $LV_{DD}1$ | 9 |
| $LV_{DD}2$ | B18, E21 | Power for UCC2 Ethernet interface option 2 (2.5 V, 3.3 V) | $LV_{DD}2$ | 9 |
| $V_{DD}$ | C36, D29, D35, E16, F9, F12, F15, F17, F18, F20, F21, F23, F25, F26, F29, F31, F32, F33, G6, J6, K32, M32, N6, P33, R6, R32, U32, V6, Y5, Y32, AB6, AB33, AD6, AF32, AK6, AL6, AM7, AM9, AM10, AM11, AM12, AM13, AM14, AM15, AM18, AM21, AM25, AM28, AM32, AN15, AN21, AN26, AU9, AU17 | Power for core (1.2 V) | $V_{DD}$ | — |
| $OV_{DD}$ | A10, B9, B15, B32, C1, C12, C22, C29, D24, E3, E10, E27, G4, H35, J1, J35, K2, M4, N3, N34, R2, R37, T36, U2, U33, V4, V34, W3, Y35, Y37, AA1, AA36, AB2, AB34 | PCI, 10/100 Ethernet, and other standard (3.3 V) | $OV_{DD}$ | — |
| MVREF1 | AN20 | I | DDR reference voltage | — |
| MVREF2 | AU32 | I | DDR reference voltage | — |
| | | | | |
| SPARE1 | B11 | I/O | $OV_{DD}$ | 8 |
| SPARE3 | AH32 | — | $GV_{DD}$ | 8 |
| SPARE4 | AU18 | — | $GV_{DD}$ | 7 |
| SPARE5 | AP1 | — | $GV_{DD}$ | 8 |

# 21 Clocking

This figure shows the internal distribution of clocks within the MPC8360E.

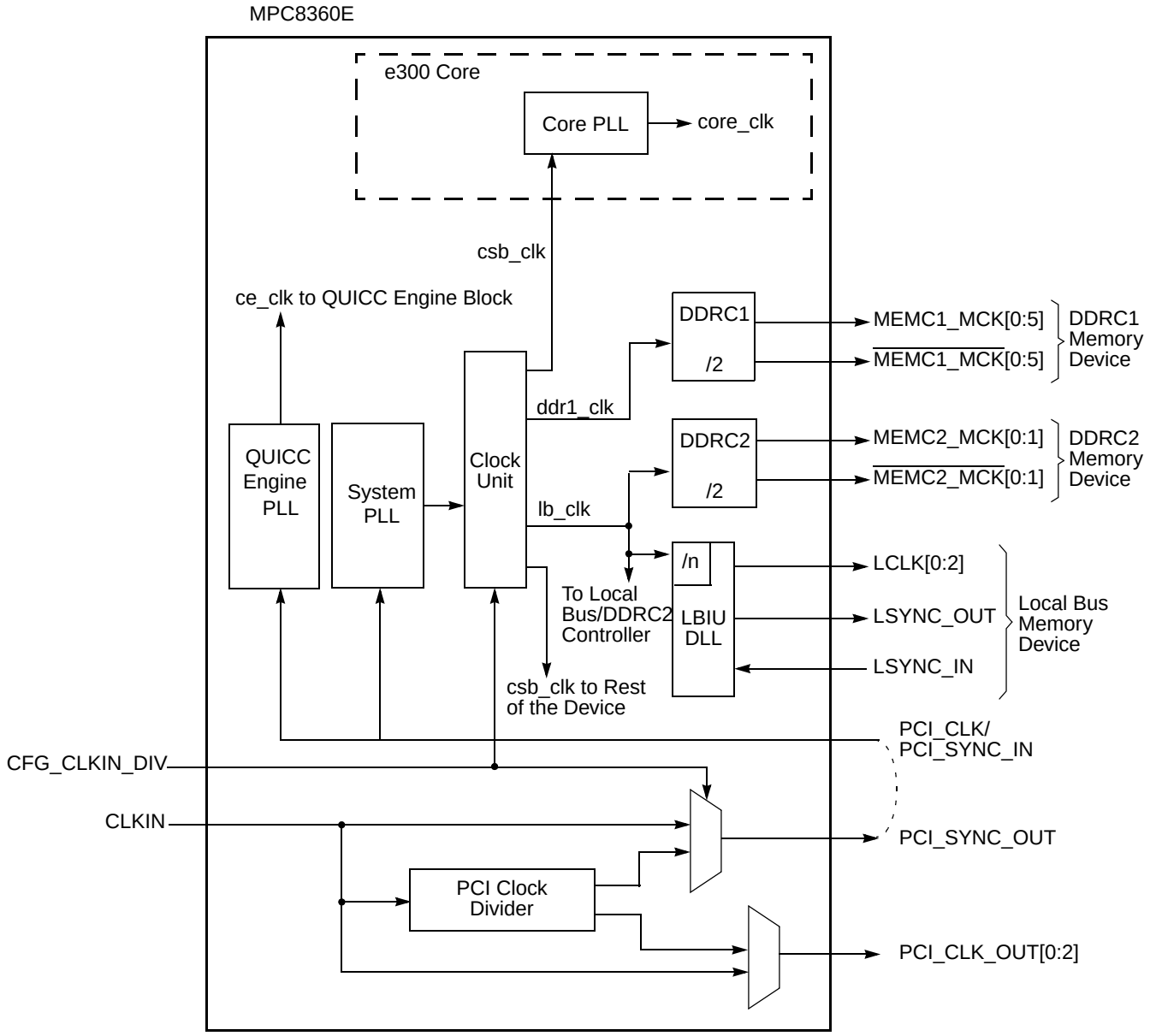


**Figure 54. MPC8360E Clock Subsystem**

## 21.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). This table shows the encodings for RCWL[COREPLL]. COREPLL values not listed in this table should be considered reserved.

**Table 73. e300 Core PLL Configuration**

| RCWL[COREPLL] | | | ***core_clk*:*csb_clk* Ratio** | **VCO divider** |
|---|---|---|---|---|
| **0–1** | **2–5** | **6** | | |
| **nn** | **0000** | n | PLL bypassed (PLL off, *csb_clk* clocks core directly) | PLL bypassed (PLL off, *csb_clk* clocks core directly) |
| **00** | **0001** | 0 | 1:1 | ÷2 |
| **01** | **0001** | 0 | 1:1 | ÷4 |
| **10** | **0001** | 0 | 1:1 | ÷8 |
| **11** | **0001** | 0 | 1:1 | ÷8 |
| **00** | **0001** | 1 | 1.5:1 | ÷2 |
| **01** | **0001** | 1 | 1.5:1 | ÷4 |
| **10** | **0001** | 1 | 1.5:1 | ÷8 |
| **11** | **0001** | 1 | 1.5:1 | ÷8 |
| **00** | **0010** | 0 | 2:1 | ÷2 |
| **01** | **0010** | 0 | 2:1 | ÷4 |
| **10** | **0010** | 0 | 2:1 | ÷8 |
| **11** | **0010** | 0 | 2:1 | ÷8 |
| **00** | **0010** | 1 | 2.5:1 | ÷2 |
| **01** | **0010** | 1 | 2.5:1 | ÷4 |
| **10** | **0010** | 1 | 2.5:1 | ÷8 |
| **11** | **0010** | 1 | 2.5:1 | ÷8 |
| **00** | **0011** | 0 | 3:1 | ÷2 |
| **01** | **0011** | 0 | 3:1 | ÷4 |
| **10** | **0011** | 0 | 3:1 | ÷8 |
| **11** | **0011** | 0 | 3:1 | ÷8 |

### NOTE

Core VCO frequency = Core frequency × VCO divider. The VCO divider (RCWL[COREPLL[0:1]]) must be set properly so that the core VCO frequency is in the range of 800–1800 MHz. Having a core frequency below the CSB frequency is not a possible option because the core frequency must be equal to or greater than the CSB frequency.

The QUICC Engine block VCO frequency is derived from the following equations:

*ce_clk* = (primary clock input × CEPMF) ÷ (1 + CEPDF)

QE VCO Frequency = *ce_clk* × VCO divider × (1 + CEPDF)

## 21.4 Suggested PLL Configurations

To simplify the PLL configurations, the device might be separated into two clock domains. The first domain contains the CSB PLL and the core PLL. The core PLL is connected serially to the CSB PLL, and has the csb_clk as its input clock. The second clock domain has the QUICC Engine block PLL. The clock domains are independent, and each of their PLLs are configured separately. Both of the domains has one common input clock. This table shows suggested PLL configurations for 33 and 66 MHz input clocks and illustrates each of the clock domains separately. Any combination of clock domains setting with same input clock are valid. Refer to Section 21, "Clocking," for the appropriate operating frequencies for your device.

**Table 76. Suggested PLL Configurations**

| Conf No.[1] | SPMF | CORE PLL | CEPMF | CEPDF | Input Clock Freq (MHz) | CSB Freq (MHz) | Core Freq (MHz) | QUICC Engine Freq (MHz) | 400 (MHz) | 533 (MHz) | 667 (MHz) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **33 MHz CLKIN/PCI_SYNC_IN Options** | | | | | | | | | | | |
| **s1** | **0100** | **0000100** | æ | æ | 33 | 133 | 266 | — | ∞ | ∞ | ∞ |
| **s2** | **0100** | **0000101** | æ | æ | 33 | 133 | 333 | — | ∞ | ∞ | ∞ |
| **s3** | **0101** | **0000100** | æ | æ | 33 | 166 | 333 | — | ∞ | ∞ | ∞ |
| **s4** | **0101** | **0000101** | æ | æ | 33 | 166 | 416 | — | — | ∞ | ∞ |
| **s5** | **0110** | **0000100** | æ | æ | 33 | 200 | 400 | — | ∞ | ∞ | ∞ |
| **s6** | **0110** | **0000110** | æ | æ | 33 | 200 | 600 | — | — | — | ∞ |
| **s7** | **0111** | **0000011** | æ | æ | 33 | 233 | 350 | — | ∞ | ∞ | ∞ |
| **s8** | **0111** | **0000100** | æ | æ | 33 | 233 | 466 | — | — | ∞ | ∞ |
| **s9** | **0111** | **0000101** | æ | æ | 33 | 233 | 583 | — | — | — | ∞ |
| **s10** | **1000** | **0000011** | æ | æ | 33 | 266 | 400 | — | ∞ | ∞ | ∞ |
| **s11** | **1000** | **0000100** | æ | æ | 33 | 266 | 533 | — | — | ∞ | ∞ |
| **s12** | **1000** | **0000101** | æ | æ | 33 | 266 | 667 | — | — | — | ∞ |
| **s13** | **1001** | **0000010** | æ | æ | 33 | 300 | 300 | — | ∞ | ∞ | ∞ |
| **s14** | **1001** | **0000011** | æ | æ | 33 | 300 | 450 | — | — | ∞ | ∞ |
| **s15** | **1001** | **0000100** | æ | æ | 33 | 300 | 600 | — | — | — | ∞ |
| **s16** | **1010** | **0000010** | æ | æ | 33 | 333 | 333 | — | ∞ | ∞ | ∞ |
| **s17** | **1010** | **0000011** | æ | æ | 33 | 333 | 500 | — | — | ∞ | ∞ |
| **s18** | **1010** | **0000100** | æ | æ | 33 | 333 | 667 | — | — | — | ∞ |
| **c1** | æ | æ | **01001** | **0** | 33 | — | — | 300 | ∞ | ∞ | ∞ |
| **c2** | æ | æ | **01100** | **0** | 33 | — | — | 400 | ∞ | ∞ | ∞ |
| **c3** | æ | æ | **01110** | **0** | 33 | — | — | 466 | — | ∞ | ∞ |
| **c4** | æ | æ | **01111** | **0** | 33 | — | — | 500 | — | ∞ | ∞ |

This table shows heat sinks and junction-to-ambient thermal resistance for TBGA package.

**Table 78. Heat Sinks and Junction-to-Ambient Thermal Resistance of TBGA Package**

| Heat Sink Assuming Thermal Grease | Airflow | 35 × 35 mm TBGA |
|---|---|---|
| | | Junction-to-Ambient Thermal Resistance |
| AAVID 30 × 30 × 9.4 mm pin fin | Natural convention | 10.7 |
| AAVID 30 × 30 × 9.4 mm pin fin | 1 m/s | 6.2 |
| AAVID 30 × 30 × 9.4 mm pin fin | 2 m/s | 5.3 |
| AAVID 31 × 35 × 23 mm pin fin | Natural convention | 8.1 |
| AAVID 31 × 35 × 23 mm pin fin | 1 m/s | 4.4 |
| AAVID 31 × 35 × 23 mm pin fin | 2 m/s | 3.7 |
| Wakefield, 53 × 53 × 25 mm pin fin | Natural convention | 5.4 |
| Wakefield, 53 × 53 × 25 mm pin fin | 1 m/s | 3.2 |
| Wakefield, 53 × 53 × 25 mm pin fin | 2 m/s | 2.4 |
| MEI, 75 × 85 × 12 no adjacent board, extrusion | Natural convention | 6.4 |
| MEI, 75 × 85 × 12 no adjacent board, extrusion | 1 m/s | 3.8 |
| MEI, 75 × 85 × 12 no adjacent board, extrusion | 2 m/s | 2.5 |
| MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass | 1 m/s | 2.8 |

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #15
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

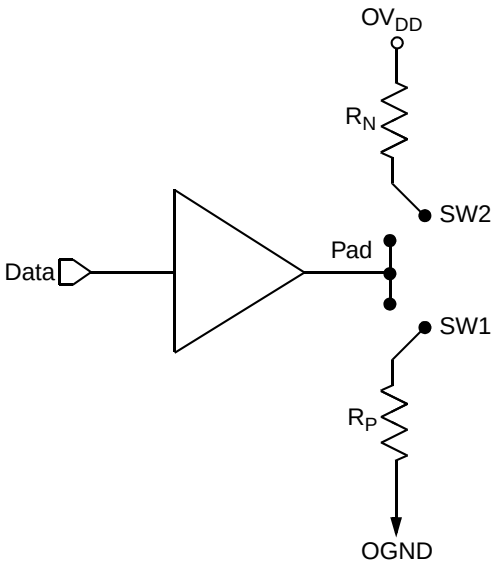


**Figure 57. Driver Impedance Measurement**

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value $R_{term}$. The measured voltage is $V_2 = 1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum $V_{DD}$, nominal $OV_{DD}$, 105° C.

**Table 79. Impedance Characteristics**

| Impedance | Local Bus, Ethernet, DUART, Control, Configuration, Power Management | PCI | DDR DRAM | Symbol | Unit |
|---|---|---|---|---|---|
| $R_N$ | 42 Target | 25 Target | 20 Target | $Z_0$ | W |
| $R_P$ | 42 Target | 25 Target | 20 Target | $Z_0$ | W |
| Differential | NA | NA | NA | $Z_{DIFF}$ | W |

**Note:** Nominal supply voltages. See Table 1, $T_J$ = 105° C.

## 23.6 Configuration Pin Muxing

The device provides the user with power-on configuration options that can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.