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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	-
Number of Cores/Bus Width	-
Speed	-
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8360zualfha

  - Programmable highest priority request
  - Four groups of interrupts with programmable priority
  - External and internal interrupts directed to communication processor
  - Redirects interrupts to external $\overline{\text{INTA}}$ pin when in core disable mode
  - Unique vector number for each interrupt source
- Dual industry-standard I^2C interfaces
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
  - System initialization data is optionally loaded from I^2C-1 EPROM by boot sequencer embedded hardware
- DMA controller
  - Four independent virtual channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - All channels accessible by local core and remote PCI masters
  - Misaligned transfer capability
  - Data chaining and direct mode
  - Interrupt on completed segment and chain
  - DMA external handshake signals: $\overline{\text{DMA\_DREQ}}$[0:3]/$\overline{\text{DMA\_DACK}}$[0:3]/$\overline{\text{DMA\_DONE}}$[0:3]. There is one set for each DMA channel. The pins are multiplexed to the parallel IO pins with other QE functions.
- DUART
  - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- System timers
  - Periodic interrupt timer
  - Real-time clock
  - Software watchdog timer
  - Eight general-purpose timers
- IEEE Std. 1149.1™-compliant, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8360E/58E. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

Physical Layer Device Specification Version 1.2a (9/22/2000). The electrical characteristics for the MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

8.1.1 10/100/1000 Ethernet DC Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), reduced media independent interface (RMII) signals, management data input/output (MDIO) and management data clock (MDC).

The MII and RMII interfaces are defined for 3.3 V, while the RGMII and RTBI interfaces can be operated at 2.5 V. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3.* The RMII interface follows the *RMII Consortium RMII Specification Version 1.2.*

Table 25. RGMII/RTBI, GMII, TBI, MII, and RMII DC Electrical Characteristics (when operating at 3.3 V)

Parameter	Symbol	Conditions		Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD}	—		2.97	3.63	V	1
Output high voltage	V_{OH}	I_{OH} = –4.0 mA	LV_{DD} = Min	2.40	LV_{DD} + 0.3	V	—
Output low voltage	V_{OL}	I_{OL} = 4.0 mA	LV_{DD} = Min	GND	0.50	V	—
Input high voltage	V_{IH}	—	—	2.0	LV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	—	—	–0.3	0.90	V	—
Input current	I_{IN}	0 V ≤V_{IN} ≤LV_{DD}		—	±10	μA	—

Note:
1. GMII/MII pins that are not needed for RGMII, RMII, or RTBI operation are powered by the OV_{DD} supply.

Table 26. RGMII/RTBI DC Electrical Characteristics (when operating at 2.5 V)

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.00	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	LV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	–0.3	0.70	V
Input current	I_{IN}	0 V ≤V_{IN} ≤LV_{DD}		—	±10	μA

8.2 GMII, MII, RMII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII Timing Specifications

This sections describe the GMII transmit and receive AC timing specifications.

8.2.1.2 GMII Receive AC Timing Specifications

This table provides the GMII receive AC timing specifications.

Table 28. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
RX_CLK clock period	t_{GRX}	—	8.0	—	ns	—
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	%	—
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns	—
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.2	—	—	ns	2
RX_CLK clock rise time, (20% to 80%)	t_{GRXR}	—	—	1.0	ns	—
RX_CLK clock fall time, (80% to 20%)	t_{GRXF}	—	—	1.0	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In rev. 2.0 silicon, due to errata, t_{GRDXKH} minimum is 0.5 which is not compliant with the standard. Refer to Errata *QE_ENET18* in *Chip Errata for the MPC8360E, Rev. 1*.

This figure shows the GMII receive AC timing diagram.

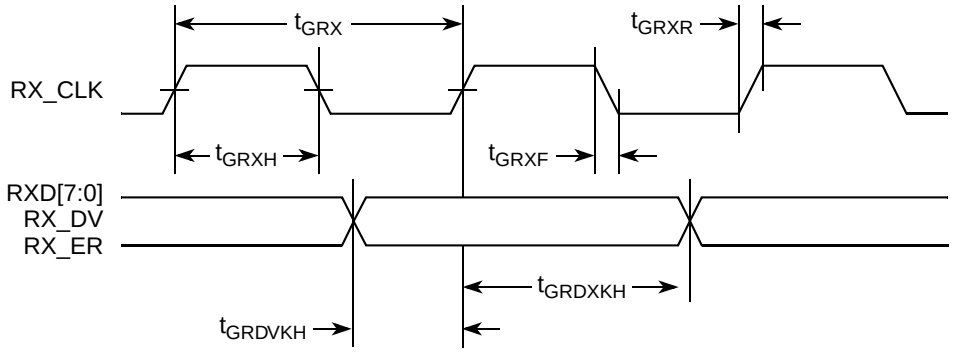


Figure 11. GMII Receive AC Timing Diagram

Table 32. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise time	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load.

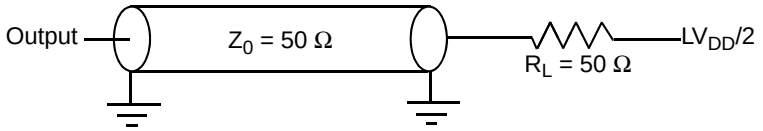


Figure 16. AC Test Load

This figure shows the RMII receive AC timing diagram.

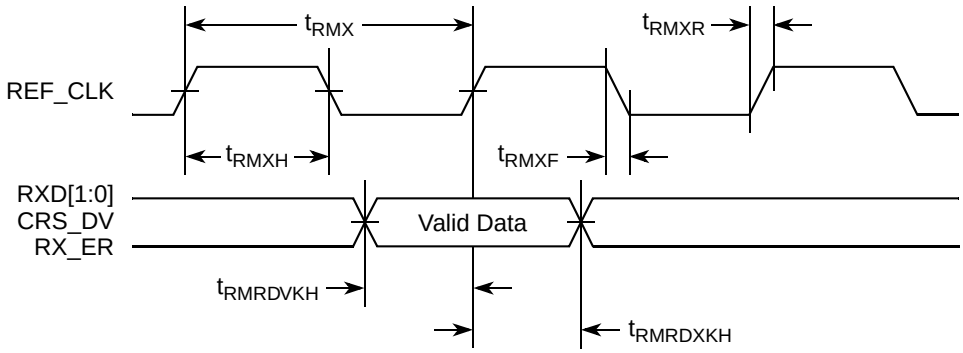


Figure 17. RMII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.2 TBI Receive AC Timing Specifications

This table provides the TBI receive AC timing specifications.

Table 34. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
PMA_RX_CLK clock period	t_{TRX}	—	16.0	—	ns	—
PMA_RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns	—
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%	—
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns	2
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.0	—	—	ns	2
RX_CLK clock rise time, V_{IL}(min) to V_{IH}(max)	t_{TRXR}	0.7	—	2.4	ns	—
RX_CLK clock fall time, V_{IH}(max) to V_{IL}(min)	t_{TRXF}	0.7	—	2.4	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Setup and hold time of even numbered RCG are measured from riding edge of PMA_RX_CLK1. Setup and hold time of odd numbered RCG are measured from riding edge of PMA_RX_CLK0.

This figure shows the TBI receive AC timing diagram.

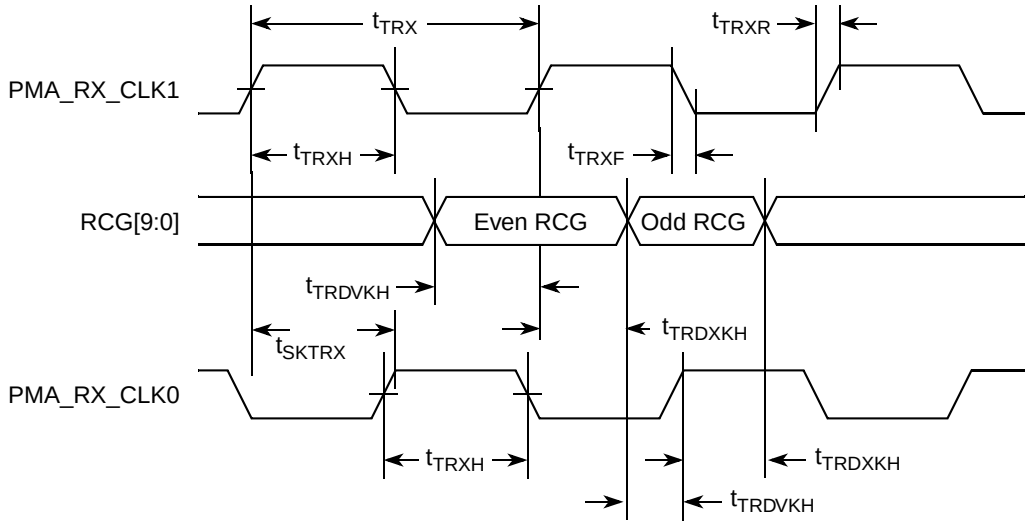


Figure 19. TBI Receive AC Timing Diagram

8.2.5 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 35. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	$t_{SKRGTKHDX}$ $t_{SKRGTKHDV}$	–0.5 —	—	— 0.5	ns	7
Data to clock input skew (at receiver)	$t_{SKRGDXKH}$ $t_{SKRGDVKH}$	1.0 —	—	— 2.6	ns	2
Clock cycle duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	t_{RGTH}/t_{RGT}	45	50	55	%	4, 5
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 5
Rise time (20–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20–80%)	t_{RGTF}	—	—	0.75	ns	—
GTX_CLK125 reference clock period	t_{G125}	—	8.0	—	ns	6
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%	—

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (Rx) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns can be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Duty cycle reference is $LV_{DD}/2$.
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention.
7. In rev. 2.0 silicon, due to errata, $t_{SKRGTKHDX}$ minimum is –2.3 ns and $t_{SKRGTKHDV}$ maximum is 1 ns for UCC1, 1.2 ns for UCC2 option 1, and 1.8 ns for UCC2 option 2. In rev. 2.1 silicon, due to errata, $t_{SKRGTKHDX}$ minimum is –0.65 ns for UCC2 option 1 and –0.9 for UCC2 option 2, and $t_{SKRGTKHDV}$ maximum is 0.75 ns for UCC1 and UCC2 option 1 and 0.85 for UCC2 option 2. Refer to Errata QE_ENET10 in *Chip Errata for the MPC8360E, Rev. 1*. UCC1 does meet $t_{SKRGTKHDX}$ minimum for rev. 2.1 silicon.

Table 41. Local Bus General Timing Parameters—DLL Bypass Mode[9] (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus clock to output valid	t_{LBKHOV}	—	3	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4	ns	8

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $OV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on LALE output pin is at least 10 pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
9. DLL bypass mode is not recommended for use at frequencies above 66 MHz.

This figure provides the AC test load for the local bus.

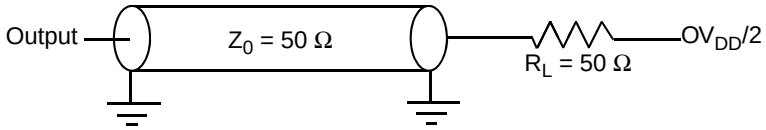


Figure 22. Local Bus C Test Load

This figure provides the AC test load for the I^2C.

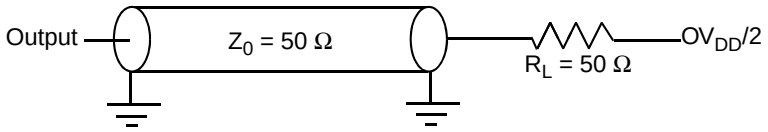


Figure 34. I^2C AC Test Load

This figure shows the AC timing diagram for the I^2C bus.

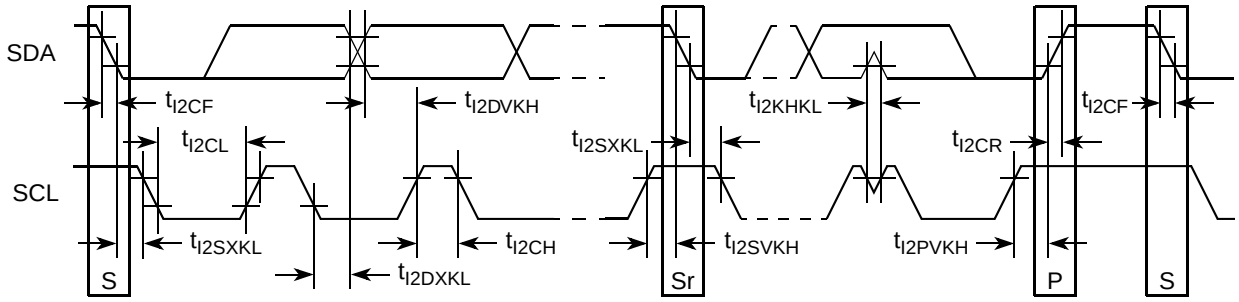


Figure 35. I^2C Bus AC Timing Diagram

12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8360E/58E.

12.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface of the device.

Table 46. PCI DC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	$0.5 \times OV_{DD}$	$OV_{DD} + 0.5$	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	-0.5	$0.3 \times OV_{DD}$	V
High-level output voltage	V_{OH}	I_{OH} = –500 µA	$0.9 \times OV_{DD}$	—	V
Low-level output voltage	V_{OL}	I_{OL} = 1500 µA	—	$0.1 \times OV_{DD}$	V
Input current	I_{IN}	$0 V \leq V_{IN}$[1] $\leq OV_{DD}$	—	±10	µA

12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the device. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. This table provides the PCI AC timing specifications at 66 MHz.

Table 47. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2, 5
Output hold from clock	t_{PCKHOX}	1	—	ns	2

13.2 Timers AC Timing Specifications

This table provides the timer input and output AC timing specifications.

Table 50. Timers Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Typ	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

This figure provides the AC test load for the timers.

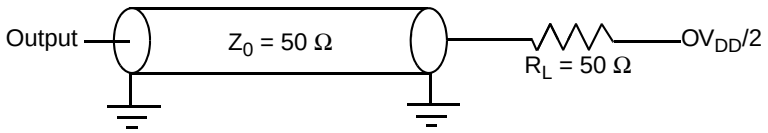


Figure 39. Timers AC Test Load

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8360E/58E.

14.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the device GPIO.

Table 51. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	0 V ≤V_{IN} ≤OV_{DD}	—	±10	μA	—

Note:
1. This specification applies when operating from 3.3-V supply.

14.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 52. GPIO Input AC Timing Specifications[1]

Characteristic	Symbol[2]	Typ	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

This figure provides the AC test load for the GPIO.

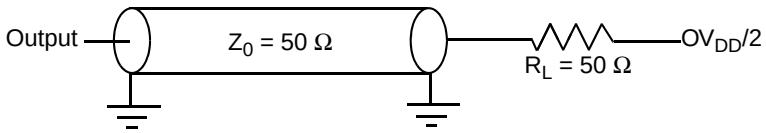


Figure 40. GPIO AC Test Load

15 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8360E/58E.

15.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins of the IPIC.

Table 53. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±10	μA
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, $\overline{\text{MCP\_OUT}}$, and CE ports Interrupts.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

Table 56. SPI AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

This figure provides the AC test load for the SPI.

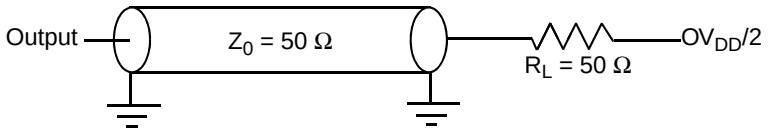
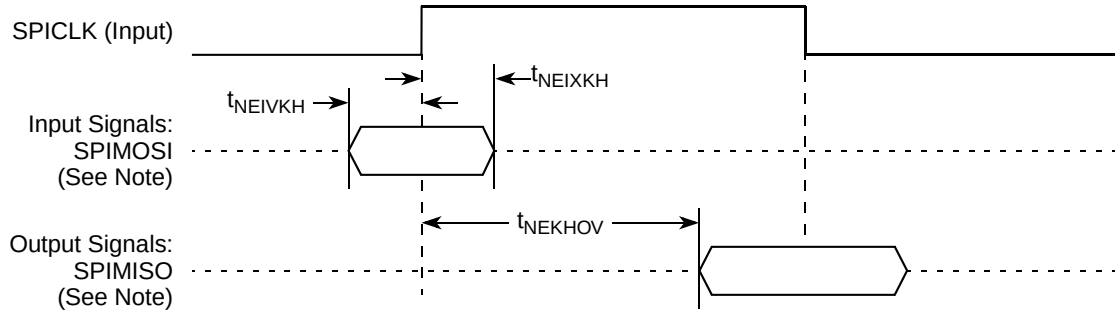


Figure 41. SPI AC Test Load

These figures represent the AC timing from Table 56. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

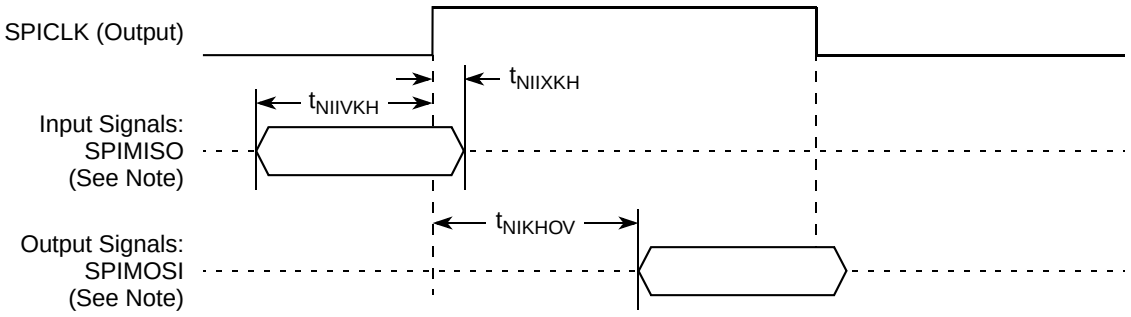
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 42. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in Master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 43. SPI AC Timing in Master Mode (Internal Clock) Diagram

Table 62. HDLC, BISYNC, and Transparent AC Timing Specifications[1] (continued)

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock high impedance	t_{HIKHOX}	-0.5	5.5	ns
Outputs—External clock high impedance	t_{HEKHOX}	1	8	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	8.5	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns
Inputs—Internal clock input hold time	t_{HIIXKH}	1.4	—	ns
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Table 63. Synchronous UART AC Timing Specifications[1]

Characteristic	Symbol[2]	Min	Max	Unit
Outputs—Internal clock delay	$t_{UAIKHOV}$	0	11.3	ns
Outputs—External clock delay	$t_{UAEKHOV}$	1	14	ns
Outputs—Internal clock high impedance	$t_{UAIKHOX}$	0	11	ns
Outputs—External clock high impedance	$t_{UAEKHOX}$	1	14	ns
Inputs—Internal clock input setup time	$t_{UAIIVKH}$	6	—	ns
Inputs—External clock input setup time	$t_{UAEIVKH}$	8	—	ns
Inputs—Internal clock input hold time	$t_{UAIIXKH}$	1	—	ns
Inputs—External clock input hold time	$t_{UAEIXKH}$	1	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

This figure provides the AC test load.

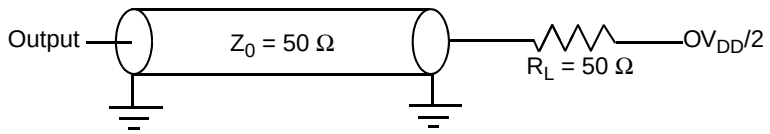
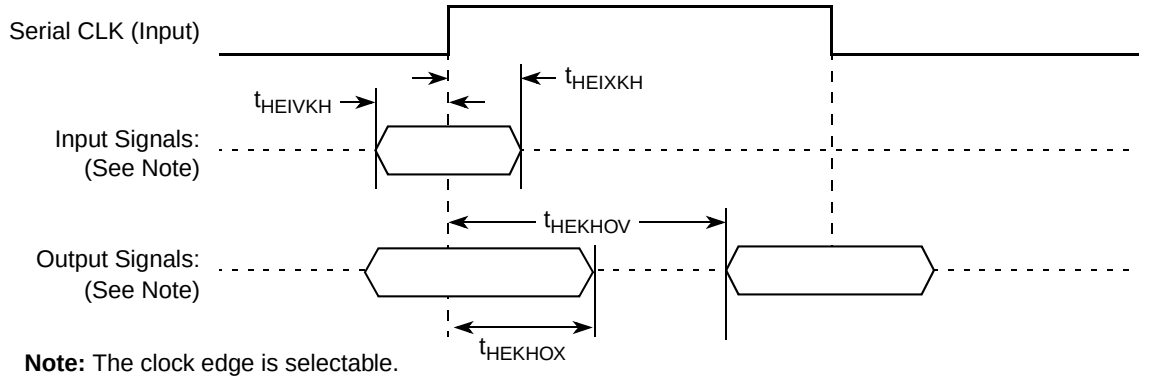


Figure 49. AC Test Load

18.3 AC Test Load

These figures represent the AC timing from Table 62 and Table 63. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

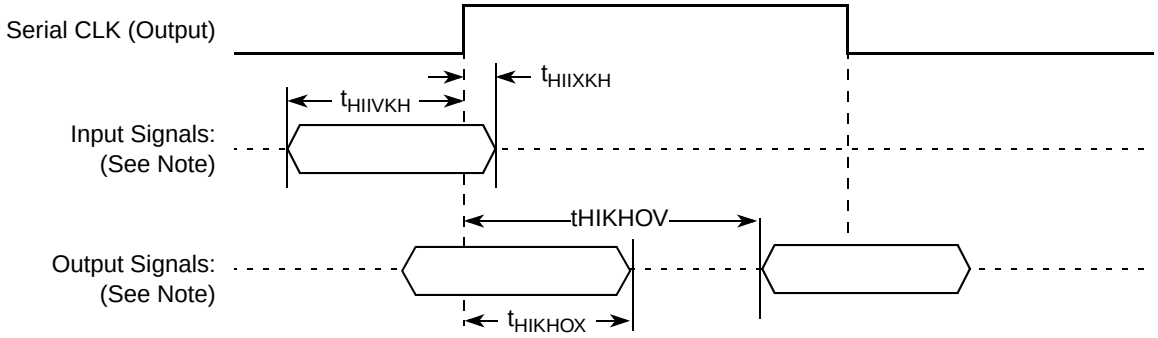
This figure shows the timing with external clock.



Note: The clock edge is selectable.

Figure 50. AC Timing (External Clock) Diagram

This figure shows the timing with internal clock.



Note: The clock edge is selectable.

Figure 51. AC Timing (Internal Clock) Diagram

Table 66. MPC8360E TBGA Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$LV_{DD}0$	D5, D6	Power for UCC1 Ethernet interface (2.5 V, 3.3 V)	$LV_{DD}0$	—
$LV_{DD}1$	C17, D16	Power for UCC2 Ethernet interface option 1 (2.5 V, 3.3 V)	$LV_{DD}1$	9
$LV_{DD}2$	B18, E21	Power for UCC2 Ethernet interface option 2 (2.5 V, 3.3 V)	$LV_{DD}2$	9
V_{DD}	C36, D29, D35, E16, F9, F12, F15, F17, F18, F20, F21, F23, F25, F26, F29, F31, F32, F33, G6, J6, K32, M32, N6, P33, R6, R32, U32, V6, Y5, Y32, AB6, AB33, AD6, AF32, AK6, AL6, AM7, AM9, AM10, AM11, AM12, AM13, AM14, AM15, AM18, AM21, AM25, AM28, AM32, AN15, AN21, AN26, AU9, AU17	Power for core (1.2 V)	V_{DD}	—
OV_{DD}	A10, B9, B15, B32, C1, C12, C22, C29, D24, E3, E10, E27, G4, H35, J1, J35, K2, M4, N3, N34, R2, R37, T36, U2, U33, V4, V34, W3, Y35, Y37, AA1, AA36, AB2, AB34	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV_{DD}	—
MVREF1	AN20	I	DDR reference voltage	—
MVREF2	AU32	I	DDR reference voltage	—
SPARE1	B11	I/O	OV_{DD}	8
SPARE3	AH32	—	GV_{DD}	8
SPARE4	AU18	—	GV_{DD}	7
SPARE5	AP1	—	GV_{DD}	8

21 Clocking

This figure shows the internal distribution of clocks within the MPC8360E.

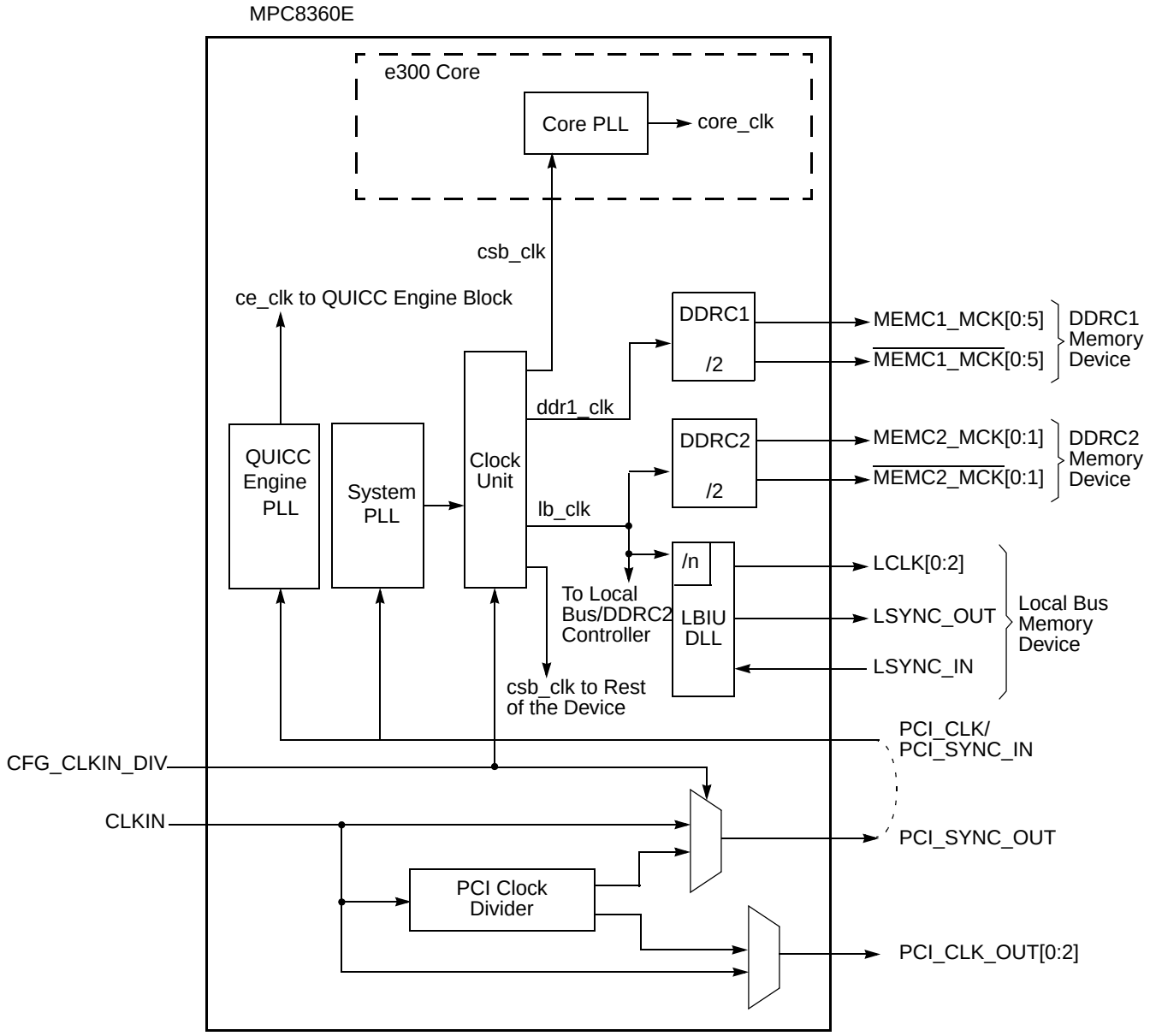


Figure 54. MPC8360E Clock Subsystem

Table 70. System PLL Multiplication Factors (continued)

RCWL[SPMF]	System PLL Multiplication Factor
1100	× 12
1101	× 13
1110	× 14
1111	× 15

The RCWL[SVCOD] denotes the system PLL VCO internal frequency as shown in this table.

Table 71. System PLL VCO Divider

RCWL[SVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider must be set properly so that the system VCO frequency is in the range of 600–1400 MHz.

The system VCO frequency is derived from the following equations:

- *csb_clk* = {PCI_SYNC_IN × (1 + CFG_CLKIN_DIV)} × SPMF
- System VCO Frequency = *csb_clk* × VCO divider (if both RCWL[DDRCM] and RCWL[LBCM] are cleared) OR
- System VCO frequency = 2 × *csb_clk* × VCO divider (if either RCWL[DDRCM] or RCWL[LBCM] are set).

As described in Section 21, "Clocking," the LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). This table shows the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

Table 72. CSB Frequency Options

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk*: Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2:1				133
Low	0011	3:1			100	200
Low	0100	4:1		100	133	266
Low	0101	5:1		125	166	333

21.3 QUICC Engine Block PLL Configuration

The QUICC Engine block PLL is controlled by the RCWL[CEPMF], RCWL[CEPDF], and RCWL[CEVCOD] parameters. This table shows the multiplication factor encodings for the QUICC Engine block PLL.

Table 74. QUICC Engine Block PLL Multiplication Factors

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF])
00000	0	× 16
00001	0	Reserved
00010	0	× 2
00011	0	× 3
00100	0	× 4
00101	0	× 5
00110	0	× 6
00111	0	× 7
01000	0	× 8
01001	0	× 9
01010	0	× 10
01011	0	× 11
01100	0	× 12
01101	0	× 13
01110	0	× 14
01111	0	× 15
10000	0	× 16
10001	0	× 17
10010	0	× 18
10011	0	× 19
10100	0	× 20
10101	0	× 21
10110	0	× 22
10111	0	× 23
11000	0	× 24
11001	0	× 25
11010	0	× 26
11011	0	× 27
11100	0	× 28

Table 74. QUICC Engine Block PLL Multiplication Factors (continued)

RCWL[CEPMF]	RCWL[CEPDF]	QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF])
11101	0	× 29
11110	0	× 30
11111	0	× 31
00011	1	× 1.5
00101	1	× 2.5
00111	1	× 3.5
01001	1	× 4.5
01011	1	× 5.5
01101	1	× 6.5
01111	1	× 7.5
10001	1	× 8.5
10011	1	× 9.5
10101	1	× 10.5
10111	1	× 11.5
11001	1	× 12.5
11011	1	× 13.5
11101	1	× 14.5

Note:
1. Reserved modes are not listed.

The RCWL[CEVCOD] denotes the QUICC Engine Block PLL VCO internal frequency as shown in this table.

Table 75. QUICC Engine Block PLL VCO Divider

RCWL[CEVCOD]	VCO Divider
00	4
01	8
10	2
11	Reserved

NOTE

The VCO divider (RCWL[CEVCOD]) must be set properly so that the QUICC Engine block VCO frequency is in the range of 600–1400 MHz. The QUICC Engine block frequency is not restricted by the CSB and core frequencies. The CSB, core, and QUICC Engine block frequencies should be selected according to the performance requirements.

Example 1. Sample Table Use

Index	SPMF	CORE PLL	CEPMF	CEPDF	Input Clock (MHz)	CSB Freq (MHz)	Core Freq (MHz)	QUICC Engine Freq (MHz)	400 (MHz)	533 (MHz)	667 (MHz)
A	**1000**	**0000011**	**01001**	**0**	33	266	400	300	∞	∞	∞
B	**0100**	**0000100**	**00110**	**0**	66	266	533	400	∞	∞	∞

- **Example A.** To configure the device with CSB clock rate of 266 MHz, core rate of 400 MHz, and QUICC Engine clock rate 300 MHz while the input clock rate is 33 MHz. Conf No. ‘s10’ and ‘c1’ are selected from Table 76. SPMF is 1000, CORPLL is 0000011, CEPMF is 01001, and CEPDF is 0.
- **Example B.** To configure the device with CSBCSB clock rate of 266 MHz, core rate of 533 MHz and QUICC Engine clock rate 400 MHz while the input clock rate is 66 MHz. Conf No. ‘s5h’ and ‘c2h’ are selected from Table 76. SPMF is 0100, CORPLL is 0000100, CEPMF is 00110, and CEPDF is 0.

22 Thermal

This section describes the thermal specifications of the MPC8360E/58E.

22.1 Thermal Characteristics

This table provides the package thermal characteristics for the 37.5 mm × 37.5 mm 740-TBGA package.

Table 77. Package Thermal Characteristics for the TBGA Package

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection on single-layer board (1s)	$R_{\theta JA}$	15	°C/W	1, 2
Junction-to-ambient natural convection on four-layer board (2s2p)	$R_{\theta JA}$	11	°C/W	1, 3
Junction-to-ambient (@1 m/s) on single-layer board (1s)	$R_{\theta JMA}$	10	°C/W	1, 3
Junction-to-ambient (@ 1 m/s) on four-layer board (2s2p)	$R_{\theta JMA}$	8	°C/W	1, 3
Junction-to-ambient (@ 2 m/s) on single-layer board (1s)	$R_{\theta JMA}$	9	°C/W	1, 3
Junction-to-ambient (@ 2 m/s) on four-layer board (2s2p)	$R_{\theta JMA}$	7	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	4.5	°C/W	4
Junction-to-case thermal	$R_{\theta JC}$	1.1	°C/W	5

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