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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302rdt6

Contents

2 Description

The STM32F302xD/E family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core with FPU operating at a frequency of 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an embedded trace macrocell (ETM). The family incorporates high-speed embedded memories (512-Kbyte Flash memory, 64-Kbyte SRAM), a flexible memory controller (FSMC) for static memories (SRAM, PSRAM, NOR and NAND), and an extensive range of enhanced I/Os and peripherals connected to an AHB and two APB buses.

The devices offer two fast 12-bit ADCs (5 Msps), four comparators, two operational amplifiers, one DAC channel, a low-power RTC, up to two general-purpose 16-bit timers, one general-purpose 32-bit timer, and one timer dedicated to motor control. They also feature standard and advanced communication interfaces: up to three I^2Cs, up to four SPIs (two SPIs are with multiplexed full-duplex I^2Ss), three USARTs, up to two UARTs, CAN and USB. To achieve audio class accuracy, the I^2S peripherals can be clocked via an external PLL.

The STM32F302xD/E family operates in the -40 to +85°C and -40 to +105°C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F302xD/E family offers devices in different packages ranging from 64 to 144 pins.

Depending on the device chosen, different sets of peripherals are included.

3.4 Embedded SRAM

STM32F302xD/E devices feature 64 Kbyte of embedded SRAM with hardware parity check implemented on the first 32 Kbyte. The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.5 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PA2/PA3) or USB (PA11/PA12) through DFU (device firmware upgrade).

3.6 Cyclic redundancy check (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

4 Pinout and pin description

Figure 4. STM32F302xD/E LQFP64 pinout

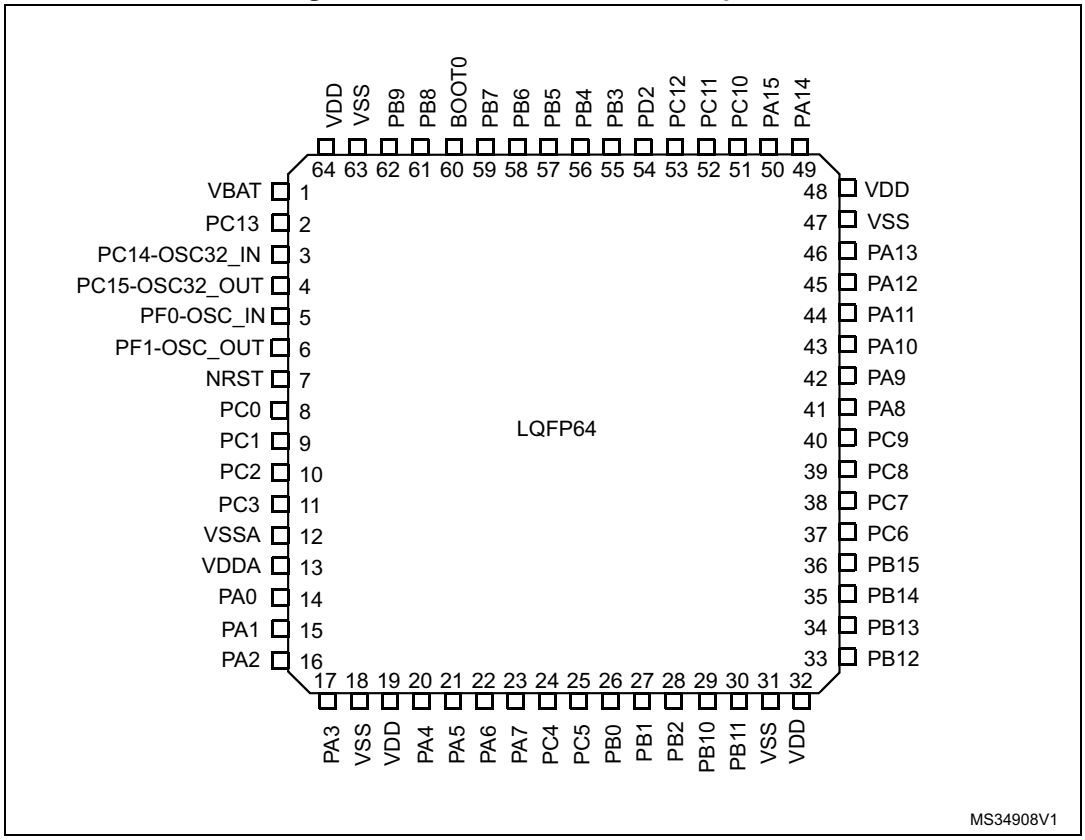


Figure 5. STM32F302xD/E LQFP100 pinout

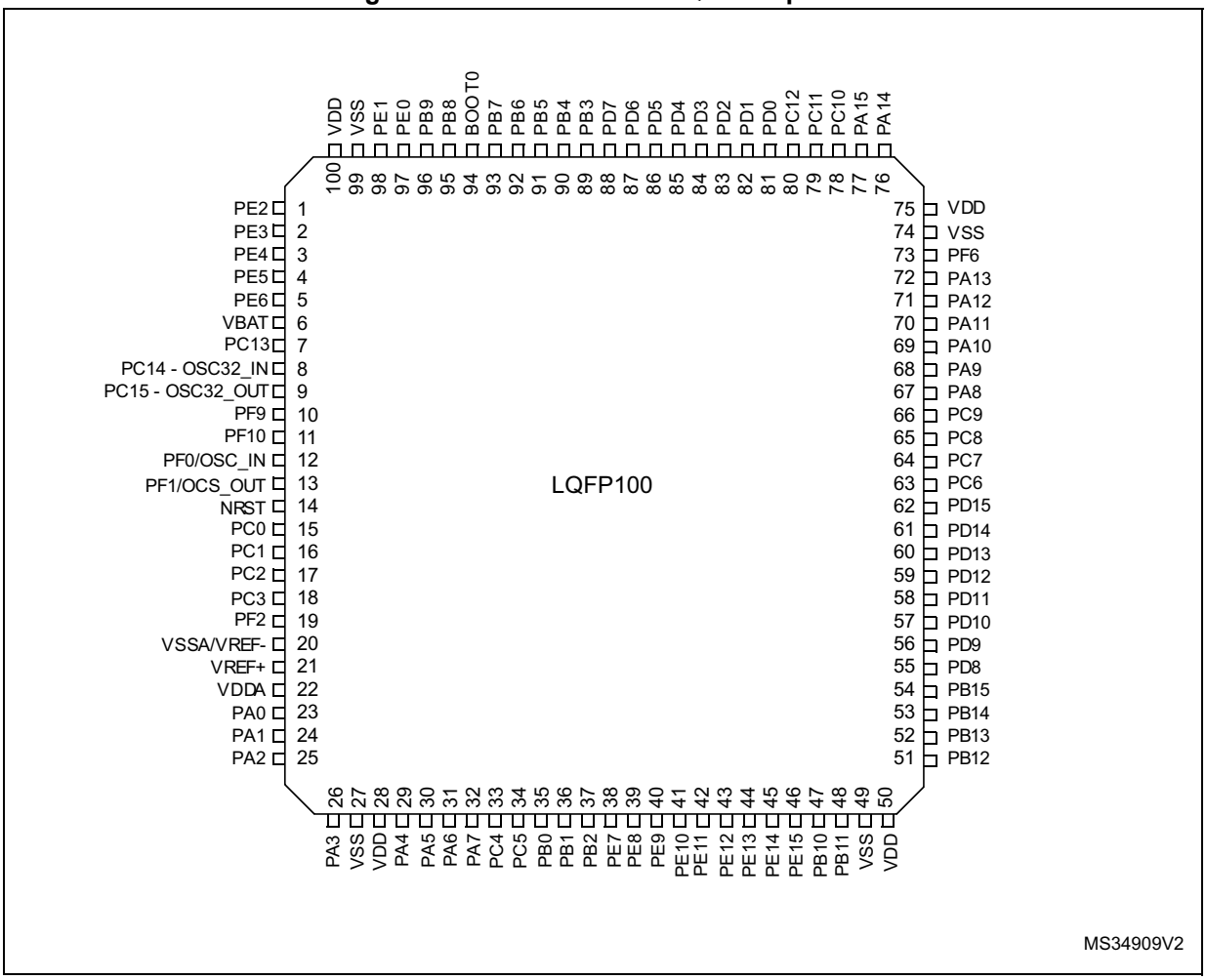


Figure 6. STM32F302xD/E LQFP144 pinout

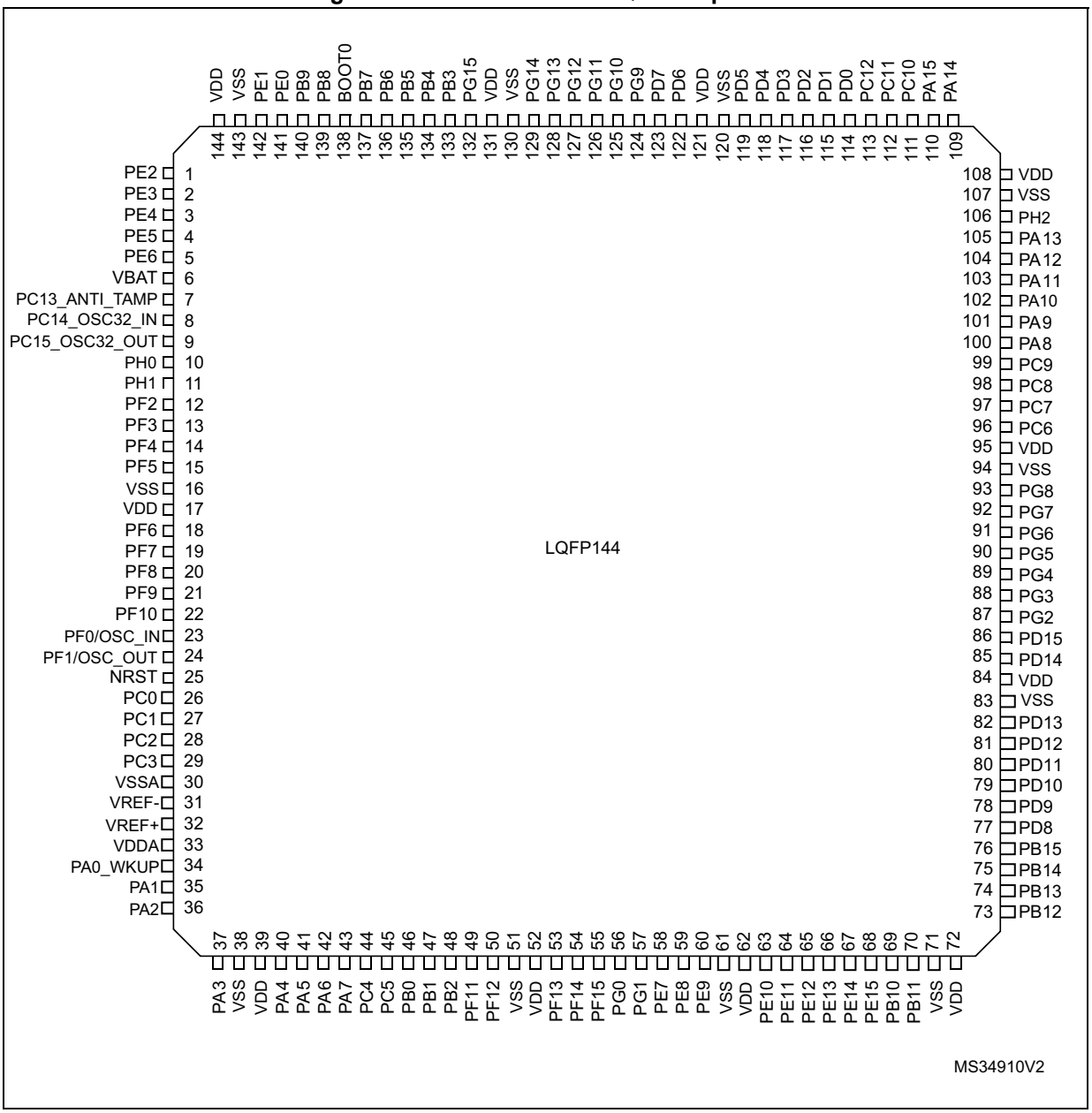


Table 13. STM32F302xD/E pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP100	LQFP144						
9	16	G9	27	PC1	I/O	TTa	-	EVENTOUT, TIM1_CH2	ADC12_IN7
10	17	G8	28	PC2	I/O	TTa	-	EVENTOUT, TIM1_CH3	ADC12_IN8
11	18	H10	29	PC3	I/O	TTa	-	EVENTOUT, TIM1_CH4, TIM1_BKIN2	ADC12_IN9
12	20	H8	30	VSSA	S	-	(1)	-	-
-	-	-	31	VREF-	S	-	(1)	-	-
-	21	J8	32	VREF+(4)	S	-	-	-	-
13	22	J10	33	VDDA	S	-	-	-	-
14	23	H9	34	PA0	I/O	TTa	-	TIM2_CH1/TIM2_ETR, TSC_G1_IO1, USART2_CTS, COMP1_OUT, EVENTOUT	ADC1_IN1(3), COMP1_INM, RTC_TAMP2, WKUP1
15	24	J9	35	PA1	I/O	TTa	-	RTC_REFIN, TIM2_CH2, TSC_G1_IO2, USART2_RTS, TIM15_CH1N, EVENTOUT	ADC1_IN2(3), COMP1_INP, OPAMP1_VINP
16	25	F7	36	PA2	I/O	TTa	(5)	TIM2_CH3, TSC_G1_IO3, USART2_TX, COMP2_OUT, TIM15_CH1, EVENTOUT	ADC1_IN3(3), COMP2_INM, OPAMP1_VOUT
17	26	G7	37	PA3	I/O	TTa	-	TIM2_CH4, TSC_G1_IO4, USART2_RX, TIM15_CH2, EVENTOUT	ADC1_IN4(3), OPAMP1_VINM/ OPAMP1_VINP
18	27	K9, K10	38	VSS	S	-	-	-	-
19	28	K8	39	VDD	S	-	(1)	-	-
20	29	J7	40	PA4	I/O	TTa	(5)	TIM3_CH2, TSC_G2_IO1, SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_CK, EVENTOUT	ADC2_IN1(3), DAC1_OUT1, COMP1_INM, COMP2_INM, COMP4_INM, COMP6_INM,

Table 13. STM32F302xD/E pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP100	LQFP144						
-	-	-	90	PG5	I/O	FT	(1)	EVENTOUT, FMC_A15	-
-	-	-	91	PG6	I/O	FT	(1)	EVENTOUT, FMC_INT2	-
-	-	-	92	PG7	I/O	FT	(1)	EVENTOUT, FMC_INT3	-
-	-	-	93	PG8	I/O	FT	(1)	EVENTOUT	-
-	-	-	94	VSS	S	-	(1)	-	-
-	-	-	95	VDD	S	-	(1)	-	-
37	63	F4	96	PC6	I/O	FT	-	EVENTOUT, TIM3_CH1, I2S2_MCK, COMP6_OUT	-
38	64	F2	97	PC7	I/O	FT	-	EVENTOUT, TIM3_CH2, I2S3_MCK	-
39	65	F1	98	PC8	I/O	FT	-	EVENTOUT, TIM3_CH3	-
40	66	F3	99	PC9	I/O	FTf	-	EVENTOUT, TIM3_CH4, I2C3_SDA, I2SCKIN	-
41	67	F5	100	PA8	I/O	FTf	-	MCO, I2C3_SCL, I2C2_SMBAL, I2S2_MCK, TIM1_CH1, USART1_CK, TIM4_ETR, EVENTOUT	-
42	68	E5	101	PA9	I/O	FTf	-	I2C3_SMBAL, TSC_G4_IO1, I2C2_SCL, I2S3_MCK, TIM1_CH2, USART1_TX, TIM15_BKIN, TIM2_CH3, EVENTOUT	-
43	69	E1	102	PA10	I/O	FTf	-	TIM17_BKIN, TSC_G4_IO2, I2C2_SDA, SPI2_MISO/I2S2ext_SD, TIM1_CH3, USART1_RX, COMP6_OUT, TIM2_CH4, EVENTOUT	-
44	70	E2	103	PA11	I/O	FT	-	SPI2_MOSI/I2S2_SD, TIM1_CH1N, USART1_CTS, COMP1_OUT, CAN_RX, TIM4_CH1, TIM1_CH4, TIM1_BKIN2, EVENTOUT	USB_DM

Table 13. STM32F302xD/E pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP100	LQFP144						
-	98	A8	142	PE1	I/O	FT	(1)	EVENTOUT, TIM17_CH1, USART1_RX, FMC_NBL1	-
63	99	C7	143	VSS	S	-	-	-	-
64	100	A9, A10, B10, B8	144	VDD	S	-	-	-	-

1. Function availability depends on the chosen device.
2. PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED)
   After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the RM0316 reference manual.
3. Fast ADC channel.
4. The VREF+ functionality is not available on the 64-pin package. In this package, the VREF+ is internally connected to VDDA.
5. These GPIOs offer a reduced touch sensing sensitivity. It is thus recommended to use them as sampling capacitor I/O.

Table 14. STM32F302xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3//15/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port A	PA10	-	TIM17_BKIN	-	TSC_G4_IO2	I2C2_SDA	SPI2_MISO/I2S2ext_SD	TIM1_CH3	USART1_RX	COMP6_OUT	-	TIM2_CH4	-	-	-	-	EVENTOUT
	PA11	-	-	-	-	-	SPI2_MOSI/I2S2_SD	TIM1_CH1N	USART1_CTS	COMP1_OUT	CAN_RX	TIM4_CH1	TIM1_CH4	TIM1_BKIN2	-	-	EVENTOUT
	PA12	-	TIM16_CH1	-	-	-	I2SCKIN	TIM1_CH2N	USART1_RTS	COMP2_OUT	CAN_TX	TIM4_CH2	TIM1_ETR	-	-	-	EVENTOUT
	PA13	SWDIO-JTMS	TIM16_CH1N	-	TSC_G4_IO3	-	IR-OUT	-	USART3_CTS	-	-	TIM4_CH3	-	-	-	-	EVENTOUT
	PA14	SWCLK-JTCK	-	-	TSC_G4_IO4	I2C1_SDA	-	TIM1_BKIN	USART2_TX	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	TIM2_CH1/TIM2_ETR	-	TSC_SYNC	I2C1_SCL	SPI1_NSS	SPI3_NSS/I2S3_WS	USART2_RX	-	TIM1_BKIN	-	-	-	-	-	EVENTOUT
Port B	PB0	-	-	TIM3_CH3	TSC_G3_IO2	-	-	TIM1_CH2N	-	-	-	-	-	-	-	-	EVENTOUT
	PB1	-	-	TIM3_CH4	TSC_G3_IO3	-	-	TIM1_CH3N	-	COMP4_OUT	-	-	-	-	-	-	EVENTOUT
	PB2	-	-	-	TSC_G3_IO4	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB3	JTDO-TRACESWO	TIM2_CH2	TIM4_ETR	TSC_G5_IO1	-	SPI1_SCK	SPI3_SCK/I2S3_CK	USART2_TX	-	-	TIM3_ETR	-	-	-	-	EVENTOUT

Table 14. STM32F302xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3//15/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port B	PB4	JTRST	TIM16_CH1	TIM3_CH1	TSC_G5_IO2	-	SPI1_MISO	SPI3_MISO/I2S3ext_SD	USART2_RX	-	-	TIM17_BKIN	-	-	-	-	EVENT OUT
	PB5	-	TIM16_BKIN	TIM3_CH2	-	I2C1_SMBAI	SPI1_MOSI	SPI3_MOSI/I2S3_SD	USART2_CK	I2C3_SDA	-	TIM17_CH1	-	-	-	-	EVENT OUT
	PB6	-	TIM16_CH1N	TIM4_CH1	TSC_G5_IO3	I2C1_SCL	-	-	USART1_TX	-	-	-	-	-	-	-	EVENT OUT
	PB7	-	TIM17_CH1N	TIM4_CH2	TSC_G5_IO4	I2C1_SDA	-	-	USART1_RX	-	-	TIM3_CH4	-	FMC_NADV	-	-	EVENT OUT
	PB8	-	TIM16_CH1	TIM4_CH3	TSC_SYNC	I2C1_SCL	-	-	USART3_RX	COMP1_OUT	CAN_RX	-	-	TIM1_BKIN	-	-	EVENT OUT
	PB9	-	TIM17_CH1	TIM4_CH4	-	I2C1_SDA	-	IR-OUT	USART3_TX	COMP2_OUT	CAN_TX	-	-	-	-	-	EVENT OUT
	PB10	-	TIM2_CH3	-	TSC_SYNC	-	-	-	USART3_TX	-	-	-	-	-	-	-	EVENT OUT
	PB11	-	TIM2_CH4	-	TSC_G6_IO1	-	-	-	USART3_RX	-	-	-	-	-	-	-	EVENT OUT
	PB12	-	-	-	TSC_G6_IO2	I2C2_SMBAL	SPI2_NSS/I2S2_WS	TIM1_BKIN	USART3_CK	-	-	-	-	-	-	-	EVENT OUT
	PB13	-	-	-	TSC_G6_IO3	-	SPI2_SCK/I2S2_CK	TIM1_CH1N	USART3_CTS	-	-	-	-	-	-	-	EVENT OUT

Table 14. STM32F302xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3//15/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port B	PB14	-	TIM15_CH1	-	TSC_G6_IO4	-	SPI2_MISO/I2S2ext_SD	TIM1_CH2N	USART3_RTS	-	-	-	-	-	-	-	EVENT OUT
	PB15	RTC_REFIN	TIM15_CH2	TIM15_CH1N	-	TIM1_CH3N	SPI2_MOSI/I2S2_SD	-	-	-	-	-	-	-	-	-	EVENT OUT
Port C	PC0	-	EVENT OUT	TIM1_CH1	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC1	-	EVENT OUT	TIM1_CH2	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC2	-	EVENT OUT	TIM1_CH3	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC3	-	EVENT OUT	TIM1_CH4	-	-	-	TIM1_BKIN2	-	-	-	-	-	-	-	-	-
	PC4	-	EVENT OUT	TIM1_ETR	-	-	-	-	USART1_TX	-	-	-	-	-	-	-	-
	PC5	-	EVENT OUT	TIM15_BKIN	TSC_G3_IO1	-	-	-	USART1_RX	-	-	-	-	-	-	-	-
	PC6	-	EVENT OUT	TIM3_CH1	-	-	-	I2S2_MCK	COMP6_OUT	-	-	-	-	-	-	-	-
	PC7	-	EVENT OUT	TIM3_CH2	-	-	-	I2S3_MCK	-	-	-	-	-	-	-	-	-
	PC8	-	EVENT OUT	TIM3_CH3	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC9	-	EVENT OUT	TIM3_CH4	I2C3_SDA	-	I2SCKIN	-	-	-	-	-	-	-	-	-	-

Table 26. Typical and maximum current consumption from the V_{DDA} supply (continued)

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run mode, code executing from Flash or RAM	HSE bypass	1 MHz	1.9	3.1	3.6	4.4	2.5	3.7	4.4	5.5	µA
		HSI clock	64 MHz	266	290	301	306	295	320	335	341	
			48 MHz	216	237	247	251	240	262	274	279	
			32 MHz	170	188	196	199	190	208	217	221	
			24 MHz	148	164	170	172	166	182	189	192	
			8 MHz	70	78	81	82	84	92	95	97	

1. Current consumption from the V_{DDA} supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production.

Table 27. Typical and maximum V_{DD} consumption in Stop and Standby modes

Symbol	Parameter	Conditions	Typ @V_{DD} (V_{DD}=V_{DDA})						Max			Unit
			2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	18.4	18.7	18.8	18.9	19.0	19.1	47	435	940	µA
		Regulator in low-power mode, all oscillators OFF	6.80	6.94	7.11	7.18	7.26	7.39	33	408	898	
	Supply current in Standby mode	LSI ON and IWDG ON	0.72	0.87	0.99	1.10	1.23	1.37	-	-	-	
		LSI OFF and IWDG OFF	0.57	0.68	0.76	0.85	0.94	1.03	6.2	8.6	13.5	

Table 37. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	

1. Guaranteed by design, not tested in production.

Figure 16. Low-speed external clock source AC timing diagram

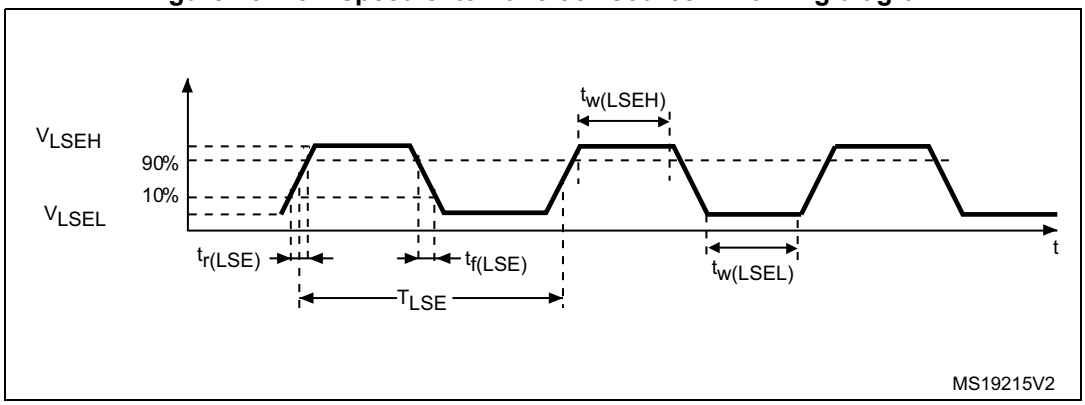
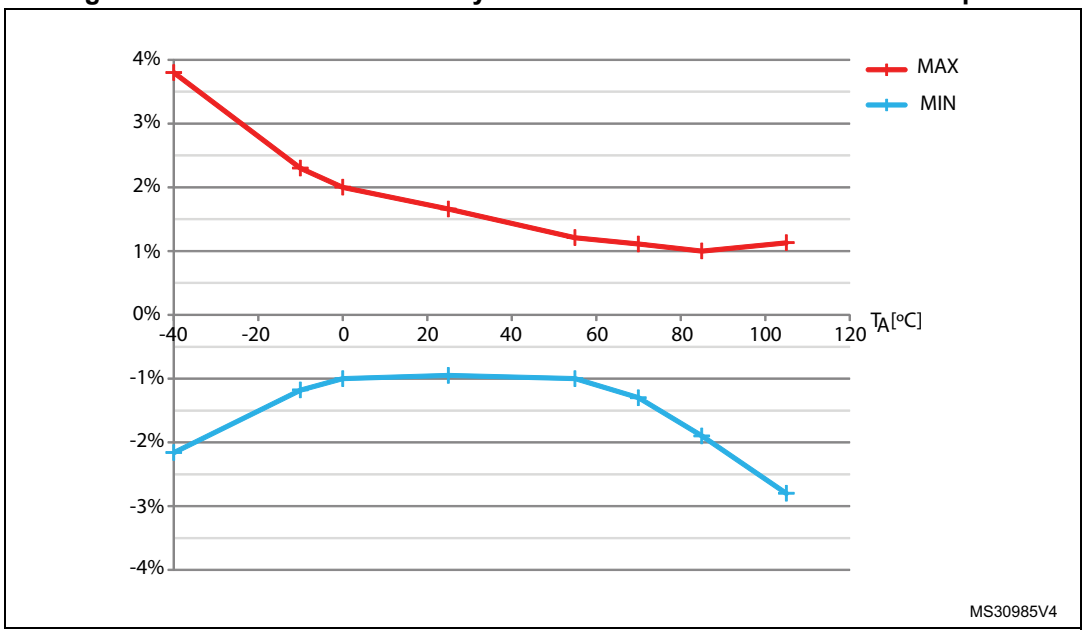


Figure 19. HSI oscillator accuracy characterization results for soldered parts



Low-speed internal (LSI) RC oscillator

Table 41. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

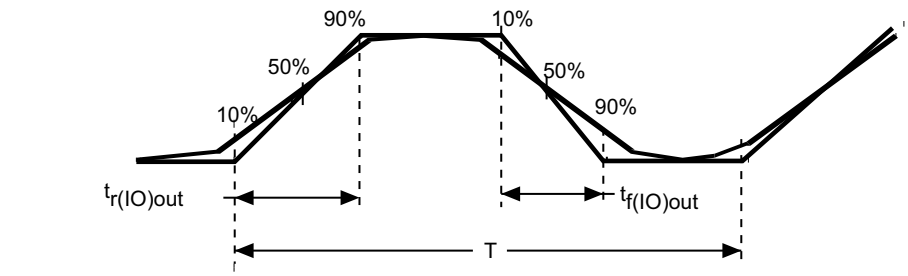
The parameters given in *Table 42* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19*.

Table 42. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	-	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
Jitter	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

Figure 40. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \le 2/3)T$ and if the duty cycle is (45-55%) when loaded by C_L (1)

MS36445V1

1. See *Table 68: I/O AC characteristics*.

6.3.16 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 66*).

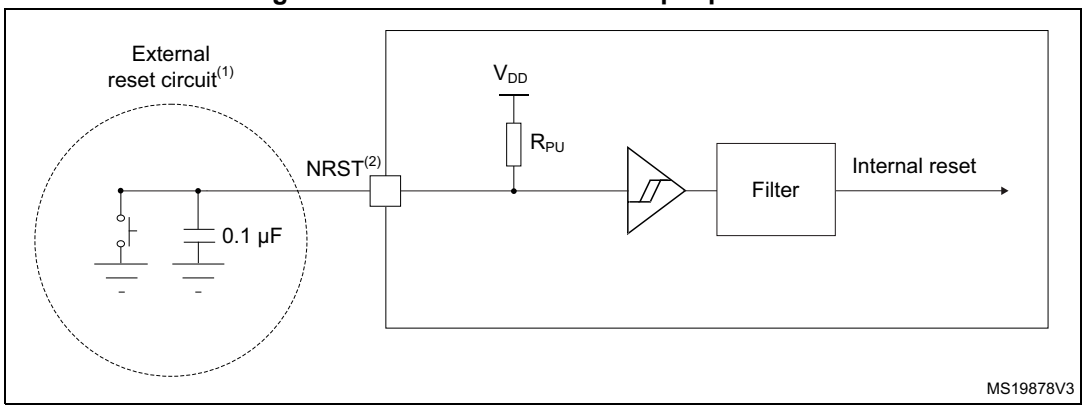
Unless otherwise specified, the parameters given in *Table 69* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*.

Table 69. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$ (1)	NRST Input low level voltage	-	-	-	$0.3V_{DD}+0.07$ (1)	V
$V_{IH(NRST)}$ (1)	NRST Input high level voltage	-	$0.445V_{DD}+0.398$ (1)	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor (2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$ (1)	NRST Input filtered pulse	-	-	-	100 (1)	ns
$V_{NF(NRST)}$ (1)	NRST Input not filtered pulse	-	500 (1)	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 41. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 69*. Otherwise the reset is not taken into account by the device.
3. Place the external capacitor 0.1u F on NRST as close as possible to the chip.

6.3.17 Timer characteristics

The parameters given in *Table 70* are guaranteed by design.

Refer to *Section 6.3.15: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 70. TIMx(1)(2) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9	-	ns
		$f_{TIMxCLK}$ = 144 MHz	6.95	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	36	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
		$f_{TIMxCLK}$ = 144 MHz	0.0069	455	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.65	s
		$f_{TIMxCLK}$ = 144 MHz	-	29.825	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM4, TIM15, TIM16 and TIM17 timers.
2. Guaranteed by design, not tested in production.

Table 71. IWDG min/max timeout period at 40 kHz (LSI) (1)

Prescaler divider	PR[2:0] bits	Min timeout (ms) RL[11:0]= 0x000	Max timeout (ms) RL[11:0]= 0xFFF
/4	0	0.1	409.6
/8	1	0.2	819.2
/16	2	0.4	1638.4
/32	3	0.8	3276.8
/64	4	1.6	6553.6
/128	5	3.2	13107.2
/256	7	6.4	26214.4

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 72. WWDG min-max timeout value @72 MHz (PCLK)(1)

Prescaler	WDGTB	Min timeout value	Max timeout value
1	0	0.05687	3.6409
2	1	0.1137	7.2817
4	2	0.2275	14.564
8	3	0.4551	29.127

1. Guaranteed by design, not tested in production.

6.3.18 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev.03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1Mbits/s

The I²C timings requirements are guaranteed by design when the I²C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.15: I/O port characteristics*.

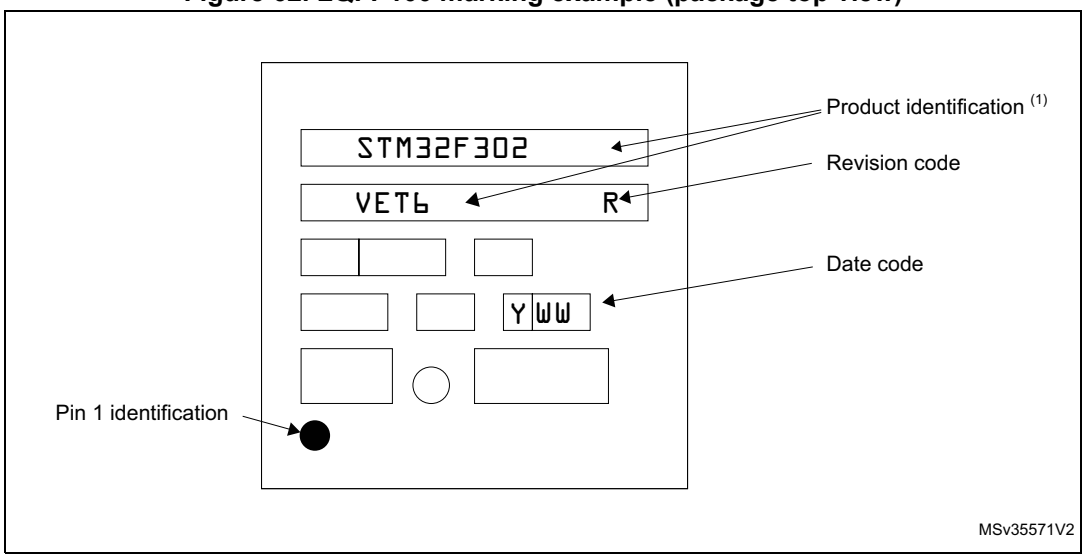
All I²C I/Os embed an analog filter, refer to the *Table 73: I2C analog filter characteristics*.

Device marking for LQFP100

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 62. LQFP100 marking example (package top view)

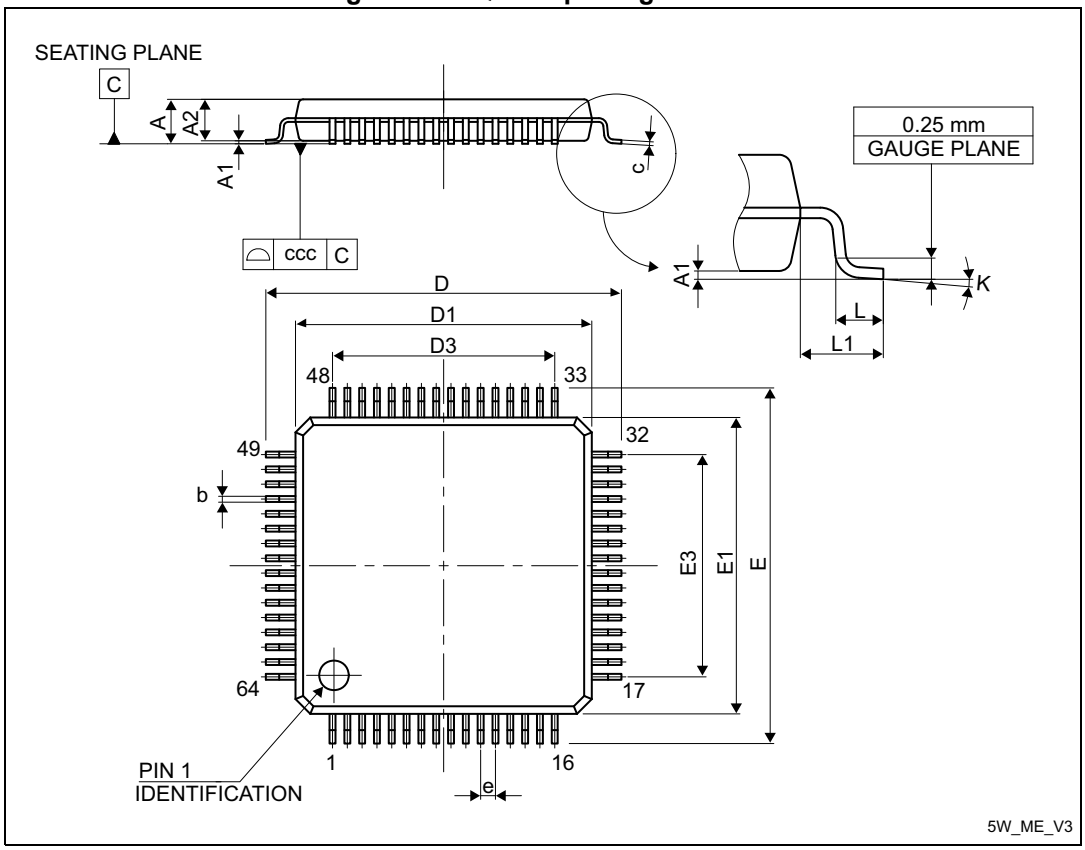


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.6 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.

Figure 66. LQFP64 package outline



1. Drawing is not to scale.

Table 98. LQFP64 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-