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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

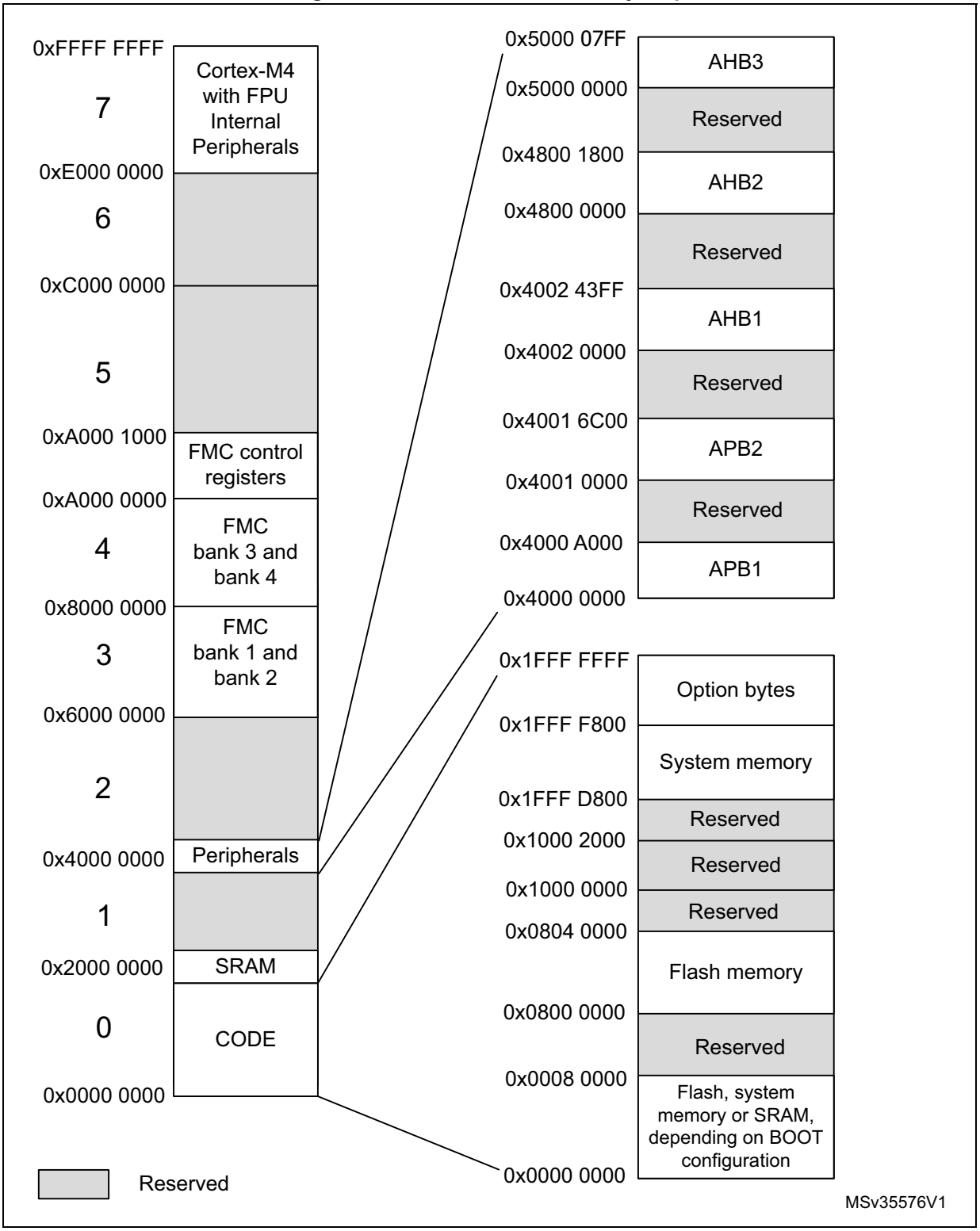
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302ret6

Table 13. STM32F302xD/E pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP100	LQFP144						
45	71	D1	104	PA12	I/O	FT	-	TIM16_CH1, I2SCKIN, TIM1_CH2N, USART1_RTS, COMP2_OUT, CAN_TX, TIM4_CH2, TIM1_ETR, EVENTOUT	USB_DP
46	72	E3	105	PA13	I/O	FT	-	SWDIO-JTMS, TIM16_CH1N, TSC_G4_IO3, IR-OUT, USART3_CTS, TIM4_CH3, EVENTOUT	-
-	-	-	106	PH2	I/O	FT	(1)	EVENTOUT	-
47	74	A1, A2, B1	107	VSS	S	-	-	-	-
48	75	D2	108	VDD	S	-	-	-	-
49	76	C2	109	PA14	I/O	FTf	-	SWCLK-JTCK, TSC_G4_IO4, I2C1_SDA, TIM1_BKIN, USART2_TX, EVENTOUT	-
50	77	B2	110	PA15	I/O	FTf	-	JTDI, TIM2_CH1/TIM2_ETR, TSC_SYNC, I2C1_SCL, SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_RX, TIM1_BKIN, EVENTOUT	-
51	78	E4	111	PC10	I/O	FT	-	EVENTOUT, UART4_TX, SPI3_SCK/I2S3_CK, USART3_TX	-
52	79	D3	112	PC11	I/O	FT	-	EVENTOUT, UART4_RX, SPI3_MISO/I2S3ext_SD, USART3_RX	-
53	80	A3	113	PC12	I/O	FT	-	EVENTOUT, UART5_TX, SPI3_MOSI/I2S3_SD, USART3_CK	-
-	81	B3	114	PD0	I/O	FT	(1)	EVENTOUT, CAN_RX, FMC_D2	-

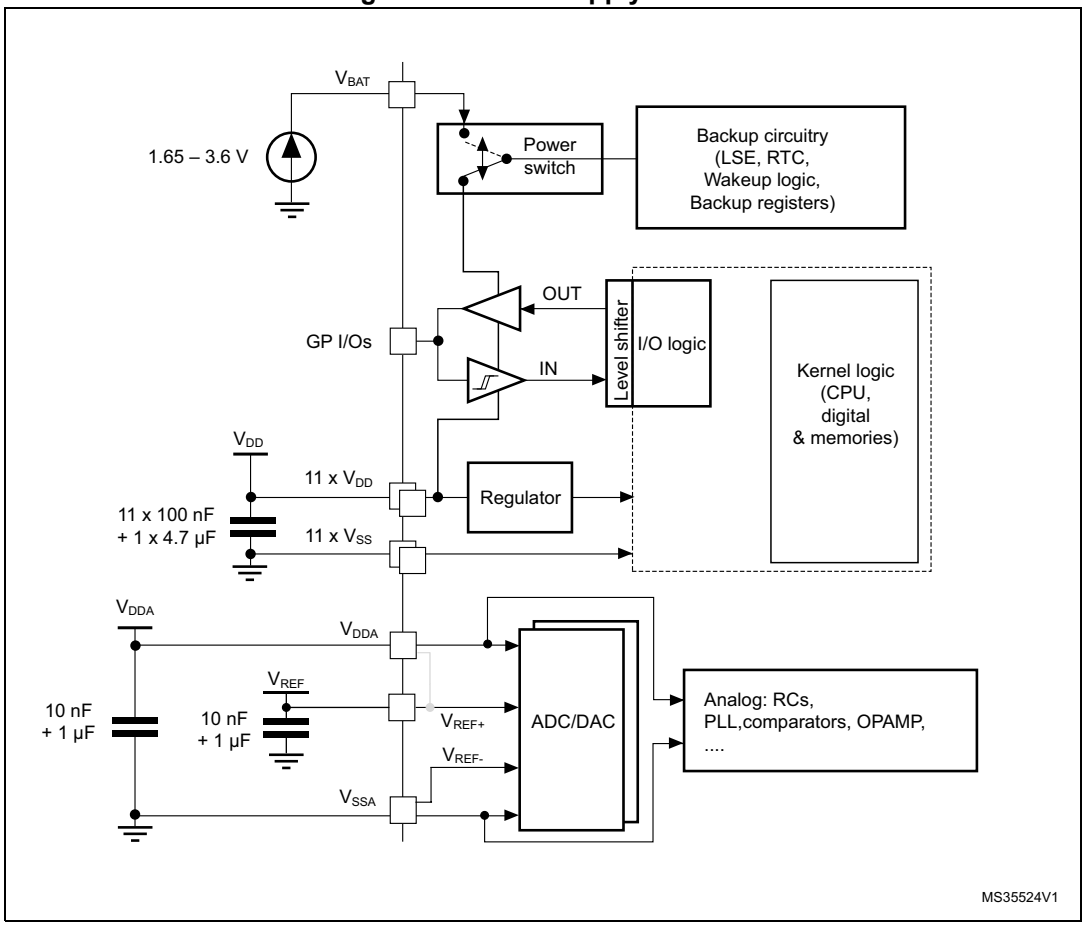
5 Memory mapping

Figure 9. STM32F302xD/E memory map



6.1.6 Power supply scheme

Figure 12. Power supply scheme



1. Dotted lines represent the internal connections on low pin count packages, joining the dedicated supply pins.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Table 22. Programmable voltage detector characteristics (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	V
		Falling edge	2.56	2.68	2.8	
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	
		Falling edge	2.66	2.78	2.9	
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
IDD(PVD)	PVD current consumption	-	-	0.15	0.26	µA

1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in *Table 23* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*.

Table 23. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.16	1.2	1.25	V
		–40 °C < T_A < +85 °C	1.16	1.2	1.24(1)	V
$T_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	-	2.2	-	-	µs
V_{RERINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV	-	-	10(2)	mV
T_{Coeff}	Temperature coefficient	-	-	-	100(2)	ppm/°C

1. Data based on characterization results, not tested in production.
2. Guaranteed by design, not tested in production.

Table 24. Internal reference voltage calibration values

Calibration value name	Description	Memory address
V_{REFINT_CAL}	Raw data acquired at temperature of 30 °C V_{DDA}= 3.3 V	0x1FFF F7BA - 0x1FFF F7BB

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 13: Current consumption measurement scheme*.

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

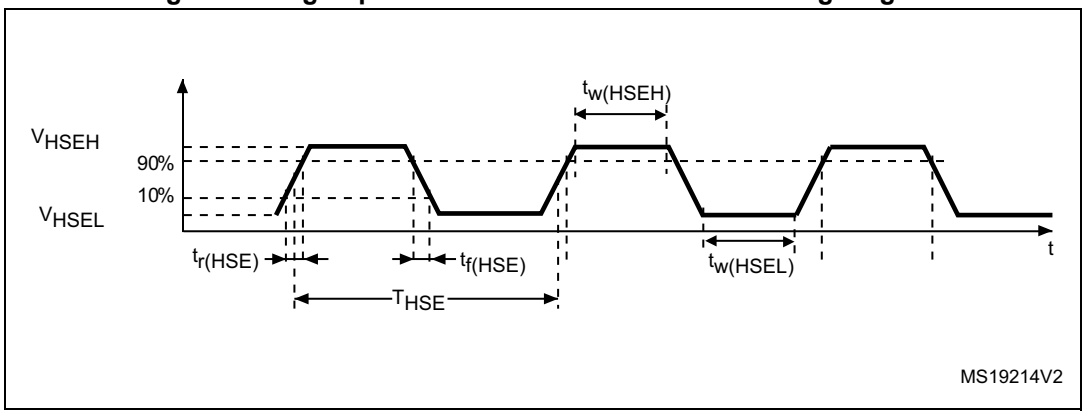
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.15*. However, the recommended clock input waveform is shown in *Figure 15*.

Table 36. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	1	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time(1)		15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	

1. Guaranteed by design, not tested in production.

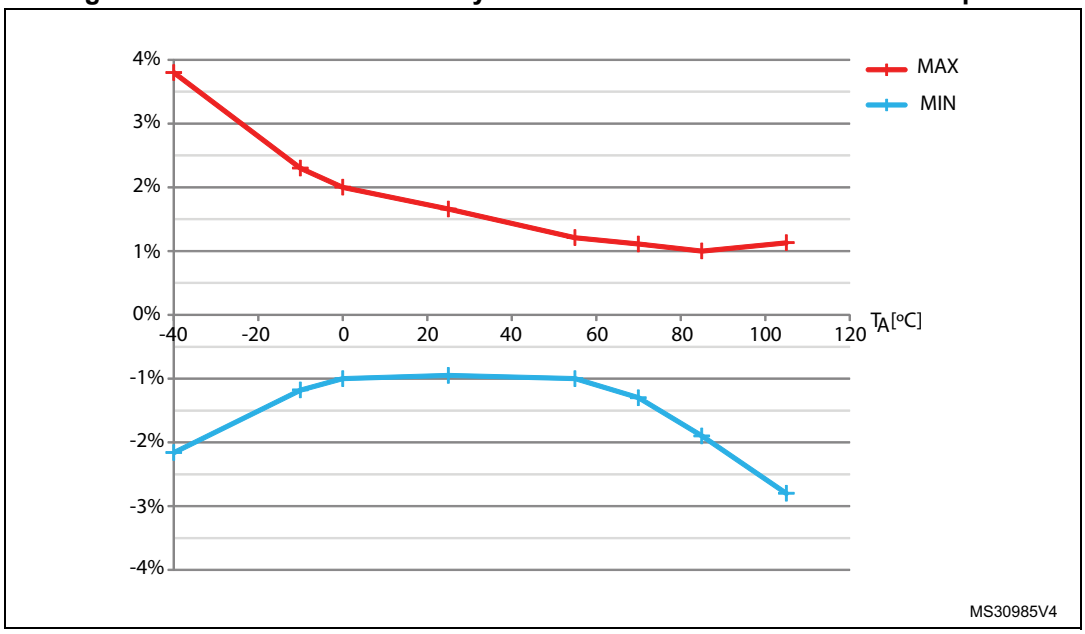
Figure 15. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in *Section 6.3.15*. However, the recommended clock input waveform is shown in *Figure 16*.

Figure 19. HSI oscillator accuracy characterization results for soldered parts



Low-speed internal (LSI) RC oscillator

Table 41. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in *Table 42* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19*.

Table 42. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	-	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
Jitter	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

Table 48. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	8THCLK+1	8THCLK+2	ns
$t_{w(NWE)}$	FMC_NWE low time	6THCLK-1	6THCLK+2	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	5THCLK-0.5	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4THCLK+2	-	

1. Based on characterization, not tested in production.

Table 49. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	8THCLK+2	8THCLK+2	ns
$t_{w(NOE)}$	FMC_NWE low time	6THCLK-1	6THCLK+1.5	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	4THCLK+6	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4THCLK-4	-	

1. Based on characterization, not tested in production.

Figure 24. Synchronous multiplexed NOR/PSRAM read timings

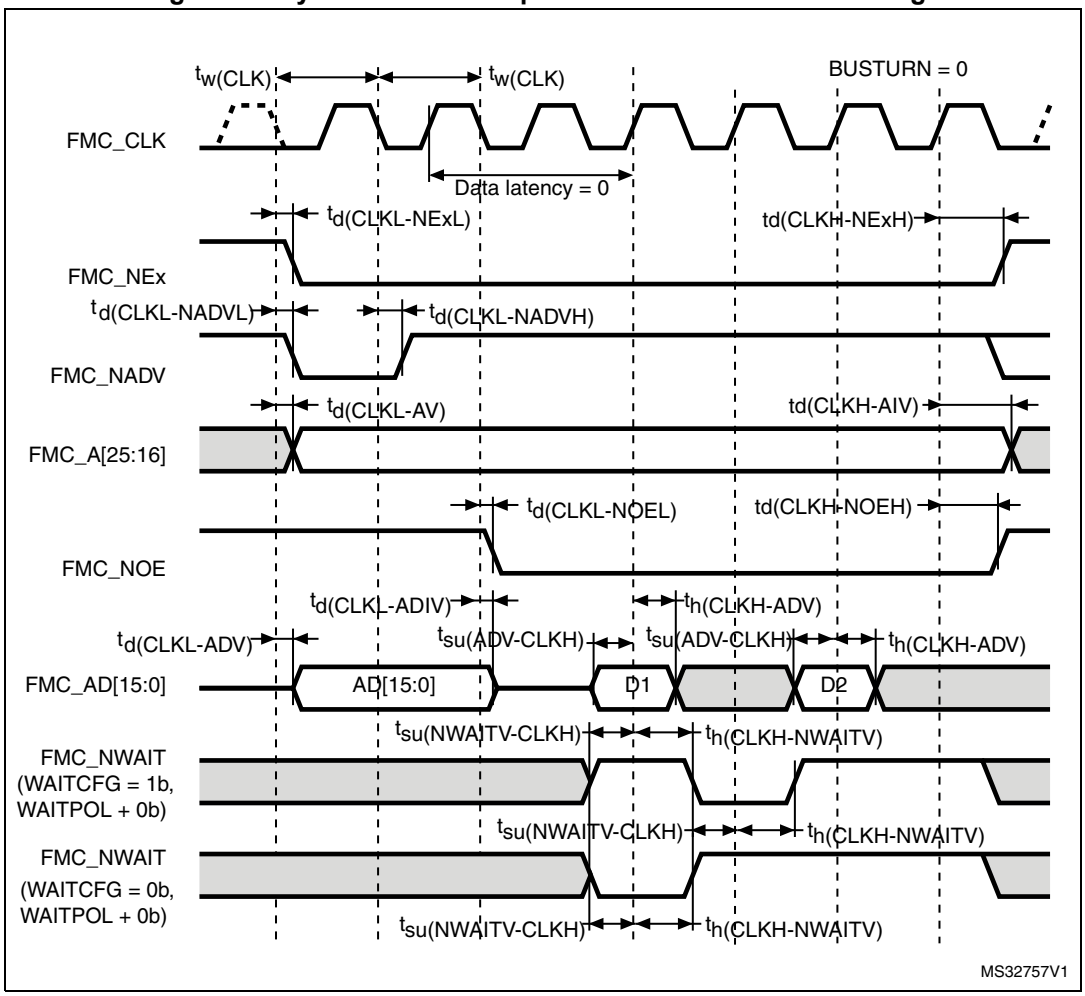


Table 53. Synchronous multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	2THCLK	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	5	
$t_{d(CLKH\_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	THCLK+1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	7	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	3	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	0	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	6	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	THCLK+1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	2	

Table 53. Synchronous multiplexed NOR/PSRAM read timings(1) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	ns
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	4	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	6	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. Based on characterization, not tested in production.

Figure 25. Synchronous multiplexed PSRAM write timings

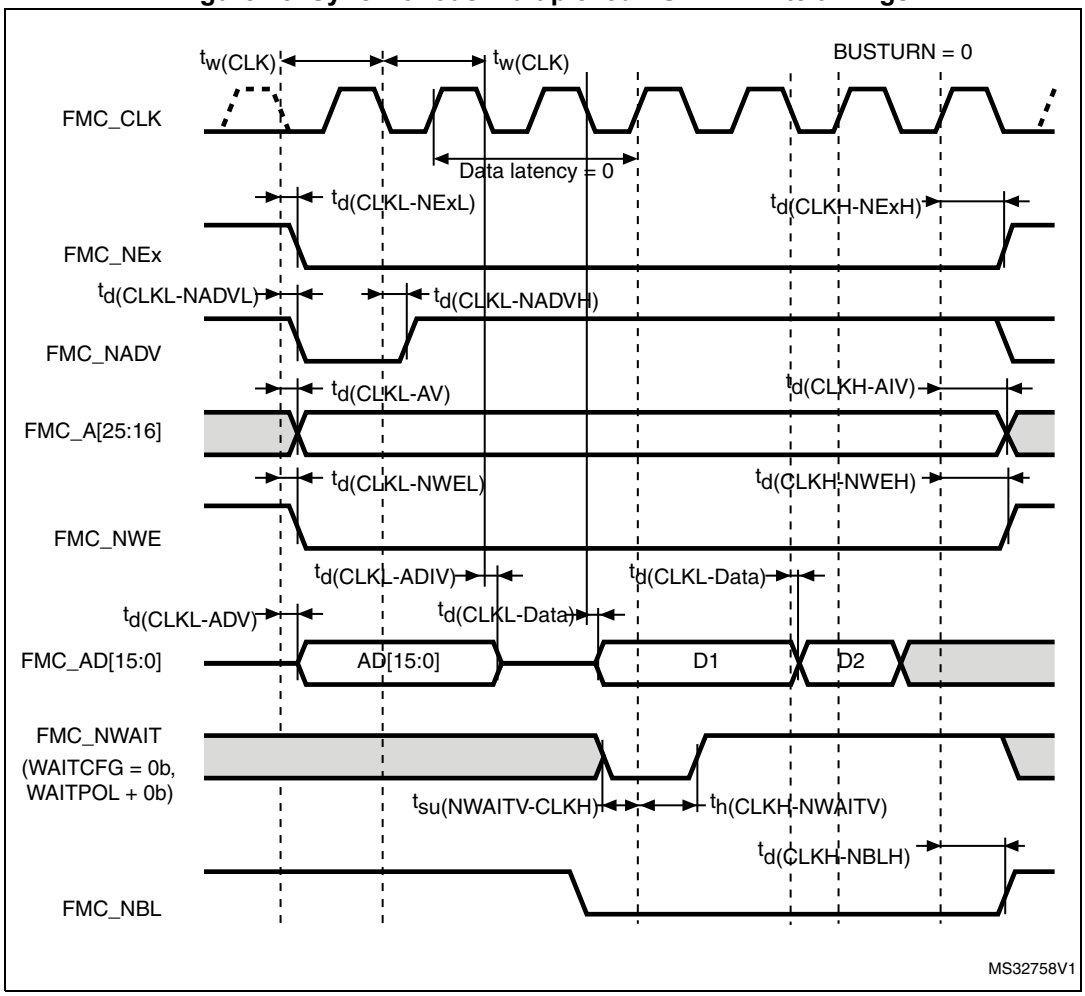


Table 54. Synchronous multiplexed PSRAM write timings(1) (2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period, VDD range= 2.7 to 3.6 V	2THCLK-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	5.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	THCLK+1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	7	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	0	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	5.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	THCLK+1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	7.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	8	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	6	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	THCLK+1	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	5	-	

1. Based on characterization, not tested in production.
2. C_L = 30 pF.

Table 75. I^2S characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256 x 8K	256xFs (2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	-
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	20	ns
$t_{h(WS)}$	WS hold time	Master mode	2	-	
$t_{su(WS)}$	WS setup time	Slave mode	0	-	
$t_{h(WS)}$	WS hold time	Slave mode	4	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD\_SR)}$		Slave receiver	1	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	8	-	
$t_{h(SD\_SR)}$		Slave receiver	2.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	50	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	22	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	8	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	1	-	

1. Data based on characterization results, not tested in production.
2. 256xFs maximum is 36 MHz (APB1 Maximum frequency)

*Note: Refer to the I^2S section in RM0365 Reference Manual for more details about the sampling frequency (Fs), f_{MCK}, f_{CK}, DCK values reflect only the digital peripheral behavior, source clock precision might slightly change the values DCK depends mainly on ODD bit value. Digital contribution leads to a min of (I2SDIV/(2*I2SDIV+ODD) and a max of (I2SDIV+ODD)/(2*I2SDIV+ODD) and Fs max supported for each mode/condition.*

Table 79. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S(1)	Sampling time	f_{ADC} = 72 MHz	0.021	-	8.35	µs
		-	1.5	-	601.5	$1/f_{ADC}$
$T_{ADCVREG\_STUP}$(1)	ADC Voltage Regulator Start-up time	-	-	-	10	µs
t_{CONV}(1)	Total conversion time (including sampling time)	f_{ADC} = 72 MHz Resolution = 12 bits	0.19	-	8.52	µs
		Resolution = 12 bits	14 to 614 (t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$
CMIR	Common Mode Input signal range	ADC differential mode	(V_{SSA} + V_{REF}+)/2 – 0.18	(V_{SSA} + V_{REF}+)/2	(V_{SSA} + V_{REF}+)/2 + 0.18	V

1. Data guaranteed by design, not tested in Production.
2. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pinout and pin description* for further details.

Figure 48. ADC typical current consumption on VDDA pin

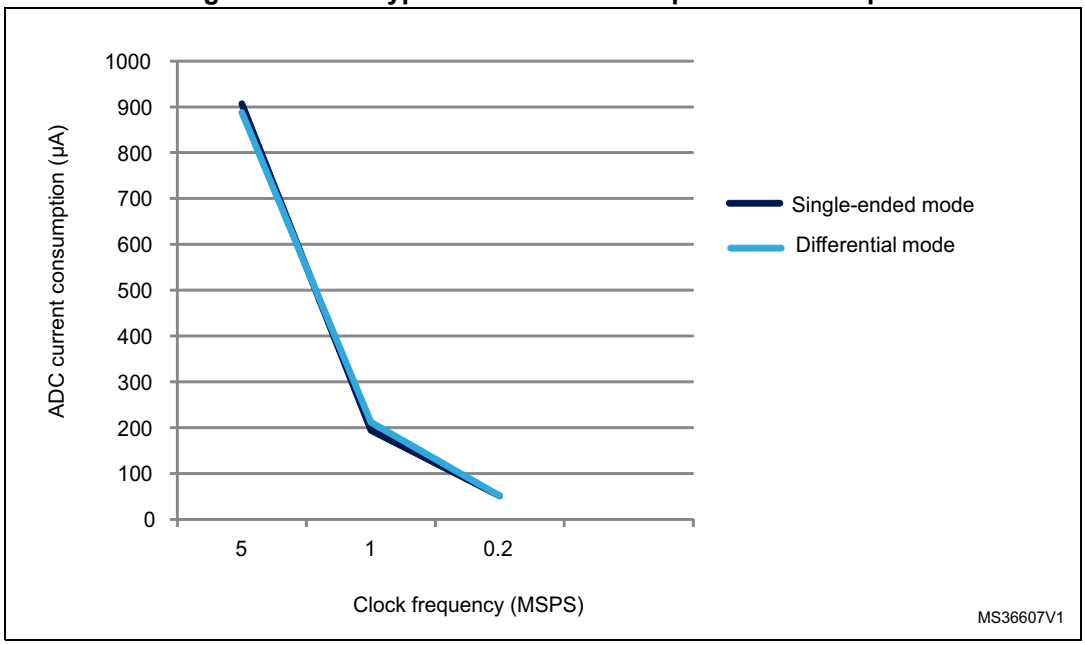


Table 85. ADC accuracy at 1MSPS(1)(2)

Symbol	Parameter	Test conditions		Typ	Max(3)	Unit
ET	Total unadjusted error	ADC Freq ≤ 72 MHz Sampling Freq ≤ 1MSPS 2.4 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V Single-ended mode	Fast channel	±2.5	±5	LSB
			Slow channel	±3.5	±5	
EO	Offset error		Fast channel	±1	±2.5	
			Slow channel	±1.5	±2.5	
EG	Gain error		Fast channel	±2	±3	
			Slow channel	±3	±4	
ED	Differential linearity error		Fast channel	±0.7	±2	
			Slow channel	±0.7	±2	
EL	Integral linearity error		Fast channel	±1	±3	
			Slow channel	±1.2	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for IINJ(PIN) and ∑IINJ(PIN) in *Section 6.3.15: I/O port characteristics* does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.

Figure 50. ADC accuracy characteristics

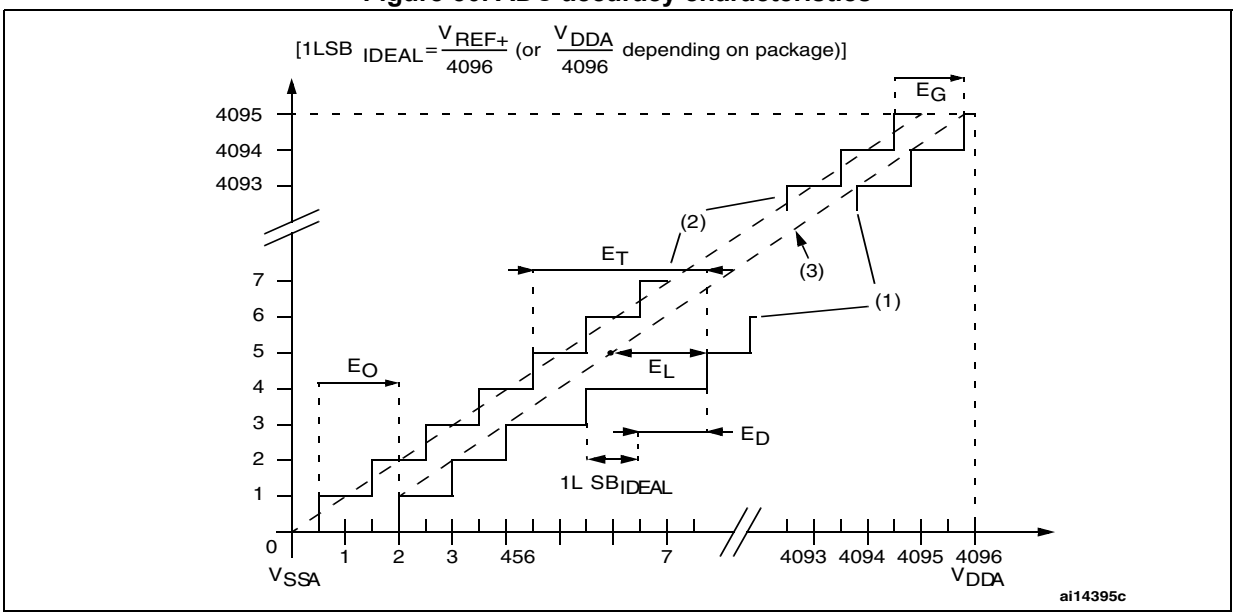
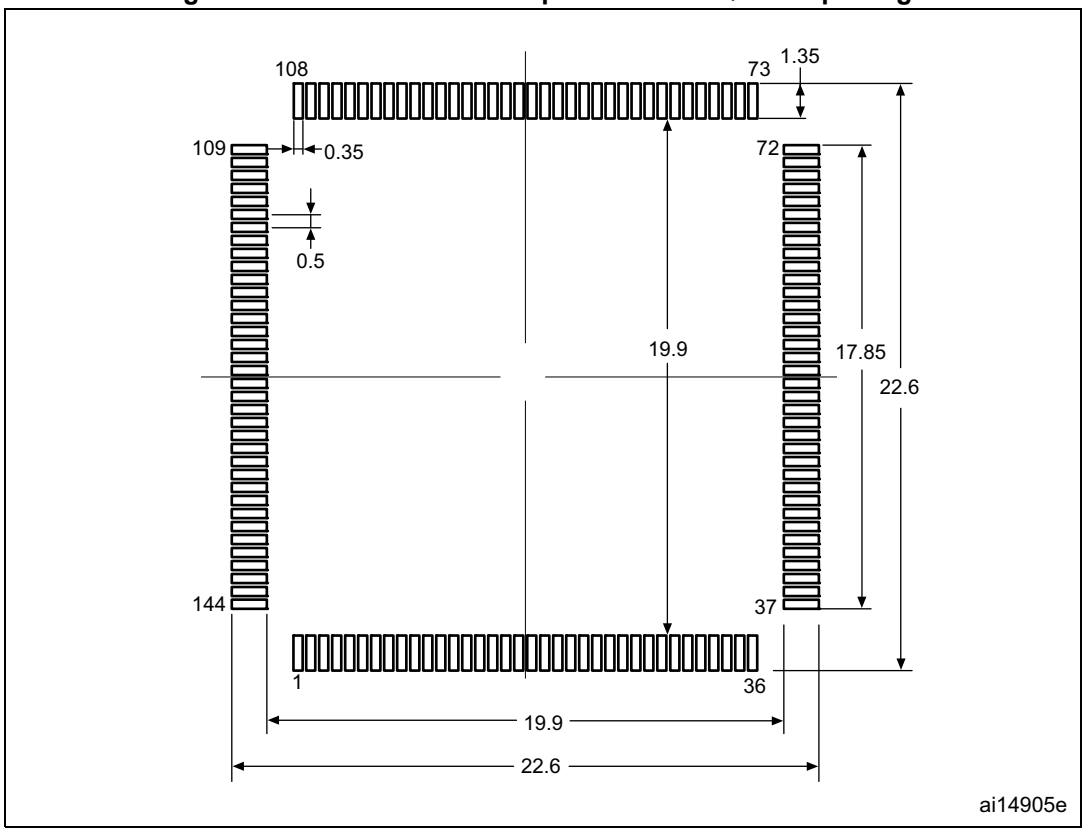


Figure 55. Recommended footprint for the LQFP144 package



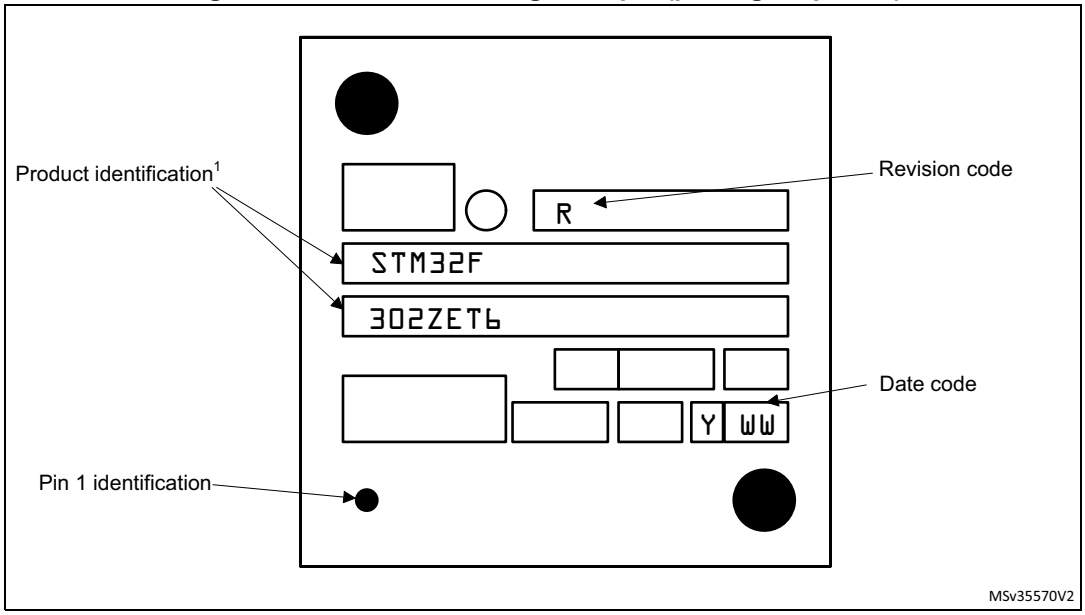
1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Device marking for LQFP144

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 56. LQFP144 marking example (package top view)

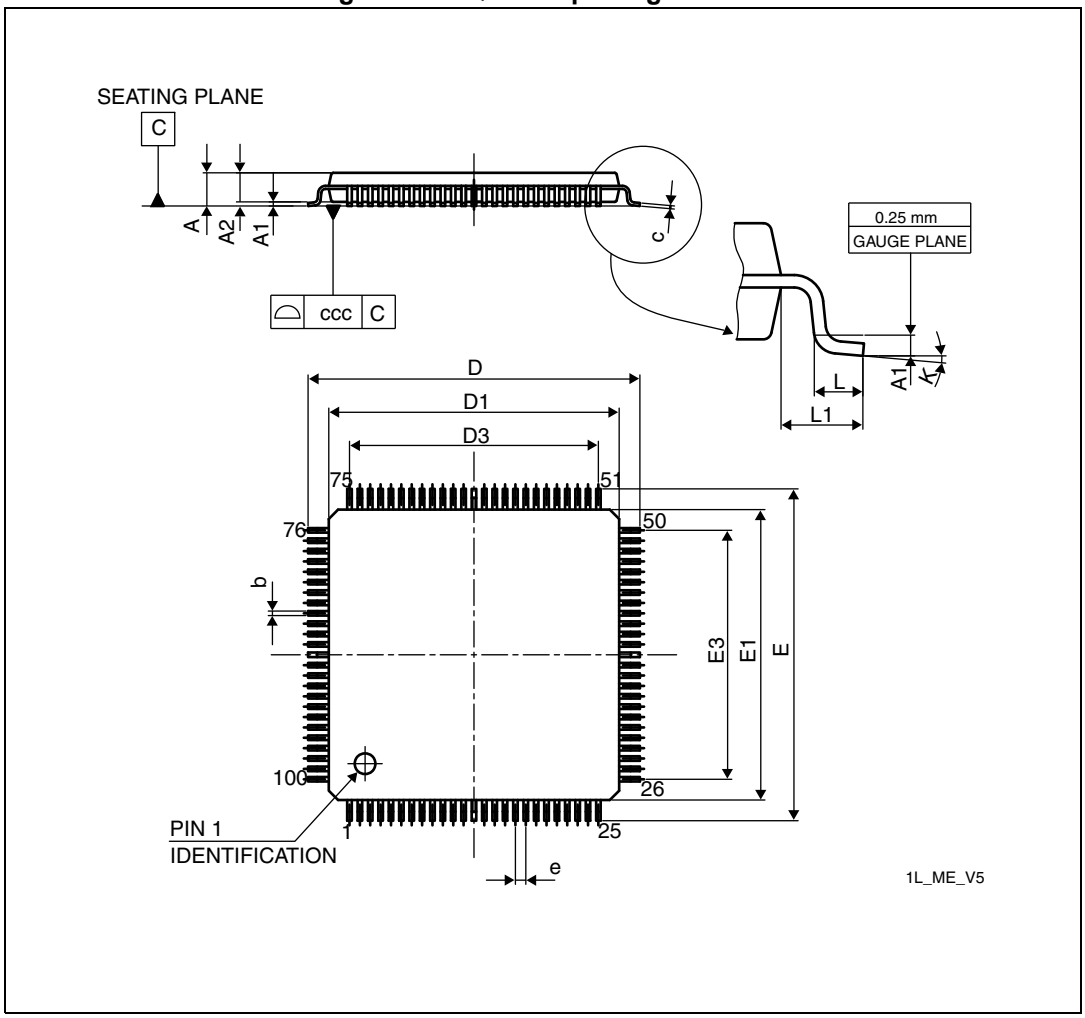


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.4 LQFP100 package information

LQFP100 is a 100-pin, 14 x 14 mm low-profile quad flat package.

Figure 60. LQFP100 package outline



1. Drawing is not to scale.

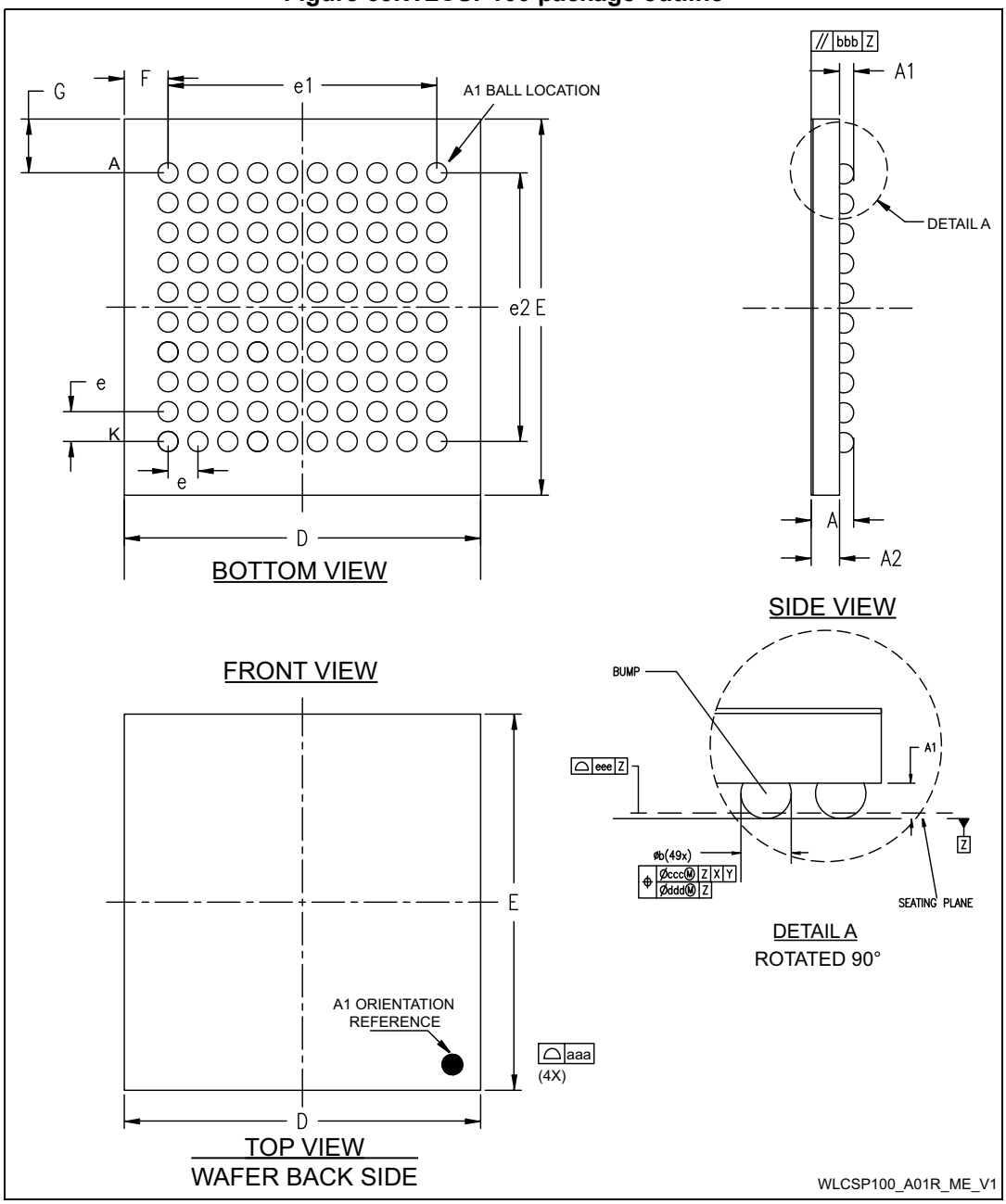
Table 95. LQPF100 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378

7.5 WLCSP100 package information

WLCSP100 is a 100-ball, 4.775 x 5.041 mm, 0.4 mm pitch wafer level chip scale package.

Figure 63.WLCSP100 package outline



1. Drawing is not to scale.

Table 97. WLCSP100 recommended PCB design rules (0.4 mm pitch)

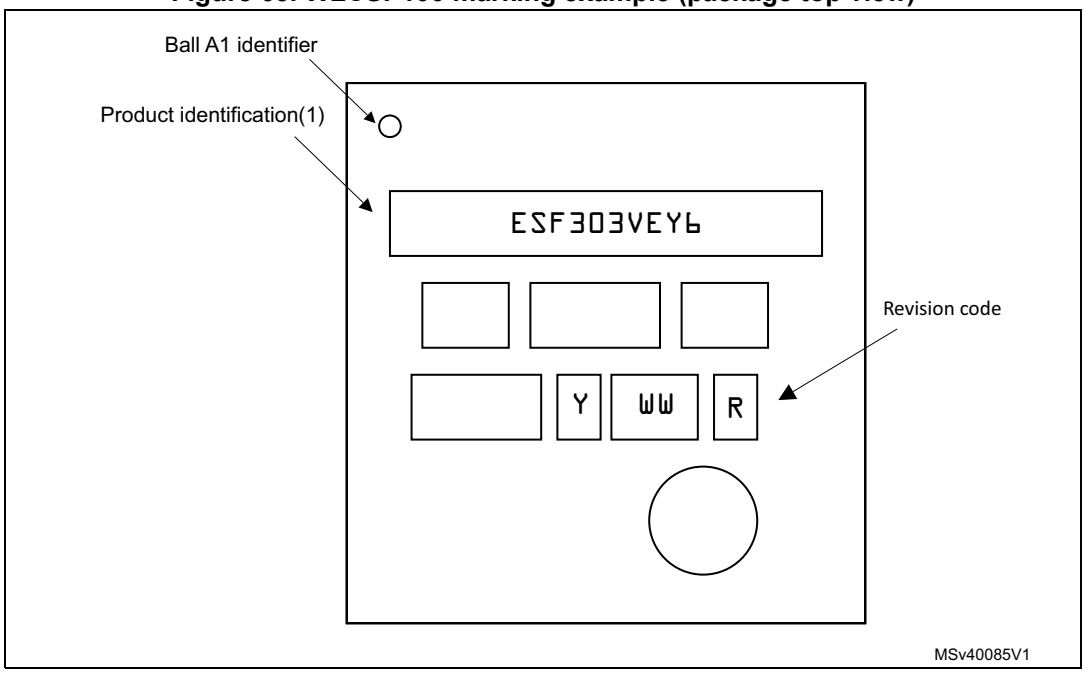
Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm
Stencil thickness	0.1 mm

Device marking for WLCSP100

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 65. WLCSP100 marking example (package top view)

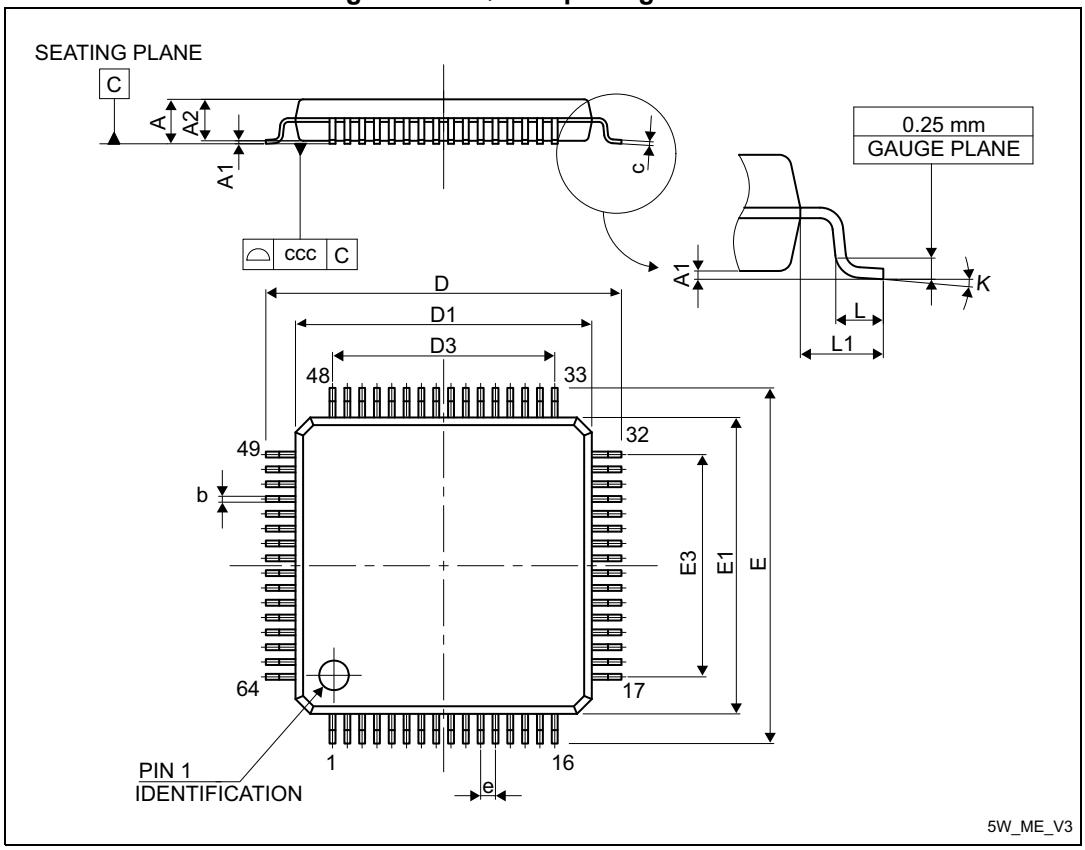


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.6 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.

Figure 66. LQFP64 package outline



1. Drawing is not to scale.

Table 98. LQFP64 package mechanical data

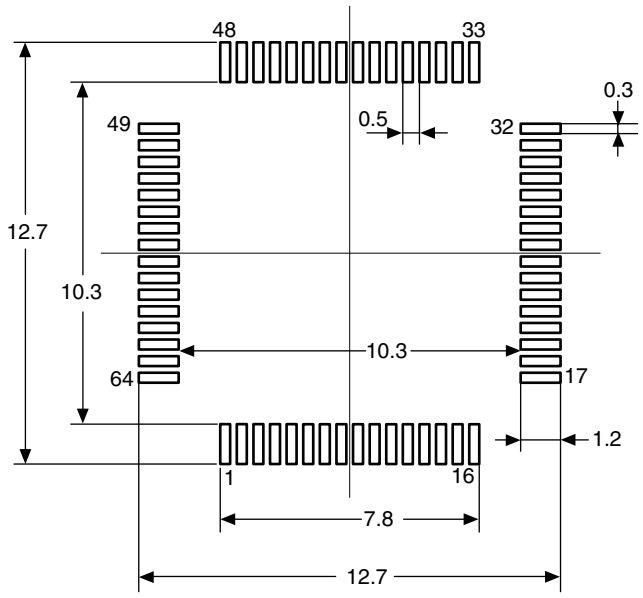
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Table 98. LQFP64 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 67. Recommended footprint for the LQFP64 package



1. Dimensions are expressed in millimeters.