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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302ret7

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F302xD/E microcontrollers.

This STM32F302xD/E datasheet should be read in conjunction with the reference manual of STM32F302xB/C/D/E, STM32F302x6/8 devices (RM0365) available on STMicroelectronics website at *www.st.com*.

For information on the ARM® Cortex®-M4 core with FPU, refer to the following documents:

- *Cortex® -M4 with FPU Technical Reference Manual*, available from the www.arm.com website
- *STM32F3 and STM32F4 Series Cortex® -M4 programming manual* (PM0214) available on STMicroelectronics website at *www.st.com*.

3 Functional overview

3.1 ARM® Cortex®-M4 core with FPU with embedded Flash and SRAM

The ARM® Cortex®-M4 processor with FPU is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 32-bit RISC processor with FPU features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allows efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F302xD/E family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32F302xD/E family devices.

3.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU manage up to 8 protection areas that are further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS detects it and takes action. In an RTOS environment, the kernel dynamically updates the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.3 Embedded Flash memory

All STM32F302xD/E devices feature 384/512 Kbyte of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

All I²C bus interfaces support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 6. Comparison of I²C analog and digital filters

-	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I²C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, they provide hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. They also have a clock domain independent from the CPU clock, allowing the I2Cx (x=1,2,3) to wake up the MCU from Stop mode on address match.

The I²C interfaces can be served by the DMA controller.

Refer to *Table 7* for the features available in I2C1, I2C2 and I2C3.

Table 7. STM32F302xD/E I²C implementation

I²C features[1]	I2C1	I2C2	I2C3
7-bit addressing mode	X	X	X
10-bit addressing mode	X	X	X
Standard mode (up to 100 kbit/s)	X	X	X
Fast mode (up to 400 kbit/s)	X	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X	X
Independent clock	X	X	X
SMBus	X	X	X
Wakeup from STOP	X	X	X

1. X = supported.

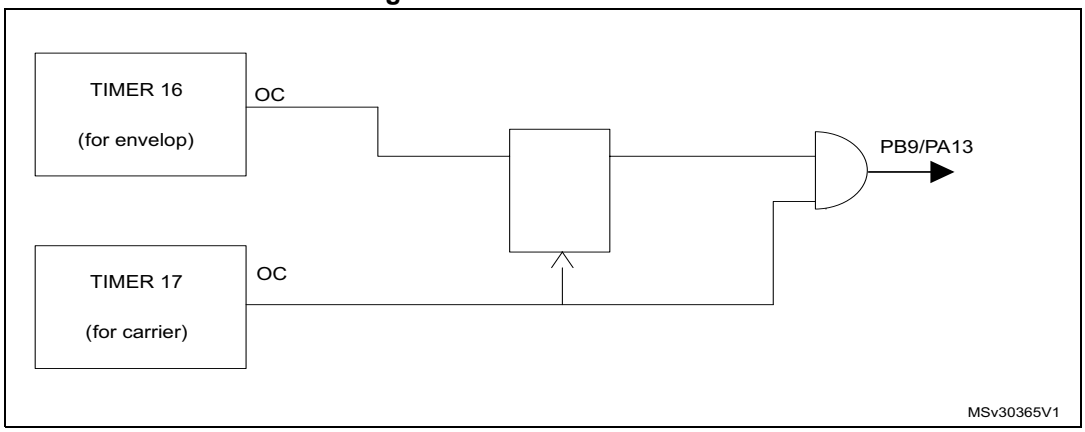
3.21 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F302xD/E devices have three embedded universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

The USART interfaces are able to communicate at speeds of up to 9 Mbit/s.

They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex

Figure 3. Infrared transmitter



3.27 Touch sensing controller (TSC)

The STM32F302xD/E devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 24 capacitive sensing channels distributed over 8 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic, etc.). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 10. Capacitive sensing GPIOs available on STM32F302xD/E devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4	6	TSC_G6_IO1	PB11
	TSC_G2_IO2	PA5		TSC_G6_IO2	PB12
	TSC_G2_IO3	PA6		TSC_G6_IO3	PB13
	TSC_G2_IO4	PA7		TSC_G6_IO4	PB14

Table 10. Capacitive sensing GPIOs available on STM32F302xD/E devices (continued)

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
3	TSC_G3_IO1	PC5	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PB0		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB1		TSC_G7_IO3	PE4
	TSC_G3_IO4	PB2		TSC_G7_IO4	PE5
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PD12
	TSC_G4_IO2	PA10		TSC_G8_IO2	PD13
	TSC_G4_IO3	PA13		TSC_G8_IO3	PD14
	TSC_G4_IO4	PA14		TSC_G8_IO4	PD15

Table 11. Number of capacitive sensing channels available on STM32F302xD/E devices

Analog I/O group	Number of capacitive sensing channels	
	STM32F302VE/ZE	STM32F302RE
G1	3	3
G2	3	3
G3	3	3
G4	3	3
G5	3	3
G6	3	3
G7	3	0
G8	3	0
Number of capacitive sensing channels	24	18

3.28 Development support

3.28.1 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.28.2 Embedded Trace Macrocell

The ARM embedded trace macrocell (ETM™) provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F302xD/E through a small number of ETM™ pins to an external hardware trace

Table 13. STM32F302xD/E pin definitions (continued)

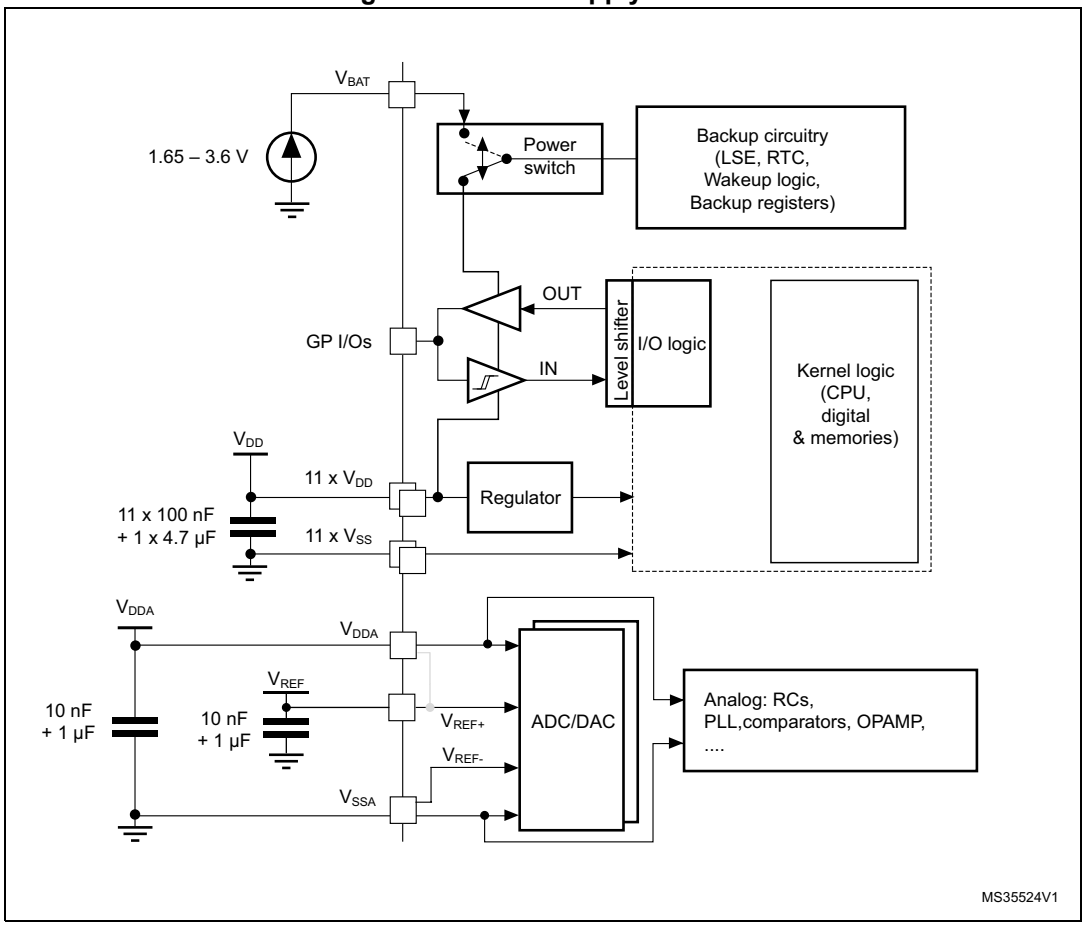
Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP100	LQFP144						
-	38	F8	58	PE7	I/O	TTa	(1)	EVENTOUT, TIM1_ETR, FMC_D4	-
-	39	E6	59	PE8	I/O	TTa	(1)	EVENTOUT, TIM1_CH1N, FMC_D5	COMP4_INM
-	40	-	60	PE9	I/O	TTa	(1)	EVENTOUT, TIM1_CH1, FMC_D6	-
-	-	-	61	VSS	S	-	(1)	-	-
-	-	-	62	VDD	S	-	(1)	-	-
-	41	-	63	PE10	I/O	TTa	(1)	EVENTOUT, TIM1_CH2N, FMC_D7	-
-	42	H5	64	PE11	I/O	TTa	(1)	EVENTOUT, TIM1_CH2, SPI4_NSS, FMC_D8	-
-	43	G5	65	PE12	I/O	TTa	(1)	EVENTOUT, TIM1_CH3N, SPI4_SCK, FMC_D9	-
-	44	-	66	PE13	I/O	TTa	(1)	EVENTOUT, TIM1_CH3, SPI4_MISO, FMC_D10	-
-	45	-	67	PE14	I/O	TTa	(1)	EVENTOUT, TIM1_CH4, SPI4_MOSI, TIM1_BKIN2, FMC_D11	-
-	46	-	68	PE15	I/O	TTa	(1)	EVENTOUT, TIM1_BKIN, USART3_RX, FMC_D12	-
29	47	K4	69	PB10	I/O	TTa	-	TIM2_CH3, TSC_SYNC, USART3_TX, EVENTOUT	-
30	48	K3	70	PB11	I/O	TTa	-	TIM2_CH4, TSC_G6_IO1, USART3_RX, EVENTOUT	ADC12_IN14, COMP6_INP
31	49	K1, J1, K2	71	VSS	S	-	-	-	-
32	50	J5	72	VDD	S	-	-	-	-
33	51	J4	73	PB12	I/O	TTa	(5)	TSC_G6_IO2, I2C2_SMBAL, SPI2_NSS/I2S2_WS, TIM1_BKIN, USART3_CK, EVENTOUT	-

Table 15. Memory map, peripheral register boundary addresses (continued)

Bus	Boundary address	Size (bytes)	Peripheral
APB2	0x4001 2C00 - 0x4001 2FFF	1 K	TIM1
	0x4001 0800 - 0x4001 2BFF	9 K	Reserved
	0x4001 0400 - 0x4001 07FF	1 K	EXTI
	0x4001 0000 - 0x4001 03FF	1 K	SYSCFG + COMP + OPAMP
-	0x4000 7C00 - 0x4000 FFFF	32 K	Reserved
APB1	0x4000 7800 - 0x4000 7BFF	1 K	I2C3
	0x4000 7400 - 0x4000 77FF	1 K	DAC
	0x4000 7000 - 0x4000 73FF	1 K	PWR
	0x4000 6800 - 0x4000 6FFF	2 K	Reserved
	0x4000 6400 - 0x4000 67FF	1 K	bxCAN
	0x4000 6000 - 0x4000 63FF	1 K	USB/CAN SRAM
	0x4000 5C00 - 0x4000 5FFF	1 K	USB device FS
	0x4000 5800 - 0x4000 5BFF	1 K	I2C2
	0x4000 5400 - 0x4000 57FF	1 K	I2C1
	0x4000 5000 - 0x4000 53FF	1 K	UART5
	0x4000 4C00 - 0x4000 4FFF	1 K	UART4
	0x4000 4800 - 0x4000 4BFF	1 K	USART3
	0x4000 4400 - 0x4000 47FF	1 K	USART2
	0x4000 4000 - 0x4000 43FF	1 K	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	1 K	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	1 K	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 K	I2S2ext
	0x4000 3000 - 0x4000 33FF	1 K	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 K	WWDG
	0x4000 2800 - 0x4000 2BFF	1 K	RTC
	0x4000 1800 - 0x4000 27FF	4 K	Reserved
	0x4000 1000 - 0x4000 13FF	1 K	TIM6
	0x4000 0C00 - 0x4000 0FFF	1 K	Reserved
	0x4000 0800 - 0x4000 0BFF	1 K	TIM4
	0x4000 0400 - 0x4000 07FF	1 K	TIM3
	0x4000 0000 - 0x4000 03FF	1 K	TIM2

6.1.6 Power supply scheme

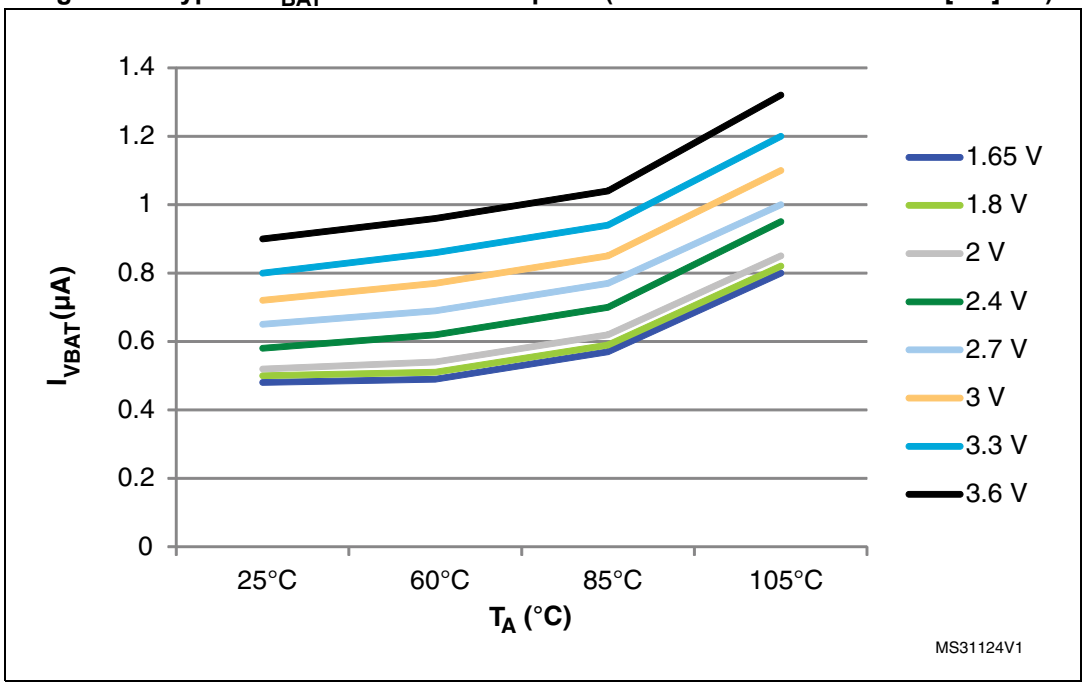
Figure 12. Power supply scheme



1. Dotted lines represent the internal connections on low pin count packages, joining the dedicated supply pins.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Figure 14. Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0] 00')



Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3$ V
- All I/O pins available on each package are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states from 48 MHz to 72 MHz), and Flash prefetch is ON
- When the peripherals are enabled, $f_{APB1} = f_{AHB/2}$, $f_{APB2} = f_{AHB}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8,16 and 64 is used for the frequencies 4 MHz, 2 MHz, 1 MHz, 500 kHz and 125 kHz respectively.

Table 48. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	8THCLK+1	8THCLK+2	ns
$t_{w(NWE)}$	FMC_NWE low time	6THCLK-1	6THCLK+2	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	5THCLK-0.5	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4THCLK+2	-	

1. Based on characterization, not tested in production.

Table 49. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	8THCLK+2	8THCLK+2	ns
$t_{w(NOE)}$	FMC_NWE low time	6THCLK-1	6THCLK+1.5	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	4THCLK+6	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	4THCLK-4	-	

1. Based on characterization, not tested in production.

Figure 24. Synchronous multiplexed NOR/PSRAM read timings

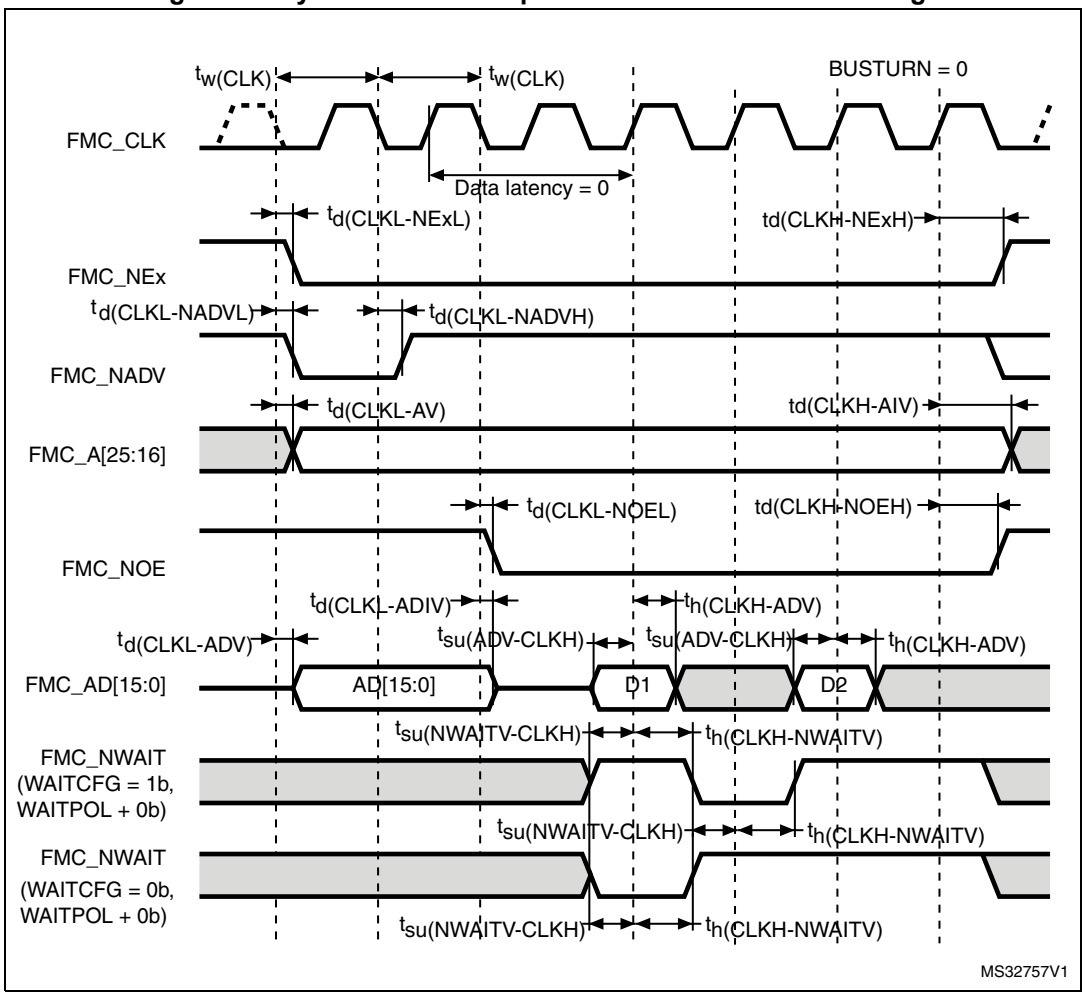


Table 53. Synchronous multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	2THCLK	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	5	
$t_{d(CLKH\_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	THCLK+1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	7	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	3	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	0	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	6	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	THCLK+1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	2	

Figure 26. Synchronous non-multiplexed NOR/PSRAM read timings

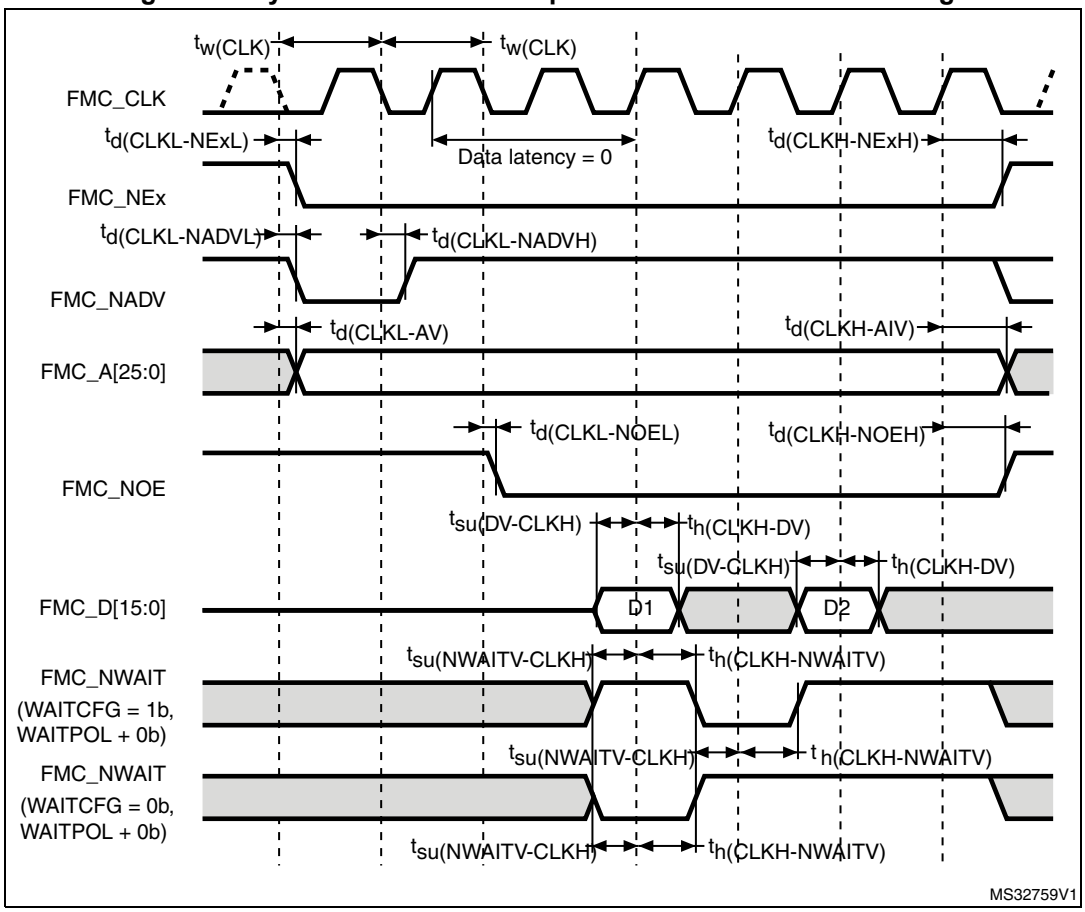


Table 55. Synchronous non-multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	2THCLK-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	THCLK+1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	7	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	7	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	THCLK	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	6	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	THCLK+1	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	3.5	-	

Table 56. Synchronous non-multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	2THCLK-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	6	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	THCLK+1.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	7.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	6.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	0	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	0	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	THCLK+2	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	7.5	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	7	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	THCLK+0.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. Based on characterization, not tested in production.

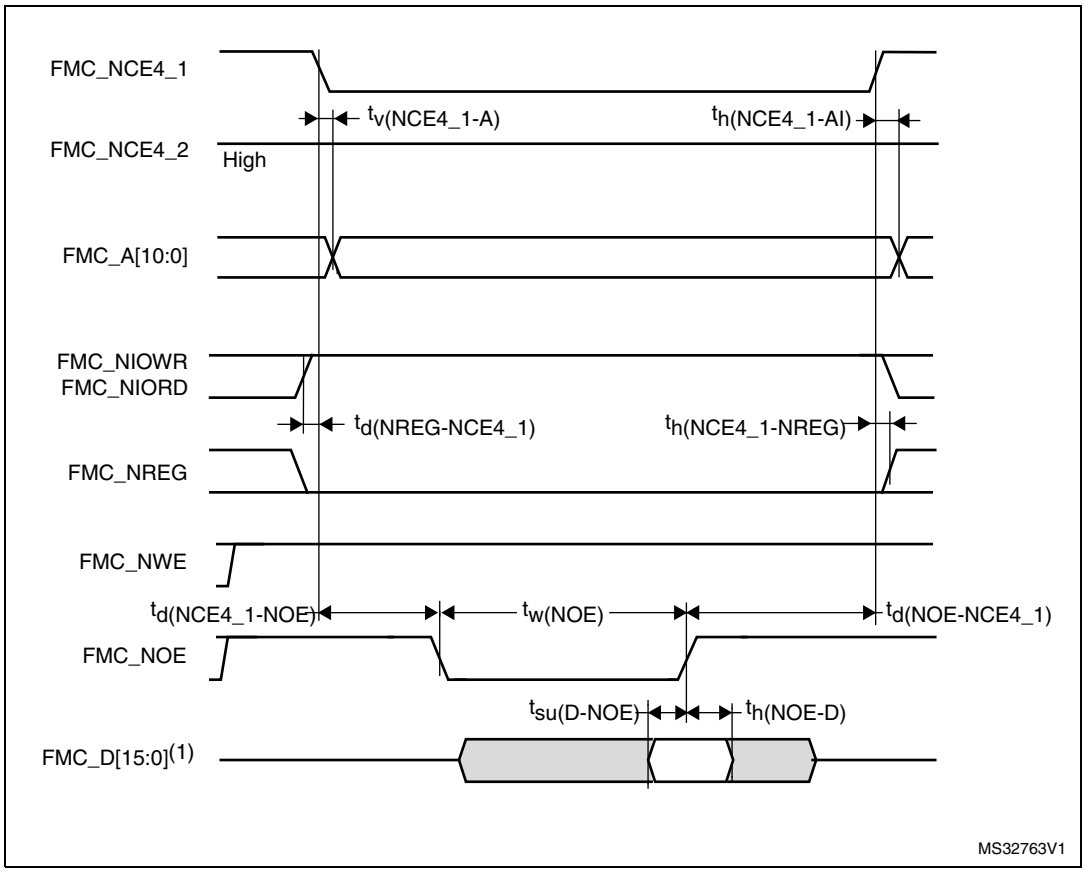
PC Card/CompactFlash controller waveforms and timings

Figure 28 to *Figure 33* present the PC Card/Compact Flash controller waveforms, and *Table 57* to *Table 58* provide the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FMC_SetupTime = 0x04;
- COM.FMC_WaitSetupTime = 0x07;
- COM.FMC_HoldSetupTime = 0x04;
- COM.FMC_HiZSetupTime = 0x05;
- ATT.FMC_SetupTime = 0x04;
- ATT.FMC_WaitSetupTime = 0x07;
- ATT.FMC_HoldSetupTime = 0x04;
- ATT.FMC_HiZSetupTime = 0x05;
- IO.FMC_SetupTime = 0x04;
- IO.FMC_WaitSetupTime = 0x07;
- IO.FMC_HoldSetupTime = 0x04;
- IO.FMC_HiZSetupTime = 0x05;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

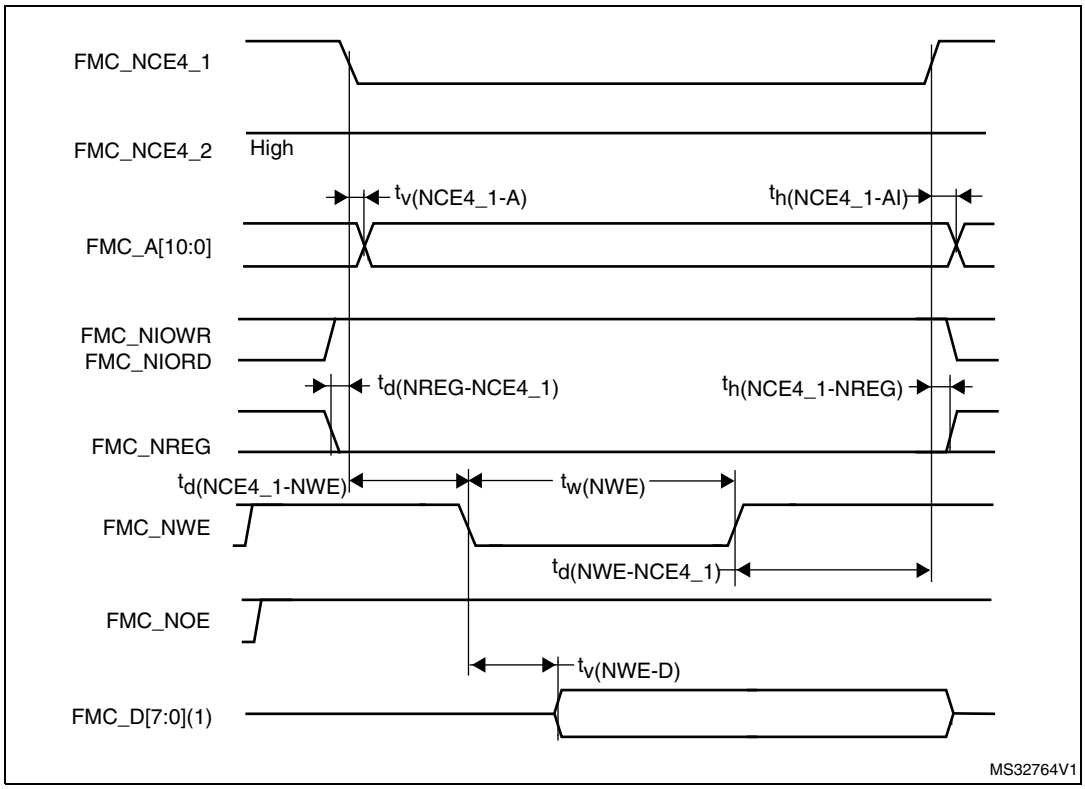
In all timing tables, the THCLK is the HCLK clock period.

Figure 30. PC Card/CompactFlash controller waveforms for attribute memory read access



1. Only data bits 0...7 are read (bits 8...15 are disregarded).

Figure 31. PC Card/CompactFlash controller waveforms for attribute memory write access



1. Only data bits 0...7 are driven (bits 8...15 remains Hi-Z).

Table 58. Switching characteristics for PC Card/CF read and write cycles in I/O space(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NIOWR)}$	FMC_NIOWR low width	8THCLK-0.5	-	ns
$t_{v(NIOWR-D)}$	FMC_NIOWR low to FMC_D[15:0] valid	-	5.5	
$t_{h(NIOWR-D)}$	FMC_NIOWR high to FMC_D[15:0] invalid	4THCLK-0.5	-	
$t_{d(NCE4\_1-NIOWR)}$	FMC_NCE4_1 low to FMC_NIOWR valid	-	5THCLK+1	
$t_{h(NCEx-NIOWR)}$	FMC_NCEx high to FMC_NIOWR invalid	4THCLK+0.5	-	
$t_{d(NIORD-NCEx)}$	FMC_NCEx low to FMC_NIORD valid	-	5THCLK	
$t_{h(NCEx-NIORD)}$	FMC_NCEx high to FMC_NIORD) valid	6THCLK+2	-	
$t_{w(NIORD)}$	FMC_NIORD low width	8THCLK-1	8THCLK+1	
$t_{su(D-NIORD)}$	FMC_D[15:0] valid before FMC_NIORD high	THCLK+2	-	
$t_{d(NIORD-D)}$	FMC_D[15:0] valid after FMC_NIORD high	0	-	

1. Based on characterization, not tested in production.

NAND controller waveforms and timings

Figure 34 and *Figure 35* present the NAND controller synchronous waveforms, and *Table 59* and *Table 60* provide the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FMC_SetupTime = 0x01;
- COM.FMC_WaitSetupTime = 0x03;
- COM.FMC_HoldSetupTime = 0x02;
- COM.FMC_HiZSetupTime = 0x03;
- ATT.FMC_SetupTime = 0x01;
- ATT.FMC_WaitSetupTime = 0x03;
- ATT.FMC_HoldSetupTime = 0x02;
- ATT.FMC_HiZSetupTime = 0x03;
- Bank = FMC_Bank_NAND;
- MemoryDataWidth = FMC_MemoryDataWidth_16b;
- ECC = FMC_ECC_Enable;
- ECCPageSize = FMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0.

In all timing tables, the THCLK is the HCLK clock period.

Figure 34. NAND controller read timings

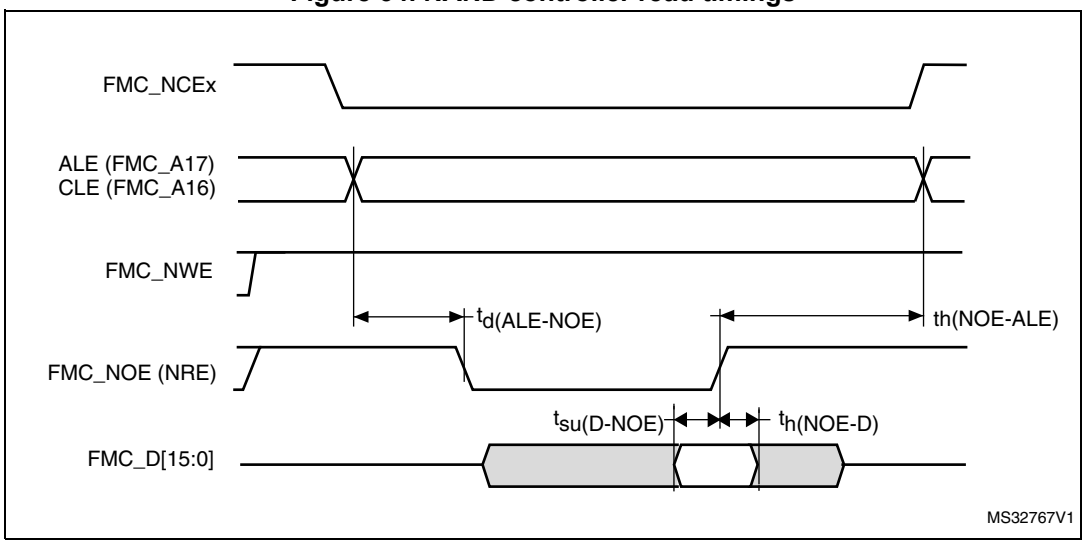


Table 66. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{lkg}	Input leakage current (3)	TC, FT and FTf I/O TTa I/O in digital mode $V_{SS} \le V_{IN} \le V_{DD}$	-	-	±0.1	µA
		TTa I/O in digital mode $V_{DD} \le V_{IN} \le V_{DDA}$	-	-	1	
		TTa I/O in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$	-	-	±0.2	
		FT and FTf I/O(4) $V_{DD} \le V_{IN} \le 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation.
2. Tested in production.
3. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 65: I/O current injection susceptibility*.
4. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up/pull-down resistors must be disabled.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 36* and *Figure 37* for standard I/Os.

Figure 36. TC and TTa I/O input characteristics - CMOS port

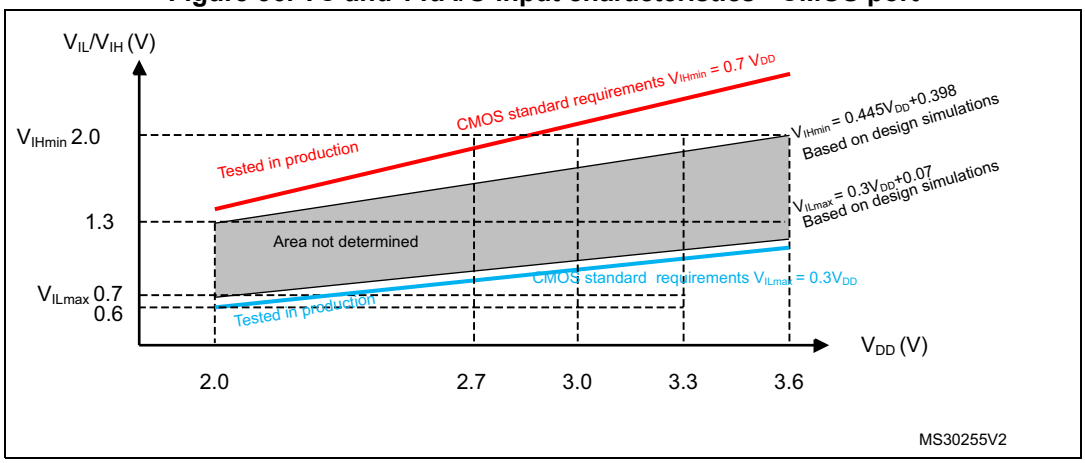


Table 88. Operational amplifier characteristics(1) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PGA gain	Non inverting gain value	-	-	2	-	-
			-	4	-	-
			-	8	-	-
			-	16	-	-
$R_{network}$	R2/R1 internal resistance values in PGA mode (3)	Gain=2	-	5.4/5.4	-	kΩ
		Gain=4	-	16.2/5.4	-	
		Gain=8	-	37.8/5.4	-	
		Gain=16	-	40.5/2.7	-	
PGA gain error	PGA gain error	-	-1%	-	1%	-
I_{bias}	OPAMP input bias current	-	-	-	±0.2(4)	µA
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, Cload = 50pF, Rload = 4 KΩ	-	4	-	MHz
		PGA Gain = 4, Cload = 50pF, Rload = 4 KΩ	-	2	-	
		PGA Gain = 8, Cload = 50pF, Rload = 4 KΩ	-	1	-	
		PGA Gain = 16, Cload = 50pF, Rload = 4 KΩ	-	0.5	-	
en	Voltage noise density	@ 1KHz, Output loaded with 4 KΩ	-	109	-	$\frac{nV}{\sqrt{Hz}}$
		@ 10KHz, Output loaded with 4 KΩ	-	43	-	

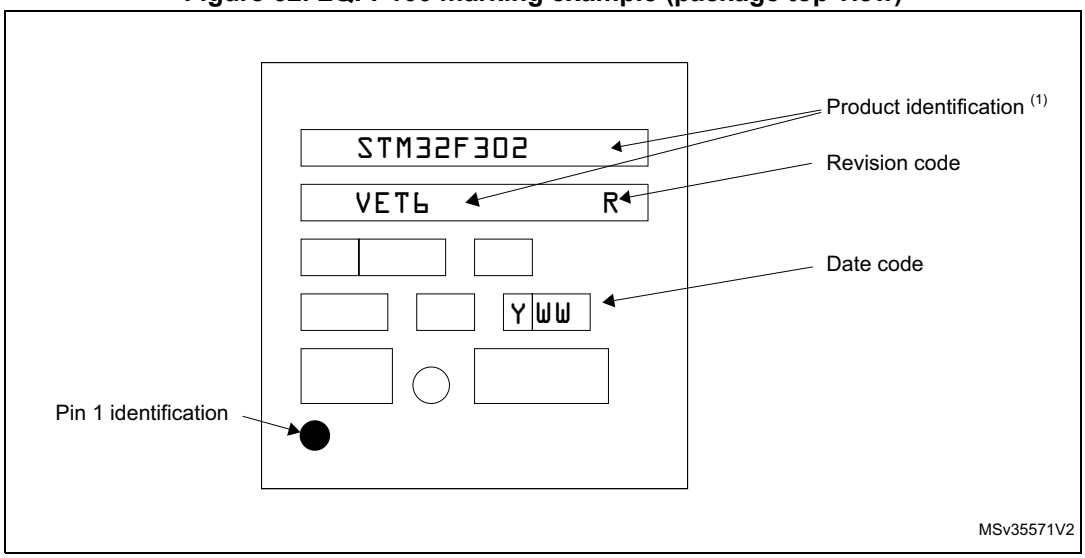
1. Guaranteed by design, not tested in production.
2. The saturation voltage can be also limited by the Iload (drive current).
3. R2 is the internal resistance between OPAMP output and OPAMP inverting input.
   R1 is the internal resistance between OPAMP inverting input and ground.
   The PGA gain =1+R2/R1
4. Mostly TTa I/O leakage, when used in analog mode.

Device marking for LQFP100

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 62. LQFP100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.