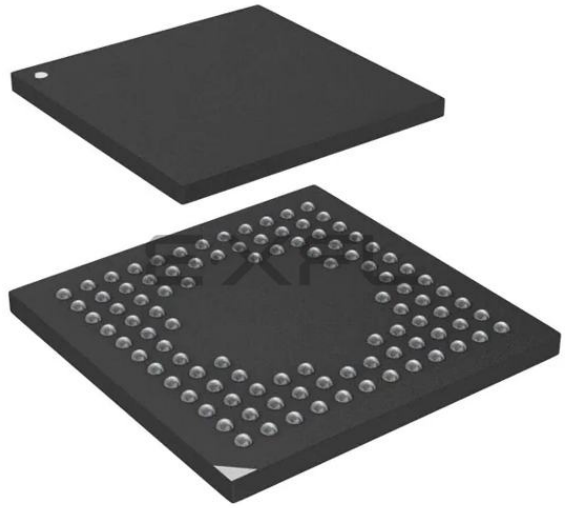

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	84
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 17x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302vdh6

List of figures

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F302xD/E microcontrollers.

This STM32F302xD/E datasheet should be read in conjunction with the reference manual of STM32F302xB/C/D/E, STM32F302x6/8 devices (RM0365) available on STMicroelectronics website at *www.st.com*.

For information on the ARM® Cortex®-M4 core with FPU, refer to the following documents:

- *Cortex® -M4 with FPU Technical Reference Manual*, available from the www.arm.com website
- *STM32F3 and STM32F4 Series Cortex® -M4 programming manual* (PM0214) available on STMicroelectronics website at *www.st.com*.

Table 2. STM32F302xD/E family device features and peripheral counts

Peripheral		STM32F302Rx		STM32F302Vx		STM32F302Zx	
Flash (Kbytes)		384	512	384	512	384	512
SRAM (Kbytes) on data bus		64					
FMC (flexible memory controller)		NO		YES			
Timers	Advanced control	1 (16-bit)					
	General purpose	5 (16-bit) 1 (32-bit)					
	Basic	1 (16-bit)					
	PWM channels (all) (1)	26					
	PWM channels (except complementary)	20					
Communication interfaces	SPI (I^2S)(2)	4(2)					
	I^2C	3					
	USART	3					
	UART	2					
	CAN	1					
	USB	1					
GPIOs	Normal I/Os (TC, TTa)	26		37 in WLCSP100,44 in LQFP100 and UFBGA100		45	
	5-volt tolerant I/Os (FT, FTf)	25		42 in LQFP100 40 in WLCSP100 and UFBGA100		70	
DMA channels		12					
Capacitive sensing channels		18		24			
12-bit ADCs		2 16 channels		2 17 channels		2 18 channels	
12-bit DAC channels		1					
Analog comparator		4					
Operational amplifiers		2					
CPU frequency		72 MHz					
Operating voltage		2.0 to 3.6 V					
Operating temperature		Ambient operating temperature: - 40 to 85 °C / - 40 to 105 °C Junction temperature: - 40 to 125 °C					
Packages		LQFP64		LQFP100 ,WLCSP100 UFBGA100		LQFP144	

1. This total number considers also the PWMs generated on the complementary output channels.
2. The SPI interfaces works in an exclusive way in either the SPI mode or the I^2S audio mode.

Table 13. STM32F302xD/E pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP100	LQFP144						
21	30	H7	41	PA5	I/O	TTa	(5)	TIM2_CH1/TIM2_ETR, TSC_G2_IO2, SPI1_SCK, EVENTOUT	ADC2_IN2(3), COMP1_INM, COMP2_INM, COMP4_INM, COMP6_INM, OPAMP1_VINP, OPAMP2_VINM,
22	31	H6	42	PA6	I/O	TTa	(5)	TIM16_CH1, TIM3_CH1, TSC_G2_IO3, SPI1_MISO, TIM1_BKIN, COMP1_OUT, EVENTOUT	ADC2_IN3(3), OPAMP2_VOUT
23	32	K7	43	PA7	I/O	TTa	-	TIM17_CH1, TIM3_CH2, TSC_G2_IO4, SPI1_MOSI, TIM1_CH1N, EVENTOUT	ADC2_IN4(3), COMP2_INP, OPAMP1_VINP, OPAMP2_VINP
24	33	G6	44	PC4	I/O	TTa	-	EVENTOUT, TIM1_ETR, USART1_TX	ADC2_IN5(3)
25	34	F6	45	PC5	I/O	TTa	-	EVENTOUT, TIM15_BKIN, TSC_G3_IO1, USART1_RX	ADC2_IN11, OPAMP1_VINM, OPAMP2_VINM
26	35	J6	46	PB0	I/O	TTa	-	TIM3_CH3, TSC_G3_IO2, TIM1_CH2N, EVENTOUT	COMP4_INP, OPAMP2_VINP,
27	36	K6	47	PB1	I/O	TTa	(5)	TIM3_CH4, TSC_G3_IO3, TIM1_CH3N, COMP4_OUT, EVENTOUT	-
28	37	K5	48	PB2	I/O	TTa	-	TSC_G3_IO4, EVENTOUT	ADC2_IN12, COMP4_INM
-	-	-	49	PF11	I/O	FT	(1)	EVENTOUT	-
-	-	-	50	PF12	I/O	FT	(1)	EVENTOUT, FMC_A6	-
-	-	-	51	VSS	S	-	-	-	-
-	-	-	52	VDD	S	-	(1)	-	-
-	-	-	53	PF13	I/O	FT	(1)	EVENTOUT, FMC_A7	-
-	-	-	54	PF14	I/O	FT	(1)	EVENTOUT, FMC_A8	-
-	-	-	55	PF15	I/O	FT	(1)	EVENTOUT, FMC_A9	-
-	-	-	56	PG0	I/O	FT	(1)	EVENTOUT, FMC_A10	-
-	-	-	57	PG1	I/O	FT	(1)	EVENTOUT, FMC_A11	-

Table 13. STM32F302xD/E pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP100	LQFP144						
34	52	J3	74	PB13	I/O	TTa	-	TSC_G6_IO3, SPI2_SCK/I2S2_CK, TIM1_CH1N, USART3_CTS, EVENTOUT	-
35	53	J2	75	PB14	I/O	TTa	-	TIM15_CH1, TSC_G6_IO4, SPI2_MISO/I2S2ext_SD, TIM1_CH2N, USART3_RTS, EVENTOUT	OPAMP2_VINP
36	54	H4	76	PB15	I/O	TTa	-	RTC_REFIN, TIM15_CH2, TIM15_CH1N, TIM1_CH3N, SPI2_MOSI/I2S2_SD, EVENTOUT	COMP6_INM
-	55	-	77	PD8	I/O	TTa	(1)	EVENTOUT, USART3_TX, FMC_D13	-
-	56	G4	78	PD9	I/O	TTa	(1)	EVENTOUT, USART3_RX, FMC_D14	-
-	57	H3	79	PD10	I/O	TTa	(1)	EVENTOUT, USART3_CK, FMC_D15	COMP6_INM
-	58	H2	80	PD11	I/O	TTa	(1)	EVENTOUT, USART3_CTS, FMC_A16	-
-	59	H1	81	PD12	I/O	TTa	(1)	EVENTOUT, TIM4_CH1, TSC_G8_IO1, USART3_RTS, FMC_A17	-
-	60	G3	82	PD13	I/O	TTa	(1)	EVENTOUT, TIM4_CH2, TSC_G8_IO2, FMC_A18	-
-	-	-	83	VSS	S	-	(1)	-	-
-	-	-	84	VDD	S	-	(1)	-	-
-	61	G2	85	PD14	I/O	TTa	(1)	EVENTOUT, TIM4_CH3, TSC_G8_IO3, FMC_D0	OPAMP2_VINP
-	62	G1	86	PD15	I/O	TTa	(1)	EVENTOUT, TIM4_CH4, TSC_G8_IO4, SPI2_NSS, FMC_D1	-
-	-	-	87	PG2	I/O	FT	(1)	EVENTOUT, FMC_A12	-
-	-	-	88	PG3	I/O	FT	(1)	EVENTOUT, FMC_A13	-
-	-	-	89	PG4	I/O	FT	(1)	EVENTOUT, FMC_A14	-

Table 14. STM32F302xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3//15/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port E	PE0	-	EVENT OUT	TIM4_ETR	-	TIM16_CH1	-	-	USART1_TX	-	-	-	-	FMC_NBL0	-	-	-
	PE1	-	EVENT OUT	-	-	TIM17_CH1	-	-	USART1_RX	-	-	-	-	FMC_NBL1	-	-	-
	PE2	TRACECK	EVENT OUT	TIM3_CH1	TSC_G7_IO1	-	SPI4_SCK	-	-	-	-	-	-	FMC_A23	-	-	-
	PE3	TRACED0	EVENT OUT	TIM3_CH2	TSC_G7_IO2	-	SPI4_NSS	-	-	-	-	-	-	FMC_A19	-	-	-
	PE4	TRACED1	EVENT OUT	TIM3_CH3	TSC_G7_IO3	-	SPI4_NSS	-	-	-	-	-	-	FMC_A20	-	-	-
	PE5	TRACED2	EVENT OUT	TIM3_CH4	TSC_G7_IO4	-	SPI4_MISO	-	-	-	-	-	-	FMC_A21	-	-	-
	PE6	TRACED3	EVENT OUT	-	-	-	SPI4_MOSI	-	-	-	-	-	-	FMC_A22	-	-	-
	PE7	-	EVENT OUT	TIM1_ETR	-	-	-	-	-	-	-	-	-	FMC_D4	-	-	-
	PE8	-	EVENT OUT	TIM1_CH1N	-	-	-	-	-	-	-	-	-	FMC_D5	-	-	-
	PE9	-	EVENT OUT	TIM1_CH1	-	-	-	-	-	-	-	-	-	FMC_D6	-	-	-
	PE10	-	EVENT OUT	TIM1_CH2N	-	-	-	-	-	-	-	-	-	FMC_D7	-	-	-
	PE11	-	EVENT OUT	TIM1_CH2	-	-	SPI4_NSS	-	-	-	-	-	-	FMC_D8	-	-	-

Table 32. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DD} = 3.3 V C_{ext} = 0 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.90	mA
			4 MHz	0.93	
			8 MHz	1.16	
			18 MHz	1.60	
			36 MHz	2.51	
			48 MHz	2.97	
		V_{DD} = 3.3 V C_{ext} = 10 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.93	
			4 MHz	1.06	
			8 MHz	1.47	
			18 MHz	2.26	
			36 MHz	3.39	
			48 MHz	5.99	
		V_{DD} = 3.3 V C_{ext} = 22 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.03	
			4 MHz	1.30	
			8 MHz	1.79	
			18 MHz	3.01	
			36 MHz	5.99	
		V_{DD} = 3.3 V C_{ext} = 33 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.10	
			4 MHz	1.31	
			8 MHz	2.06	
			18 MHz	3.47	
			36 MHz	8.35	
		V_{DD} = 3.3 V C_{ext} = 47 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.20	
			4 MHz	1.54	
			8 MHz	2.46	
			18 MHz	4.51	
			36 MHz	9.98	

1. CS = 5 pF (estimated value).

Asynchronous waveforms and timings

Figure 20 to *Figure 23* represent asynchronous waveforms and *Table 45* to *Table 52* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- NOR NWAIT pulse width= 1THCLK

In all the timing tables, the T_{HCLK} is the HCLK clock period.

Figure 20. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings

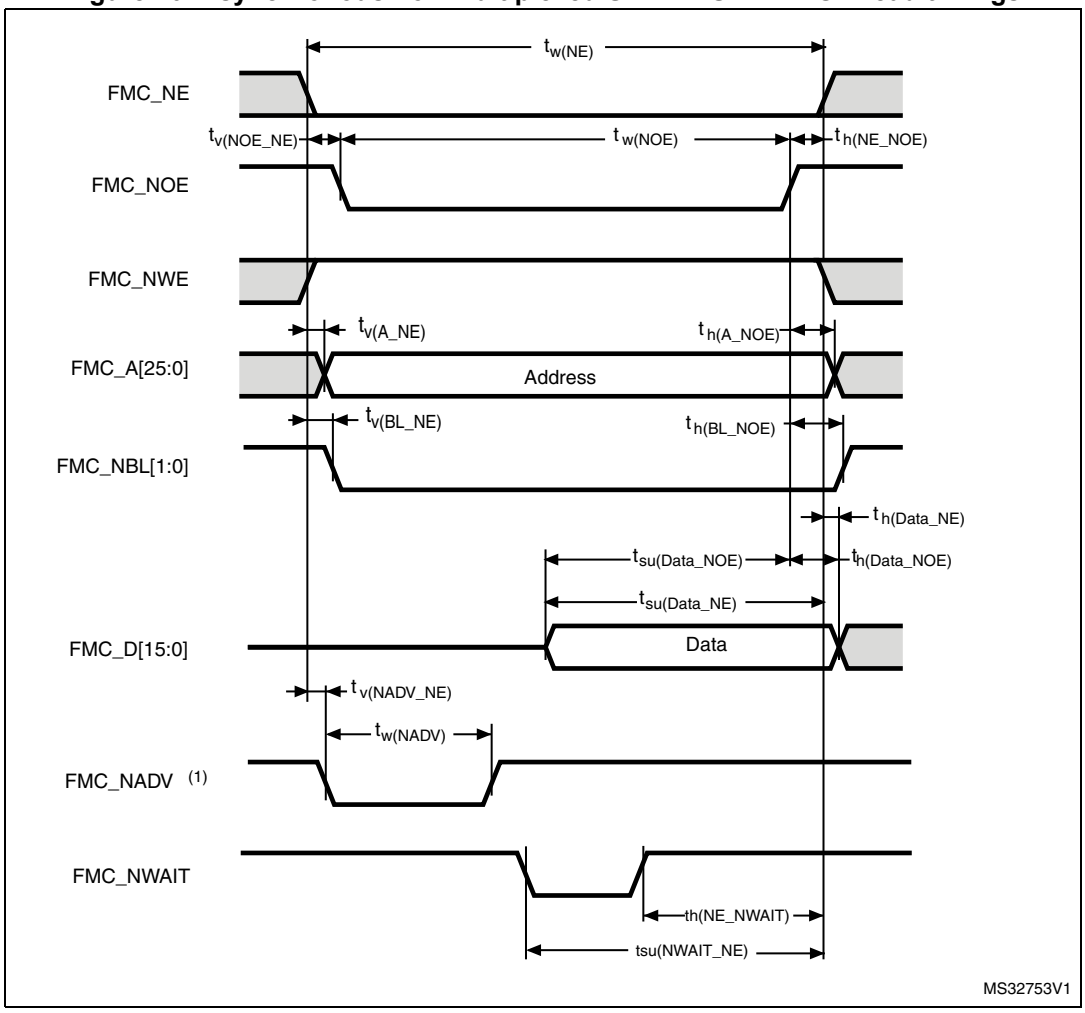


Figure 26. Synchronous non-multiplexed NOR/PSRAM read timings

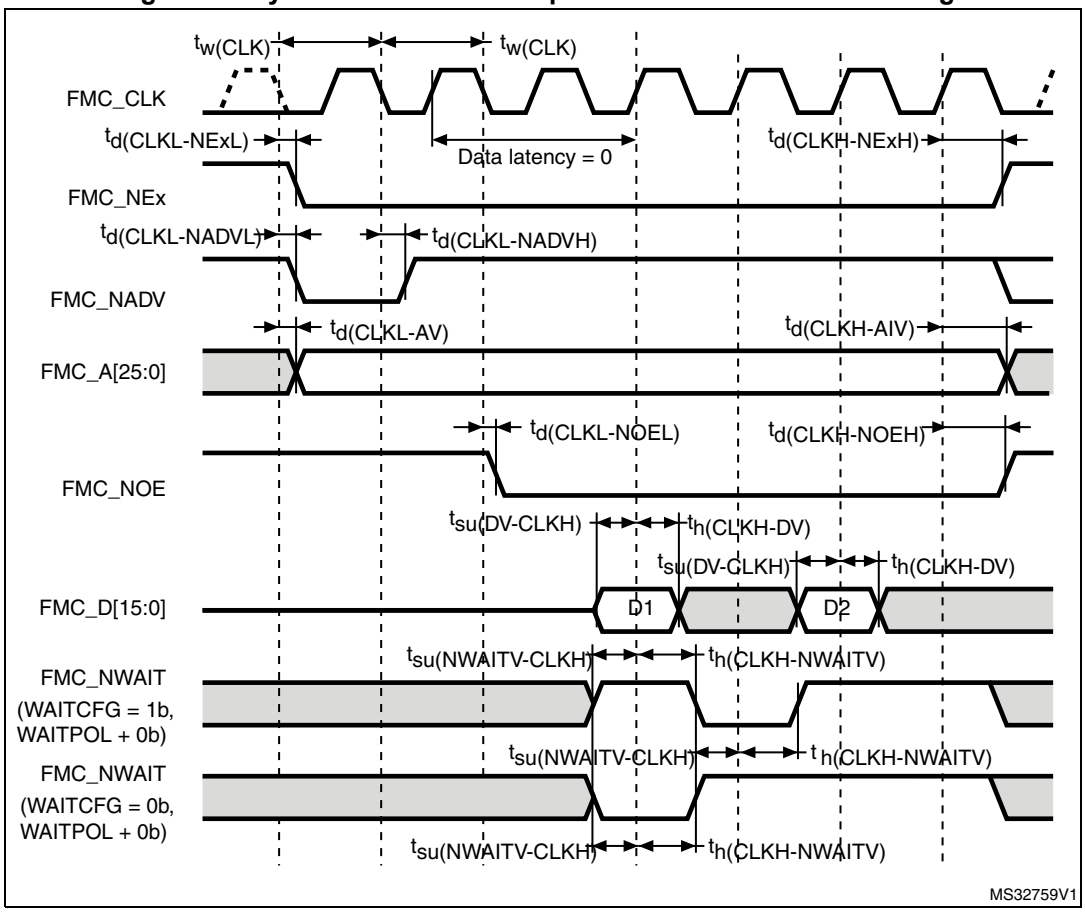


Table 55. Synchronous non-multiplexed NOR/PSRAM read timings(1)

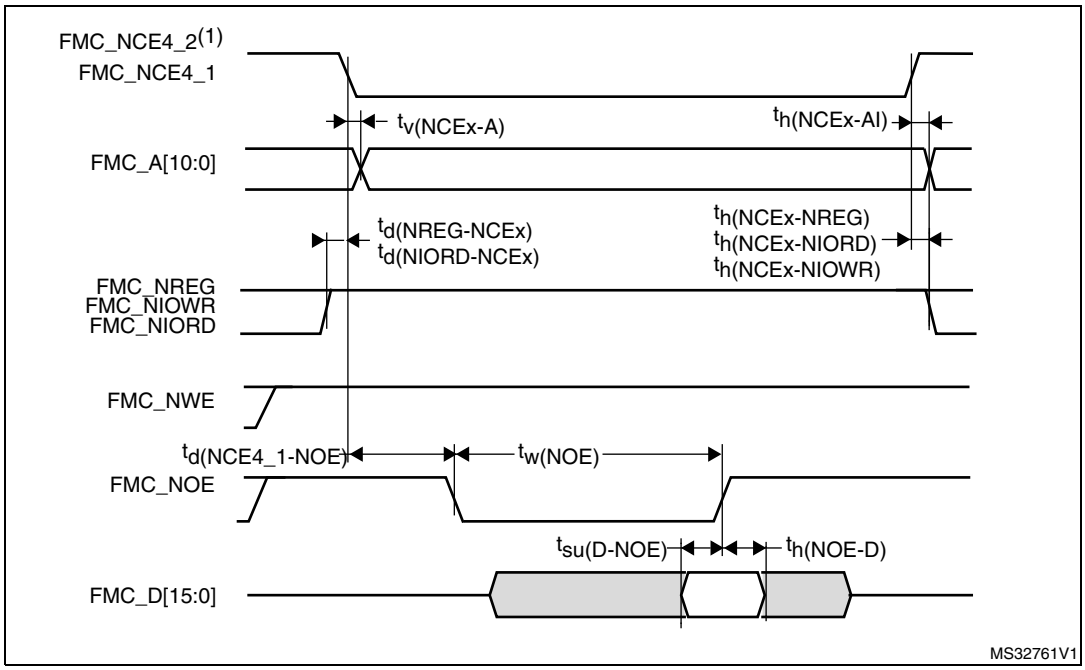
Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	2THCLK-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	THCLK+1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	7	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	7	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	THCLK	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	6	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	THCLK+1	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	3.5	-	

Table 57. Switching characteristics for PC Card/CF read and write cycles in attribute/common space(1)

Symbol	Parameter	Min	Max	Unit
$t_{v(NCEx-A)}$	FMC_Ncex low to FMC_Ay valid	-	0	ns
$t_{h(NCEx\_AI)}$	FMC_NCEx high to FMC_Ax invalid	2.5	-	
$t_{d(NREG-NCEx)}$	FMC_NCEx low to FMC_NREG valid	-	2	
$t_{h(NCEx-NREG)}$	FMC_NCEx high to FMC_NREG invalid	0	-	
$t_{d(NCEx-NWE)}$	FMC_NCEx low to FMC_NWE low	-	5THCLK+2	
$t_{w(NWE)}$	FMC_NWE low width	8THCLK	8THCLK+0.5	
$t_{d(NWE\_NCEx)}$	FMC_NWE high to FMC_NCEx high	5THCLK-1	-	
$t_{v\ (NWE-D)}$	FMC_NWE low to FMC_D[15:0] valid	-	5	
$t_{h\ (NWE-D)}$	FMC_NWE high to FMC_D[15:0] invalid	4THCLK-1	-	
$t_{d\ (D-NWE)}$	FMC_D[15:0] valid before FMC_NWE high	13THCLK-3	-	
$t_{d(NCEx-NOE)}$	FMC_NCEx low to FMC_NOE low	-	5THCLK+2	
$t_{w(NOE)}$	FMC_NOE low width	8THCLK-1	8THCLK+2	
$t_{d(NOE\_NCEx)}$	FMC_NOE high to FMC_NCEx high	5THCLK-1	-	
$t_{su\ (D-NOE)}$	FMC_D[15:0] valid data before FMC_NOE high	THCLK+2	-	
$t_{h(NOE-D)}$	FMC_N0E high to FMC_D[15:0] invalid	0	-	

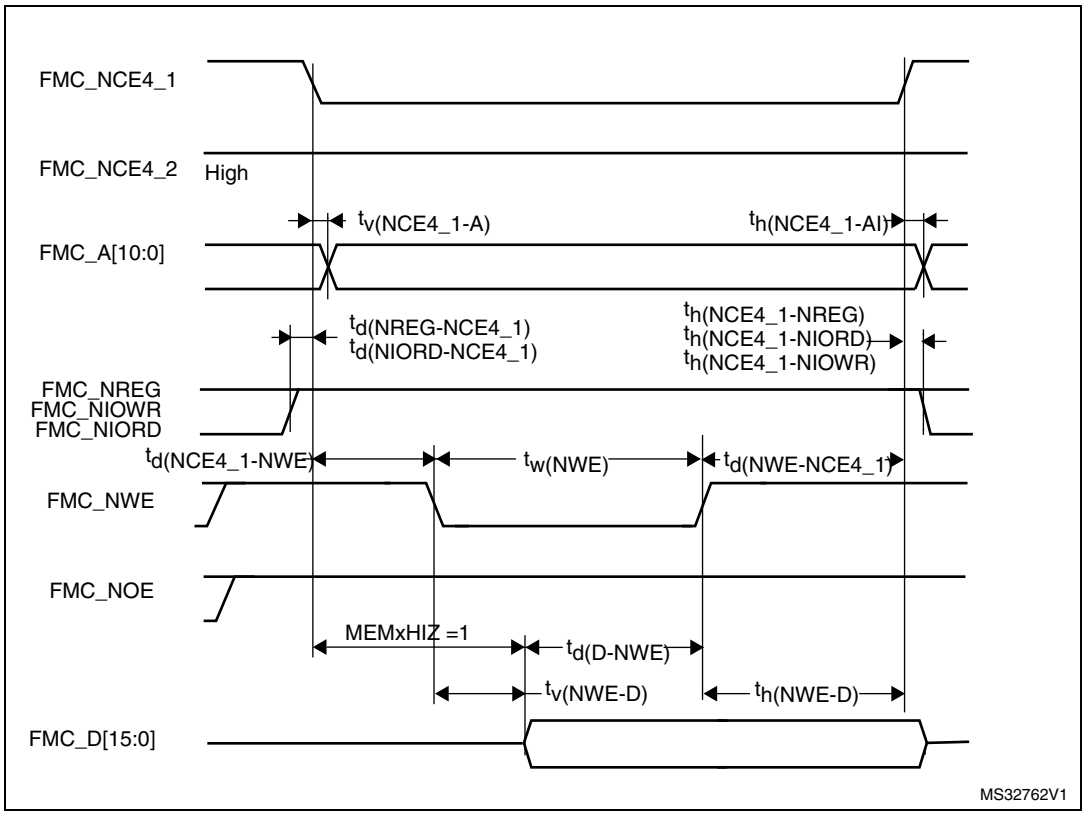
1. Based on characterization, not tested in production.

Figure 28. PC Card/CompactFlash controller waveforms for common memory read access



1. FMC_NCE4_2 remains high (inactive during 8-bit access.

Figure 29. PC Card/CompactFlash controller waveforms for common memory write access



Pre qualification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 62. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP144 package compliant with IEC 61967-2	0.1 to 30 MHz	7	dBµV
			30 to 130 MHz	15	
			130 MHz to 1GHz	31	
			SAE EMI Level	4	-

6.3.13 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 63. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	C3	250	

1. Data based on characterization results, not tested in production.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 17*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 17*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 67* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 19*. All I/Os (FT, TTa and TC unless otherwise specified) are CMOS and TTL compliant.

Table 67. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +48 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH} (3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH}(3)(4)	Output high level voltage for an I/O pin		V_{DD}–1.3	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	
V_{OH}(3)(4)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OLFM+}(4)(4)	Output low level voltage for an FTf I/O pin in FM+ mode	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 17* and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 17* and the sum of I_{IO} (I/O ports and control pins) must not exceed $\Sigma I_{IO(PIN)}$.
4. Data based on design simulation.

Table 78. USB: full-speed electrical characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	-	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	-	2.0	V
Output driver Impedance(3)	Z_{DRV}	driving high and low	28	40	44	Ω

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed information, refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-), the matching impedance is already included in the embedded driver.

CAN (controller area network) interface

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

6.3.19 ADC characteristics

Unless otherwise specified, the parameters given in *Table 79* to *Table 82* are guaranteed by design, with conditions summarized in *Table 19*.

Table 79. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC	-	2.0	-	3.6	V
I_{DDA}	Current on VDDA pin (see *Figure 48*)	Single-ended mode, 5 MSPS	-	907	1033	µA
		Single-ended mode, 1 MSPS	-	194	285.5	
		Single-ended mode, 200 KSPS	-	51.5	70	
		Differential mode, 5 MSPS	-	887.5	1009	
		Differential mode, 1 MSPS	-	212	285	
		Differential mode, 200 KSPS	-	51	69.5	

Table 84. ADC accuracy, 64-pin packages(1)(2)(3) (continued)

Symbol	Parameter	Conditions			Min(4)	Max (4)	Unit
EL	Integral linearity error	ADC clock freq. ≤ 72 MHz, Sampling freq ≤ 5 Msps, 2.0 V ≤ V_{DDA} ≤ 3.6 V 64-pin package	Single ended	Fast channel 5.1 Ms	-	±3	LSB
				Slow channel 4.8 Ms	-	±3.5	
			Differential	Fast channel 5.1 Ms	-	±2	
				Slow channel 4.8 Ms	-	±2.5	
ENOB (5)	Effective number of bits		Single ended	Fast channel 5.1 Ms	10.4	-	bits
				Slow channel 4.8 Ms	10.4	-	
			Differential	Fast channel 5.1 Ms	10.8	-	
				Slow channel 4.8 Ms	10.8	-	
SINAD (5)	Signal-to-noise and distortion ratio		Single ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	63	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
SNR(5)	Signal-to-noise ratio		Single ended	Fast channel 5.1 Ms	64	-	dB
				Slow channel 4.8 Ms	64	-	
			Differential	Fast channel 5.1 Ms	67	-	
				Slow channel 4.8 Ms	67	-	
THD(5)	Total harmonic distortion		Single ended	Fast channel 5.1 Ms	-	-75	
				Slow channel 4.8 Ms	-	-75	
			Differential	Fast channel 5.1 Ms	-	-79	
				Slow channel 4.8 Ms	-	-78	

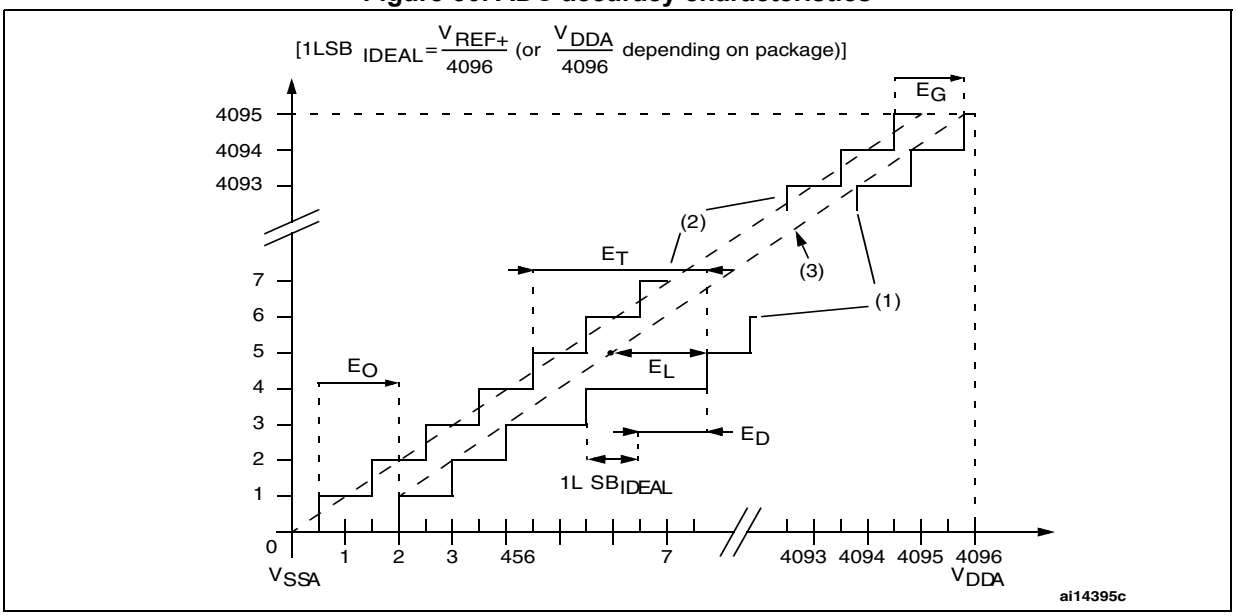
1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.15* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.
5. Value measured with a -0.5 dB full scale 50 kHz sine wave input signal.

Table 85. ADC accuracy at 1MSPS(1)(2)

Symbol	Parameter	Test conditions		Typ	Max(3)	Unit
ET	Total unadjusted error	ADC Freq ≤ 72 MHz Sampling Freq ≤ 1MSPS 2.4 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V Single-ended mode	Fast channel	±2.5	±5	LSB
			Slow channel	±3.5	±5	
EO	Offset error		Fast channel	±1	±2.5	
			Slow channel	±1.5	±2.5	
EG	Gain error		Fast channel	±2	±3	
			Slow channel	±3	±4	
ED	Differential linearity error		Fast channel	±0.7	±2	
			Slow channel	±0.7	±2	
EL	Integral linearity error		Fast channel	±1	±3	
			Slow channel	±1.2	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current. Any positive injection current within the limits specified for IINJ(PIN) and ∑IINJ(PIN) in *Section 6.3.15: I/O port characteristics* does not affect the ADC accuracy.
3. Data based on characterization results, not tested in production.

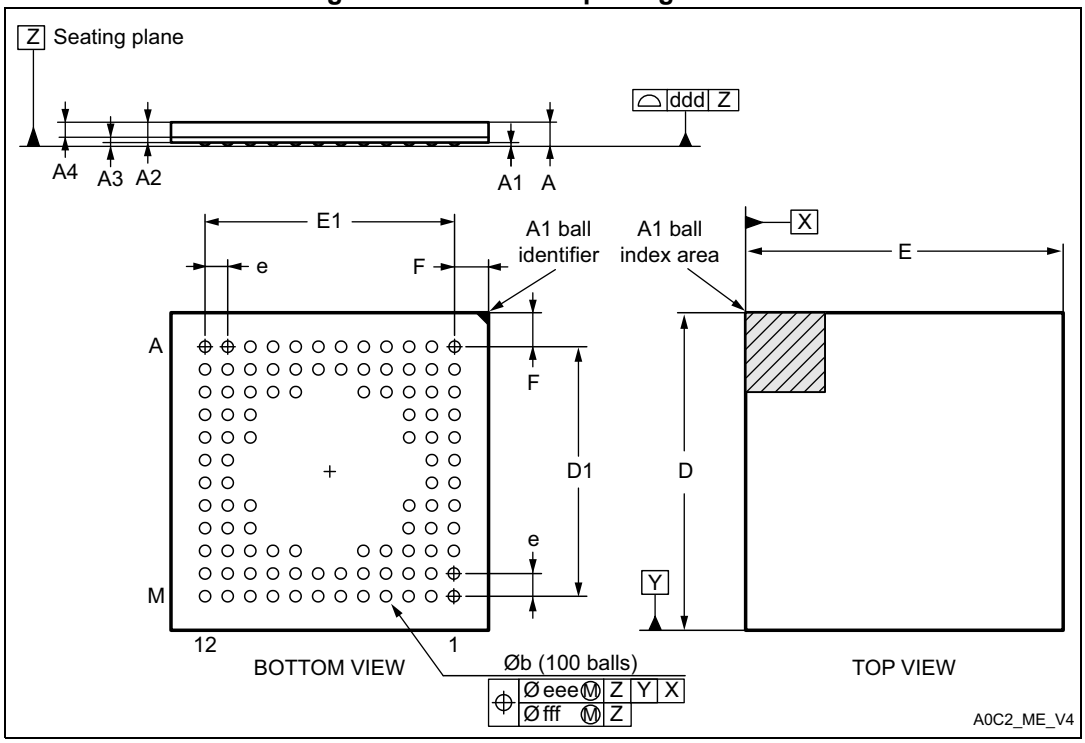
Figure 50. ADC accuracy characteristics



7.3 UFBGA100 package information

UFBGA100 is a 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package.

Figure 57. UFBGA100 package outline



1. Drawing is not to scale.

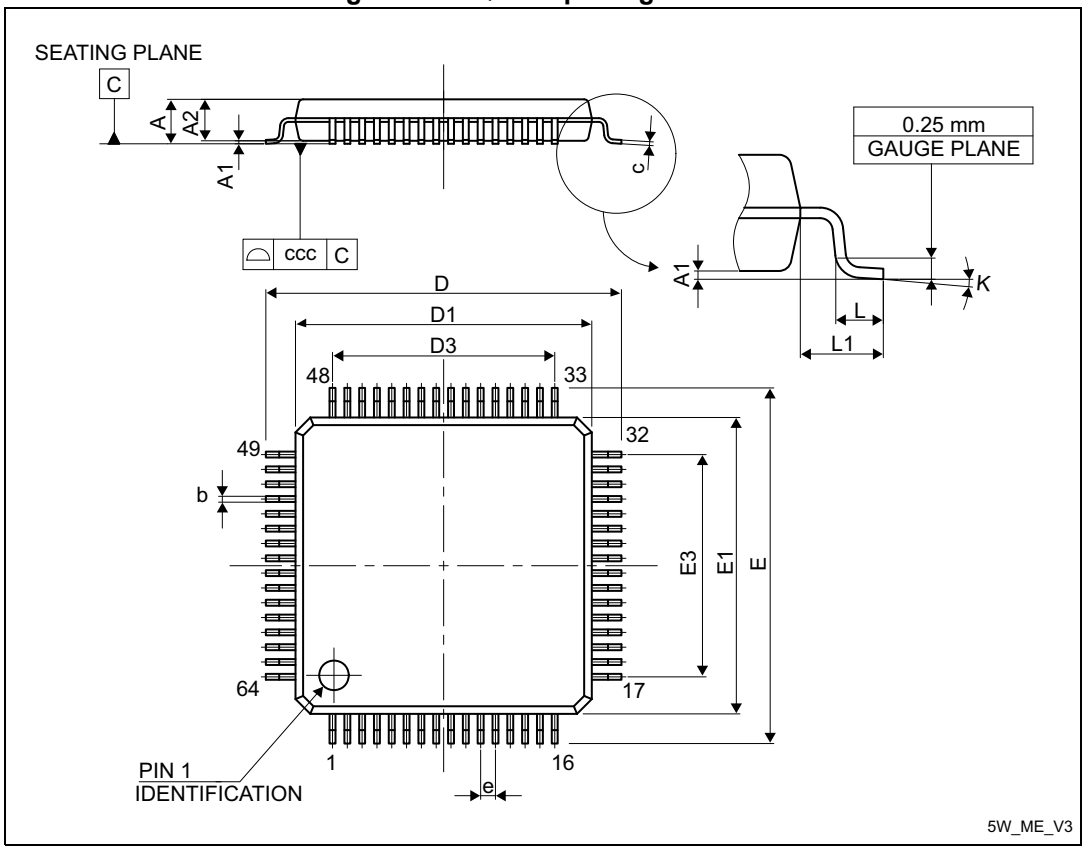
Table 93. UFBGA100 package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.450	5.500	5.550	0.2146	0.2165	0.2185
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.450	5.500	5.550	0.2146	0.2165	0.2185
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315

7.6 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.

Figure 66. LQFP64 package outline



1. Drawing is not to scale.

Table 98. LQFP64 package mechanical data

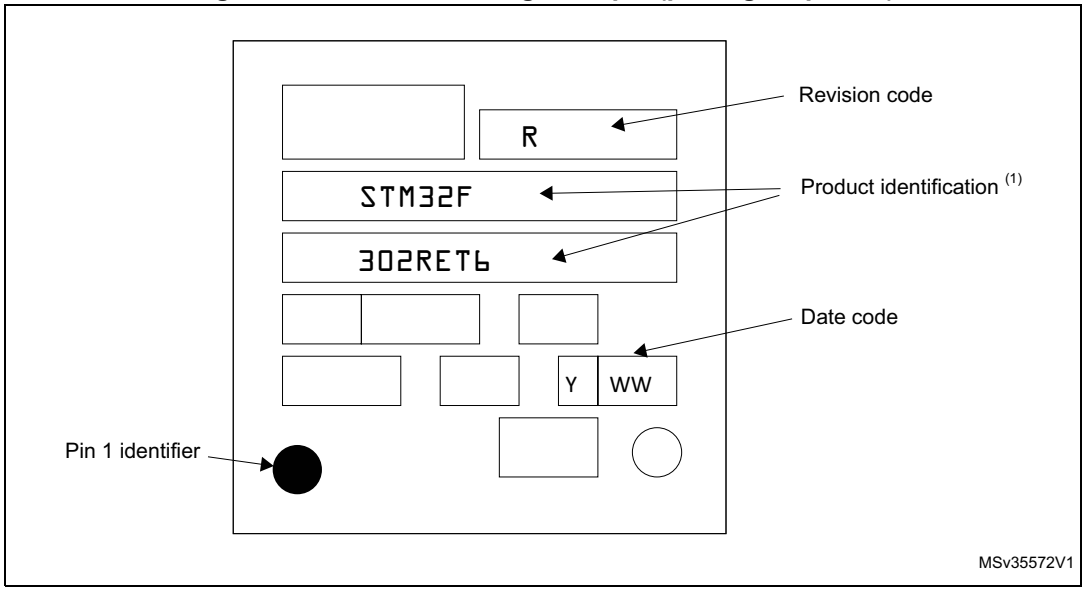
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Device marking for LQFP64

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 68. LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.