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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	86
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 17x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302vdt6tr

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F302xD/E microcontrollers.

This STM32F302xD/E datasheet should be read in conjunction with the reference manual of STM32F302xB/C/D/E, STM32F302x6/8 devices (RM0365) available on STMicroelectronics website at *www.st.com*.

For information on the ARM® Cortex®-M4 core with FPU, refer to the following documents:

- *Cortex® -M4 with FPU Technical Reference Manual*, available from the www.arm.com website
- *STM32F3 and STM32F4 Series Cortex® -M4 programming manual* (PM0214) available on STMicroelectronics website at *www.st.com*.

- External triggers for conversion
- Input voltage reference VREF+

3.16 Operational amplifier (OPAMP)

The STM32F302xD/E embed two operational amplifiers (OPAMP1 and OPAMP2) with external or internal follower routing and PGA capability (or even amplifier and filter capability with external components). When an operational amplifier is selected, an external ADC channel is used to enable output measurement.

The operational amplifier features:

- 8.2 MHz bandwidth
- 0.5 mA output capability
- Rail-to-rail input/output
- In PGA mode, the gain is programmed to be 2, 4, 8 or 16.

3.17 Ultra-fast comparators (COMP)

The STM32F302xD/E devices embed four ultra-fast rail-to-rail comparators (COMP1, 2, 4, 6) with programmable reference voltage (internal or external) and selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pin
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to *Table 23: Embedded internal reference voltage* for the value and precision of the internal reference voltage.

All comparators can wake up from STOP mode, generate interrupts and breaks for the timers.

3.18 Timers and watchdogs

The STM32F302xD/E include one advanced control timer, up to six general-purpose timers, one basic timer, two watchdog timers and one SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced	TIM1	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	Yes
General-purpose	TIM2	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No

Table 5. Timer feature comparison (continued)

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
General-purpose	TIM3, TIM4	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Note: TIM1/2/3/4/15/16/17 can have PLL as clock source, and therefore can be clocked at 144 MHz.

3.18.1 Advanced timers (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIM timer (described in *Section 3.18.2*) using the same architecture, so the advanced-control timers can work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

3.18.2 General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16, TIM17)

There are up to six synchronizable general-purpose timers embedded in the STM32F302xD/E (see *Table 5* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

4 Pinout and pin description

Figure 4. STM32F302xD/E LQFP64 pinout

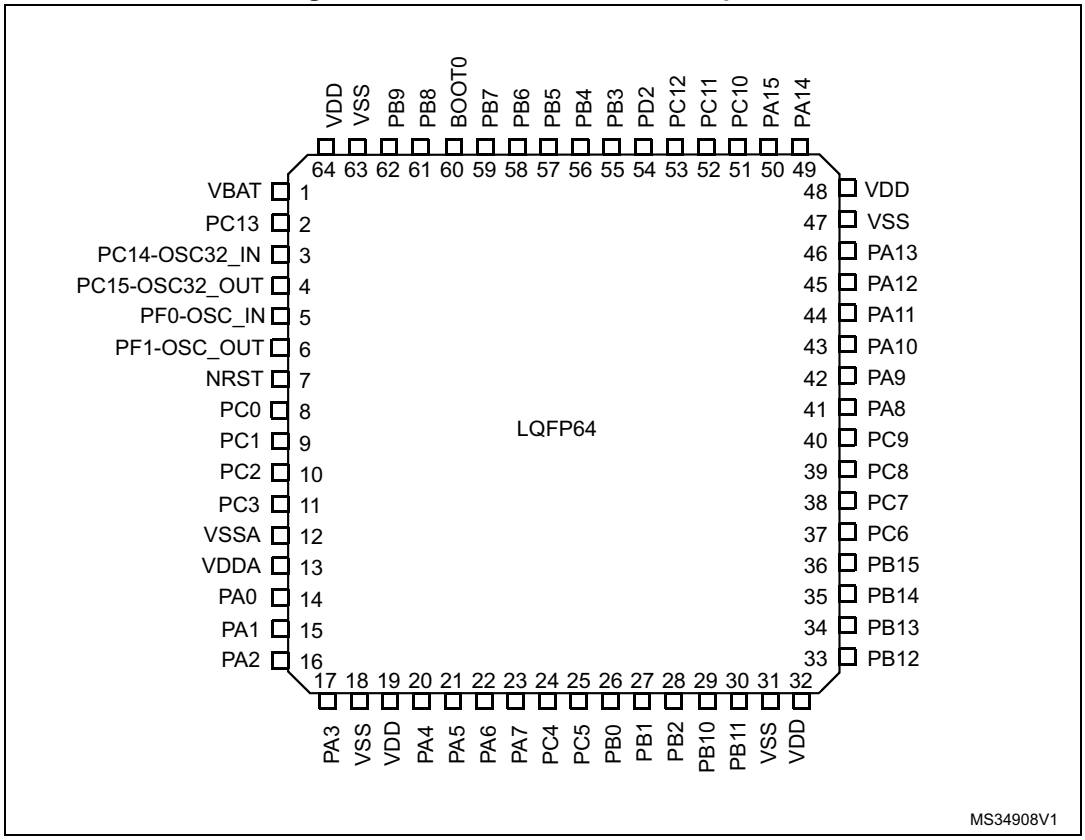


Table 13. STM32F302xD/E pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP100	LQFP144						
21	30	H7	41	PA5	I/O	TTa	(5)	TIM2_CH1/TIM2_ETR, TSC_G2_IO2, SPI1_SCK, EVENTOUT	ADC2_IN2(3), COMP1_INM, COMP2_INM, COMP4_INM, COMP6_INM, OPAMP1_VINP, OPAMP2_VINM,
22	31	H6	42	PA6	I/O	TTa	(5)	TIM16_CH1, TIM3_CH1, TSC_G2_IO3, SPI1_MISO, TIM1_BKIN, COMP1_OUT, EVENTOUT	ADC2_IN3(3), OPAMP2_VOUT
23	32	K7	43	PA7	I/O	TTa	-	TIM17_CH1, TIM3_CH2, TSC_G2_IO4, SPI1_MOSI, TIM1_CH1N, EVENTOUT	ADC2_IN4(3), COMP2_INP, OPAMP1_VINP, OPAMP2_VINP
24	33	G6	44	PC4	I/O	TTa	-	EVENTOUT, TIM1_ETR, USART1_TX	ADC2_IN5(3)
25	34	F6	45	PC5	I/O	TTa	-	EVENTOUT, TIM15_BKIN, TSC_G3_IO1, USART1_RX	ADC2_IN11, OPAMP1_VINM, OPAMP2_VINM
26	35	J6	46	PB0	I/O	TTa	-	TIM3_CH3, TSC_G3_IO2, TIM1_CH2N, EVENTOUT	COMP4_INP, OPAMP2_VINP,
27	36	K6	47	PB1	I/O	TTa	(5)	TIM3_CH4, TSC_G3_IO3, TIM1_CH3N, COMP4_OUT, EVENTOUT	-
28	37	K5	48	PB2	I/O	TTa	-	TSC_G3_IO4, EVENTOUT	ADC2_IN12, COMP4_INM
-	-	-	49	PF11	I/O	FT	(1)	EVENTOUT	-
-	-	-	50	PF12	I/O	FT	(1)	EVENTOUT, FMC_A6	-
-	-	-	51	VSS	S	-	-	-	-
-	-	-	52	VDD	S	-	(1)	-	-
-	-	-	53	PF13	I/O	FT	(1)	EVENTOUT, FMC_A7	-
-	-	-	54	PF14	I/O	FT	(1)	EVENTOUT, FMC_A8	-
-	-	-	55	PF15	I/O	FT	(1)	EVENTOUT, FMC_A9	-
-	-	-	56	PG0	I/O	FT	(1)	EVENTOUT, FMC_A10	-
-	-	-	57	PG1	I/O	FT	(1)	EVENTOUT, FMC_A11	-

Table 13. STM32F302xD/E pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP100	LQFP144						
34	52	J3	74	PB13	I/O	TTa	-	TSC_G6_IO3, SPI2_SCK/I2S2_CK, TIM1_CH1N, USART3_CTS, EVENTOUT	-
35	53	J2	75	PB14	I/O	TTa	-	TIM15_CH1, TSC_G6_IO4, SPI2_MISO/I2S2ext_SD, TIM1_CH2N, USART3_RTS, EVENTOUT	OPAMP2_VINP
36	54	H4	76	PB15	I/O	TTa	-	RTC_REFIN, TIM15_CH2, TIM15_CH1N, TIM1_CH3N, SPI2_MOSI/I2S2_SD, EVENTOUT	COMP6_INM
-	55	-	77	PD8	I/O	TTa	(1)	EVENTOUT, USART3_TX, FMC_D13	-
-	56	G4	78	PD9	I/O	TTa	(1)	EVENTOUT, USART3_RX, FMC_D14	-
-	57	H3	79	PD10	I/O	TTa	(1)	EVENTOUT, USART3_CK, FMC_D15	COMP6_INM
-	58	H2	80	PD11	I/O	TTa	(1)	EVENTOUT, USART3_CTS, FMC_A16	-
-	59	H1	81	PD12	I/O	TTa	(1)	EVENTOUT, TIM4_CH1, TSC_G8_IO1, USART3_RTS, FMC_A17	-
-	60	G3	82	PD13	I/O	TTa	(1)	EVENTOUT, TIM4_CH2, TSC_G8_IO2, FMC_A18	-
-	-	-	83	VSS	S	-	(1)	-	-
-	-	-	84	VDD	S	-	(1)	-	-
-	61	G2	85	PD14	I/O	TTa	(1)	EVENTOUT, TIM4_CH3, TSC_G8_IO3, FMC_D0	OPAMP2_VINP
-	62	G1	86	PD15	I/O	TTa	(1)	EVENTOUT, TIM4_CH4, TSC_G8_IO4, SPI2_NSS, FMC_D1	-
-	-	-	87	PG2	I/O	FT	(1)	EVENTOUT, FMC_A12	-
-	-	-	88	PG3	I/O	FT	(1)	EVENTOUT, FMC_A13	-
-	-	-	89	PG4	I/O	FT	(1)	EVENTOUT, FMC_A14	-

Table 14. STM32F302xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM12/3/4/8/20/15/GPCOMP1	I2C3//15/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port C	PC10	-	EVENT OUT	-	-	-	UART4_TX	SPI3_SCK/I2S3_CK	USART3_TX	-	-	-	-	-	-	-	-
	PC11	-	EVENT OUT	-	-	-	UART4_RX	SPI3_MISO/I2S3ext_SD	USART3_RX	-	-	-	-	-	-	-	-
	PC12	-	EVENT OUT	-	-	-	UART5_TX	SPI3_MOSI/I2S3_SD	USART3_CK	-	-	-	-	-	-	-	-
	PC13	-	EVENT OUT	-	-	TIM1_CH1N	-	-	-	-	-	-	-	-	-	-	-
	PC14	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC15	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Port D	PD0	-	EVENT OUT	-	-	-	-	-	CAN_RX	-	-	-	-	FMC_D2	-	-	-
	PD1	-	EVENT OUT	-	-	-		-	CAN_TX	-	-	-	-	FMC_D3	-	-	-
	PD2	-	EVENT OUT	TIM3_ETR	-	-	UART5_RX	-	-	-	-	-	-	-	-	-	-
	PD3	-	EVENT OUT	TIM2_CH1/TIM2_ETR	-	-	-	-	USART2_CTS	-	-	-	-	FMC_CLK	-	-	-
	PD4	-	EVENT OUT	TIM2_CH2	-	-	-	-	USART2_RTS	-	-	-	-	FMC_NOE	-	-	-

Table 14. STM32F302xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3//15/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port E	PE12	-	EVENT OUT	TIM1_CH3N	-	-	SPI4_SCK	-	-	-	-	-	-	FMC_D9	-	-	-
	PE13	-	EVENT OUT	TIM1_CH3	-	-	SPI4_MISO	-	-	-	-	-	-	FMC_D10	-	-	-
	PE14	-	EVENT OUT	TIM1_CH4	-	-	SPI4_MOSI	TIM1_BKIN2	-	-	-	-	-	FMC_D11	-	-	-
	PE15	-	EVENT OUT	TIM1_BKIN	-	-	-	-	USART3_RX	-	-	-	-	FMC_D12	-	-	-
Port F	PF0	-	EVENT OUT	-	-	I2C2_SDA	SPI2_NSS/I2S2_WS	TIM1_CH3N	-	-	-	-	-	-	-	-	-
	PF1	-	EVENT OUT	-	-	I2C2_SCL	SPI2_SCK/I2S2_CK	-	-	-	-	-	-	-	-	-	-
	PF2	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A2	-	-	-
	PF3	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A3	-	-	-
	PF4	-	EVENT OUT	COMP1_OUT	-	-	-	-	-	-	-	-	-	FMC_A4	-	-	-
	PF5	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	-
	PF6	-	EVENT OUT	TIM4_CH4	-	I2C2_SCL	-	-	USART3_RTS	-	-	-	-	FMC_NIORD	-	-	-
	PF7	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NREG	-	-	-

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Note: The total current consumption is the sum of I_{DD} and I_{DDA}.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz,1 wait state from 24 to 48 MHz and 2 wait states from 48 to 72 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK2} = f_{HCLK}$ and $f_{PCLK1} = f_{HCLK/2}$
- When f_{HCLK} > 8 MHz, the PLL is ON and the PLL input is equal to HSI/2 (4 MHz) or HSE (8 MHz) in bypass mode.

The parameters given in *Table 25* to *Table 29* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 19*.

Table 25. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6V

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, executing from Flash	External clock (HSE bypass)	72 MHz	66.4	76.5	76.9	77.4	33.0	37.2	38.1	38.9	mA
			64 MHz	59.8	66.4	67.7	68.6	29.7	33.5	34.3	35.0	
			48 MHz	47.3	53.7	53.8	55.1	23.2	26.2	27.1	28.0	
			32 MHz	33.3	36.8	37.4	38.5	16.8	19.8	20.6	21.4	
			24 MHz	26.0	29.4	30.0	31.2	13.5	16.6	17.4	18.6	
			8 MHz	10.7	13.8	14.4	15.3	6.63	10.2	10.5	11.2	
			1 MHz	4.27	7.47	8.13	8.90	3.78	7.40	7.70	8.50	
		Internal clock (HSI)	64 MHz	55.6	59.6	62.8	63.2	29.4	33.1	34.5	35.0	
			48 MHz	43.6	47.0	49.2	50.1	23.1	26.2	27.1	28.0	
			32 MHz	30.8	33.6	35.3	35.8	16.7	19.8	20.6	21.5	
			24 MHz	24.0	28.0	28.2	29.7	13.5	16.5	17.5	18.4	
			8 MHz	10.5	13.6	14.7	15.2	6.63	9.74	10.6	11.2	
I_{DD}	Supply current in Run mode, executing from RAM	External clock (HSE bypass)	72 MHz	66.2	76.2(2)	76.7	77.2(2)	32.8	36.9(2)	37.7	38.5(2)	
			64 MHz	59.6	66.2	67.6	68.4	29.3	33.1	33.9	34.4	
			48 MHz	47.0	53.4	53.6	54.9	22.4	25.6	26.2	27.2	
			32 MHz	33.0	36.6	37.2	38.1	16.0	19.0	19.5	20.4	
			24 MHz	25.6	29.0	29.5	30.6	12.8	15.7	16.3	17.6	
			8 MHz	10.3	13.4	13.8	14.7	6.40	9.48	9.93	10.90	

Table 32. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DD} = 3.3 V C_{ext} = 0 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.90	mA
			4 MHz	0.93	
			8 MHz	1.16	
			18 MHz	1.60	
			36 MHz	2.51	
			48 MHz	2.97	
		V_{DD} = 3.3 V C_{ext} = 10 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.93	
			4 MHz	1.06	
			8 MHz	1.47	
			18 MHz	2.26	
			36 MHz	3.39	
			48 MHz	5.99	
		V_{DD} = 3.3 V C_{ext} = 22 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.03	
			4 MHz	1.30	
			8 MHz	1.79	
			18 MHz	3.01	
			36 MHz	5.99	
		V_{DD} = 3.3 V C_{ext} = 33 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.10	
			4 MHz	1.31	
			8 MHz	2.06	
			18 MHz	3.47	
			36 MHz	8.35	
		V_{DD} = 3.3 V C_{ext} = 47 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	1.20	
			4 MHz	1.54	
			8 MHz	2.46	
			18 MHz	4.51	
			36 MHz	9.98	

1. CS = 5 pF (estimated value).

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- all I/O pins are in analog input configuration
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature at 25°C and $V_{DD} = V_{DDA} = 3.3$ V.

Table 33. Peripheral current consumption

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
BusMatrix (2)	8.3	µA/MHz
DMA1	7.0	
DMA2	5.4	
FSMC	35.0	
CRC	1.5	
GPIOH	1.3	
GPIOA	5.4	
GPIOB	5.3	
GPIOC	5.4	
GPIOD	5.0	
GPIOE	5.4	
GPIOF	5.2	
GPIOG	5.0	
TSC	5.2	
ADC1&2	15.4	
APB2-Bridge (3)	3.1	
SYSCFG	4.0	
TIM1	26.0	
USART1	17.7	
SPI4	6.2	
TIM15	11.9	
TIM16	8.0	
TIM17	8.5	

Table 53. Synchronous multiplexed NOR/PSRAM read timings(1) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	ns
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	4	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	6	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. Based on characterization, not tested in production.

Figure 25. Synchronous multiplexed PSRAM write timings

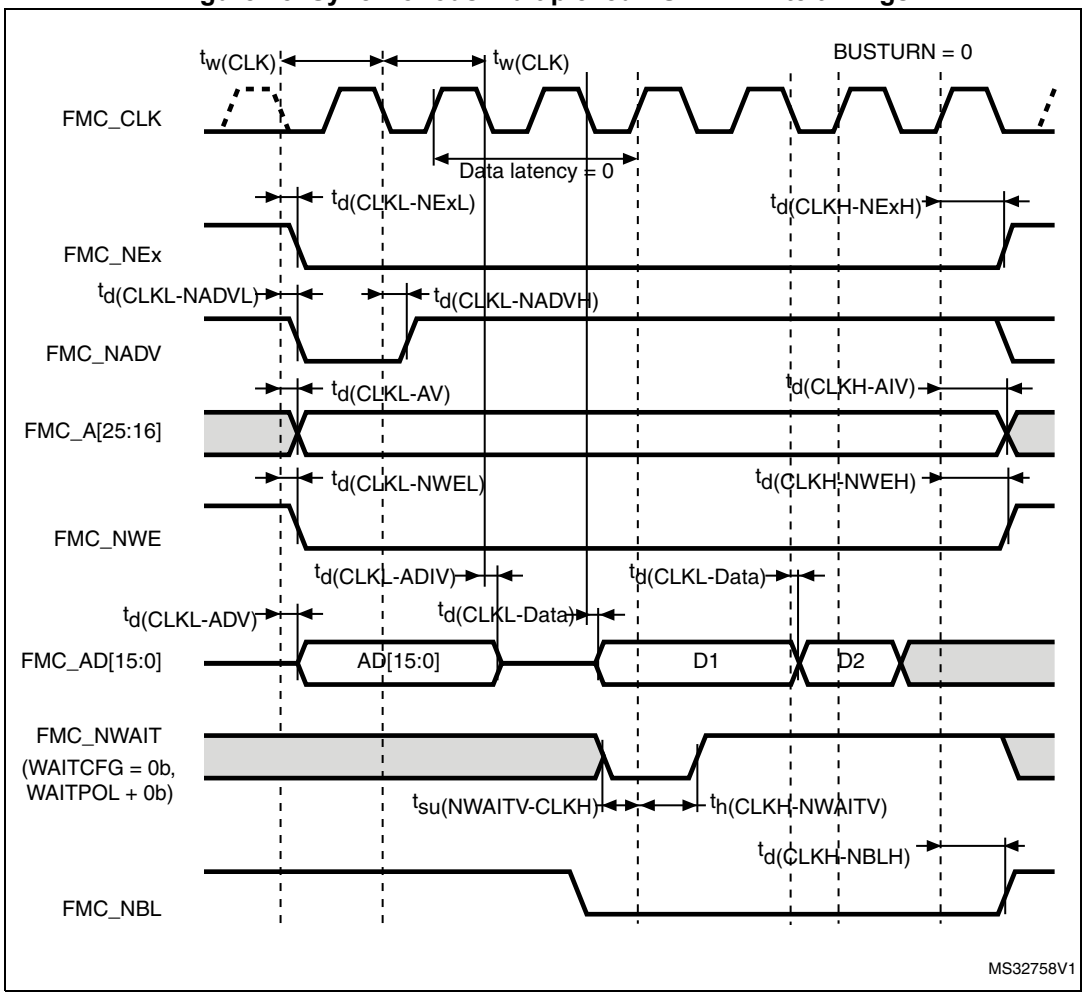


Table 54. Synchronous multiplexed PSRAM write timings(1) (2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period, VDD range= 2.7 to 3.6 V	2THCLK-1	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	5.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	THCLK+1	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	7	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	2	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	0	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	5.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	THCLK+1	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	7.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	8	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	6	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	THCLK+1	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	3	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	5	-	

1. Based on characterization, not tested in production.
2. C_L = 30 pF.

Table 71. IWDG min/max timeout period at 40 kHz (LSI) (1)

Prescaler divider	PR[2:0] bits	Min timeout (ms) RL[11:0]= 0x000	Max timeout (ms) RL[11:0]= 0xFFF
/4	0	0.1	409.6
/8	1	0.2	819.2
/16	2	0.4	1638.4
/32	3	0.8	3276.8
/64	4	1.6	6553.6
/128	5	3.2	13107.2
/256	7	6.4	26214.4

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 72. WWDG min-max timeout value @72 MHz (PCLK)(1)

Prescaler	WDGTB	Min timeout value	Max timeout value
1	0	0.05687	3.6409
2	1	0.1137	7.2817
4	2	0.2275	14.564
8	3	0.4551	29.127

1. Guaranteed by design, not tested in production.

6.3.18 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev.03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1Mbits/s

The I²C timings requirements are guaranteed by design when the I²C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.15: I/O port characteristics*.

All I²C I/Os embed an analog filter, refer to the *Table 73: I2C analog filter characteristics*.

USB characteristics

Table 76. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

Table 77. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)	-	3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F302xD/E USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design, not tested in production.
5. R_L is the load connected on the USB drivers.

Figure 47. USB timings: definition of data signal rise and fall time

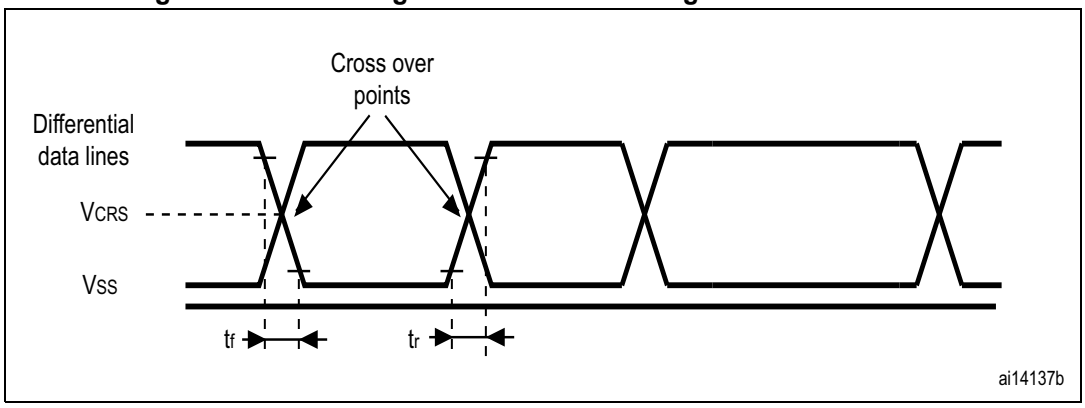


Table 78. USB: full-speed electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_r	Rise time(2)	C_L = 50 pF	4	-	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	-	20	ns

Table 78. USB: full-speed electrical characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	-	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	-	2.0	V
Output driver Impedance(3)	Z_{DRV}	driving high and low	28	40	44	Ω

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed information, refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-), the matching impedance is already included in the embedded driver.

CAN (controller area network) interface

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

6.3.19 ADC characteristics

Unless otherwise specified, the parameters given in *Table 79* to *Table 82* are guaranteed by design, with conditions summarized in *Table 19*.

Table 79. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC	-	2.0	-	3.6	V
I_{DDA}	Current on VDDA pin (see *Figure 48*)	Single-ended mode, 5 MSPS	-	907	1033	µA
		Single-ended mode, 1 MSPS	-	194	285.5	
		Single-ended mode, 200 KSPS	-	51.5	70	
		Differential mode, 5 MSPS	-	887.5	1009	
		Differential mode, 1 MSPS	-	212	285	
		Differential mode, 200 KSPS	-	51	69.5	

Table 87. Comparator characteristics(1) (continued)

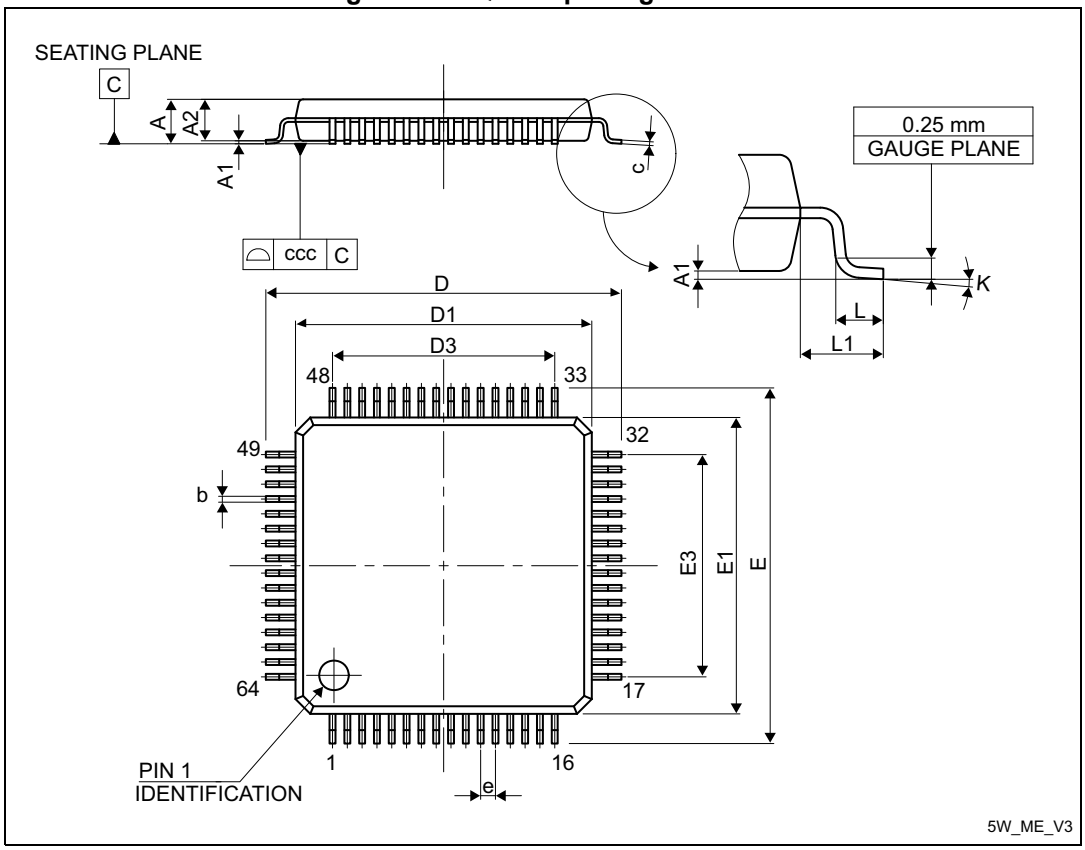
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
TV_{OFFSET}	Total offset variation	Full temperature range	-	-	3	mV
I_{DDA}	COMP current consumption	-	-	400	600	µA

1. Guaranteed by design, not tested in production.

7.6 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package.

Figure 66. LQFP64 package outline



1. Drawing is not to scale.

Table 98. LQFP64 package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 99* T_{Jmax} is calculated as follows:

– For LQFP100, 42 °C/W

T_{Jmax} = 82 °C + (42 °C/W × 447 mW) = 82 °C + 18.774 °C = 100.774 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Part numbering*).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: T_{Amax} = T_{Jmax} - (42°C/W × 447 mW) = 105-18.774 = 86.226 °C

Suffix 7: T_{Amax} = T_{Jmax} - (42°C/W × 447 mW) = 125-18.774 = 106.226 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high temperature with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 99* T_{Jmax} is calculated as follows:

– For LQFP100, 42 °C/W

T_{Jmax} = 100 °C + (42 °C/W × 134 mW) = 100 °C + 5.628 °C = 105.628 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Part numbering*) unless we reduce the power dissipation to be able to use suffix 6 parts.