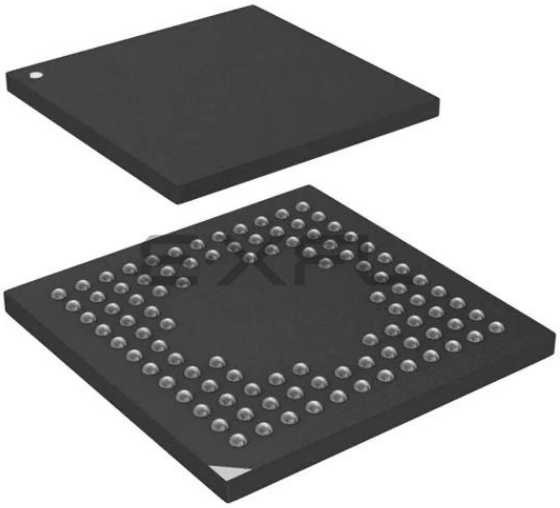


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	84
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 17x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302veh6

Table 47. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings . . . 92
Table 48. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings . . . 93
Table 49. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings . . . 93
Table 50. Asynchronous multiplexed PSRAM/NOR read timings . . . 94
Table 51. Asynchronous multiplexed PSRAM/NOR write timings . . . 96
Table 52. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings . . . 96
Table 53. Synchronous multiplexed NOR/PSRAM read timings . . . 97
Table 54. Synchronous multiplexed PSRAM write timings . . . 99
Table 55. Synchronous non-multiplexed NOR/PSRAM read timings . . . 100
Table 56. Synchronous non-multiplexed PSRAM write timings . . . 102
Table 57. Switching characteristics for PC Card/CF read and write cycles in attribute/common space . . . 103
Table 58. Switching characteristics for PC Card/CF read and write cycles in I/O space . . . 106
Table 59. Switching characteristics for NAND Flash read cycles . . . 109
Table 60. Switching characteristics for NAND Flash write cycles . . . 109
Table 61. EMS characteristics . . . 110
Table 62. EMI characteristics . . . 111
Table 63. ESD absolute maximum ratings . . . 111
Table 64. Electrical sensitivities . . . 112
Table 65. I/O current injection susceptibility . . . 112
Table 66. I/O static characteristics . . . 113
Table 67. Output voltage characteristics . . . 116
Table 68. I/O AC characteristics . . . 117
Table 69. NRST pin characteristics . . . 118
Table 70. TIMx characteristics . . . 119
Table 71. IWDG min/max timeout period at 40 kHz (LSI) . . . 120
Table 72. WWDG min-max timeout value @72 MHz (PCLK) . . . 120
Table 73. I2C analog filter characteristics . . . 121
Table 74. SPI characteristics . . . 121
Table 75. I^2S characteristics . . . 124
Table 76. USB startup time . . . 126
Table 77. USB DC electrical characteristics . . . 126
Table 78. USB: full-speed electrical characteristics . . . 126
Table 79. ADC characteristics . . . 127
Table 80. Maximum ADC RAIN . . . 130
Table 81. ADC accuracy - limited test conditions, 100-/144-pin packages . . . 132
Table 82. ADC accuracy, 100-pin/144-pin packages . . . 133
Table 83. ADC accuracy - limited test conditions, 64-pin packages . . . 135
Table 84. ADC accuracy, 64-pin packages . . . 136
Table 85. ADC accuracy at 1MSPS . . . 138
Table 86. DAC characteristics . . . 139
Table 87. Comparator characteristics . . . 141
Table 88. Operational amplifier characteristics . . . 143
Table 89. TS characteristics . . . 145
Table 90. Temperature sensor calibration values . . . 145
Table 91. V_{BAT} monitoring characteristics . . . 146
Table 92. LQFP144 mechanical data . . . 148
Table 93. UFBGA100 package mechanical data . . . 151
Table 94. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA) . . . 152
Table 95. LQPF100 package mechanical data . . . 154
Table 96. WLCSP100 package mechanical data . . . 158
Table 97. WLCSP100 recommended PCB design rules (0.4 mm pitch) . . . 159

Figure 45. I^2S slave timing diagram (Philips protocol)(1) . . . 125
Figure 46. I^2S master timing diagram (Philips protocol)(1) . . . 125
Figure 47. USB timings: definition of data signal rise and fall time . . . 126
Figure 48. ADC typical current consumption on VDDA pin . . . 129
Figure 49. ADC typical current consumption on VREF+ pin . . . 130
Figure 50. ADC accuracy characteristics . . . 138
Figure 51. Typical connection diagram using the ADC . . . 139
Figure 52. 12-bit buffered /non-buffered DAC . . . 141
Figure 53. OPAMP voltage noise versus frequency . . . 145
Figure 54. LQFP144 package outline . . . 147
Figure 55. Recommended footprint for the LQFP144 package . . . 149
Figure 56. LQFP144 marking example (package top view) . . . 150
Figure 57. UFBGA100 package outline . . . 151
Figure 58. Recommended footprint for the UFBGA100 package . . . 152
Figure 59. UFBGA100 marking example (package top view) . . . 153
Figure 60. LQFP100 package outline . . . 154
Figure 61. Recommended footprint for the LQFP100 package . . . 155
Figure 62. LQFP100 marking example (package top view) . . . 156
Figure 63. WLCSP100 package outline . . . 157
Figure 64. Recommended footprint for the WLCSP100 package . . . 158
Figure 65. WLCSP100 marking example (package top view) . . . 159
Figure 66. LQFP64 package outline . . . 160
Figure 67. Recommended footprint for the LQFP64 package . . . 161
Figure 68. LQFP64 marking example (package top view) . . . 162
Figure 69. LQFP100 P_D max vs. T_A . . . 165

3.4 Embedded SRAM

STM32F302xD/E devices feature 64 Kbyte of embedded SRAM with hardware parity check implemented on the first 32 Kbyte. The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.5 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in the system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PA2/PA3) or USB (PA11/PA12) through DFU (device firmware upgrade).

3.6 Cyclic redundancy check (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

Table 4. STM32F302xD/E peripheral interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action
GPIO RTCCLK HSE/32 MC0	TIM16	Clock source used as input channel for HSI and LSI calibration
CSS CPU (hard fault) COMPx GPIO	TIM1 TIM15, 16, 17	Timer break
GPIO	TIMx	External trigger, timer break
	ADCx DAC1	Conversion external trigger
DAC1	COMPx	Comparator inverting input

Note: For more details about the interconnect actions, refer to the corresponding sections in the STM32F302xD/E reference manual (RM0365).

3.9 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

3.18.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

3.19 Real-time clock (RTC) and backup registers

The RTC and the 16 backup registers are supplied through a switch that takes power from either the V_{DD} supply when present or the V_{BAT} pin. The backup registers are sixteen 32-bit registers used to store 64 bytes of user application data when V_{DD} power is not present.

They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Automatic correction for 28, 29 (leap year), 30 and 31 days of the month.
- Two programmable alarms with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.
- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP/STANDBY capability.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

3.20 Inter-integrated circuit interface (I^2C)

Up to three I^2C bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes.

Table 13. STM32F302xD/E pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP100	LQFP144						
-	-	-	90	PG5	I/O	FT	(1)	EVENTOUT, FMC_A15	-
-	-	-	91	PG6	I/O	FT	(1)	EVENTOUT, FMC_INT2	-
-	-	-	92	PG7	I/O	FT	(1)	EVENTOUT, FMC_INT3	-
-	-	-	93	PG8	I/O	FT	(1)	EVENTOUT	-
-	-	-	94	VSS	S	-	(1)	-	-
-	-	-	95	VDD	S	-	(1)	-	-
37	63	F4	96	PC6	I/O	FT	-	EVENTOUT, TIM3_CH1, I2S2_MCK, COMP6_OUT	-
38	64	F2	97	PC7	I/O	FT	-	EVENTOUT, TIM3_CH2, I2S3_MCK	-
39	65	F1	98	PC8	I/O	FT	-	EVENTOUT, TIM3_CH3	-
40	66	F3	99	PC9	I/O	FTf	-	EVENTOUT, TIM3_CH4, I2C3_SDA, I2SCKIN	-
41	67	F5	100	PA8	I/O	FTf	-	MCO, I2C3_SCL, I2C2_SMBAL, I2S2_MCK, TIM1_CH1, USART1_CK, TIM4_ETR, EVENTOUT	-
42	68	E5	101	PA9	I/O	FTf	-	I2C3_SMBAL, TSC_G4_IO1, I2C2_SCL, I2S3_MCK, TIM1_CH2, USART1_TX, TIM15_BKIN, TIM2_CH3, EVENTOUT	-
43	69	E1	102	PA10	I/O	FTf	-	TIM17_BKIN, TSC_G4_IO2, I2C2_SDA, SPI2_MISO/I2S2ext_SD, TIM1_CH3, USART1_RX, COMP6_OUT, TIM2_CH4, EVENTOUT	-
44	70	E2	103	PA11	I/O	FT	-	SPI2_MOSI/I2S2_SD, TIM1_CH1N, USART1_CTS, COMP1_OUT, CAN_RX, TIM4_CH1, TIM1_CH4, TIM1_BKIN2, EVENTOUT	USB_DM

Table 13. STM32F302xD/E pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP100	LQFP144						
-	82	C3	115	PD1	I/O	FT	(1)	EVENTOUT, CAN_TX, FMC_D3	-
54	83	A4	116	PD2	I/O	FT	-	EVENTOUT, TIM3_ETR, UART5_RX	-
-	84	B4	117	PD3	I/O	FT	(1)	EVENTOUT, TIM2_CH1/TIM2_ETR, USART2_CTS, FMC_CLK	-
-	85	C4	118	PD4	I/O	FT	(1)	EVENTOUT, TIM2_CH2, USART2_RTS, FMC_NOE	-
-	86	-	119	PD5	I/O	FT	(1)	EVENTOUT, USART2_TX, FMC_NWE	-
-	-	-	120	VSS	S	-	(1)	-	-
-	-	-	121	VDD	S	-	(1)	-	-
-	87	-	122	PD6	I/O	FT	(1)	EVENTOUT, TIM2_CH4, USART2_RX, FMC_NWAIT	-
-	88	D4	123	PD7	I/O	FT	(1)	EVENTOUT, TIM2_CH3, USART2_CK, FMC_NE1/FMC_NCE2	-
-	-	-	124	PG9	I/O	FT	(1)	EVENTOUT, FMC_NE2/FMC_NCE3	-
-	-	-	125	PG10	I/O	FT	(1)	EVENTOUT, FMC_NCE4_1/FMC_NE3	-
-	-	-	126	PG11	I/O	FT	(1)	EVENTOUT, FMC_NCE4_2	-
-	-	-	127	PG12	I/O	FT	(1)	EVENTOUT, FMC_NE4	-
-	-	-	128	PG13	I/O	FT	(1)	EVENTOUT, FMC_A24	-
-	-	-	129	PG14	I/O	FT	(1)	EVENTOUT, FMC_A25	-
-	-	-	130	VSS	S	-	(1)	-	-
-	-	-	131	VDD	S	-	(1)	-	-
-	-	-	132	PG15	I/O	FT	(1)	EVENTOUT	-

Table 14. STM32F302xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM12/3/4/8/20/15/GPCOMP1	I2C3//15/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port D	PD5	-	EVENT OUT	-	-	-	-	-	USART2_TX	-	-	-	-	FMC_NWE	-	-	-
	PD6	-	EVENT OUT	TIM2_CH4	-	-	-	-	USART2_RX	-	-	-	-	FMC_NWAIT	-	-	-
	PD7	-	EVENT OUT	TIM2_CH3	-	-	-	-	USART2_CK	-	-	-	-	FMC_NE1/FMC_NCE2	-	-	-
	PD8	-	EVENT OUT	-	-	-	-	-	USART3_TX	-	-	-	-	FMC_D13	-	-	-
	PD9	-	EVENT OUT	-	-	-	-	-	USART3_RX	-	-	-	-	FMC_D14	-	-	-
	PD10	-	EVENT OUT	-	-	-	-	-	USART3_CK	-	-	-	-	FMC_D15	-	-	-
	PD11	-	EVENT OUT	-	-	-	-	-	USART3_CTS	-	-	-	-	FMC_A16	-	-	-
	PD12	-	EVENT OUT	TIM4_CH1	TSC_G8_IO1	-	-	-	USART3_RTS	-	-	-	-	FMC_A17	-	-	-
	PD13	-	EVENT OUT	TIM4_CH2	TSC_G8_IO2	-	-	-	-	-	-	-	-	FMC_A18	-	-	-
	PD14	-	EVENT OUT	TIM4_CH3	TSC_G8_IO3	-	-	-	-	-	-	-	-	FMC_D0	-	-	-
	PD15	-	EVENT OUT	TIM4_CH4	TSC_G8_IO4	-	-	SPI2_NSS	-	-	-	-	-	FMC_D1	-	-	-

Table 14. STM32F302xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3//15/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port E	PE12	-	EVENT OUT	TIM1_CH3N	-	-	SPI4_SCK	-	-	-	-	-	-	FMC_D9	-	-	-
	PE13	-	EVENT OUT	TIM1_CH3	-	-	SPI4_MISO	-	-	-	-	-	-	FMC_D10	-	-	-
	PE14	-	EVENT OUT	TIM1_CH4	-	-	SPI4_MOSI	TIM1_BKIN2	-	-	-	-	-	FMC_D11	-	-	-
	PE15	-	EVENT OUT	TIM1_BKIN	-	-	-	-	USART3_RX	-	-	-	-	FMC_D12	-	-	-
Port F	PF0	-	EVENT OUT	-	-	I2C2_SDA	SPI2_NSS/I2S2_WS	TIM1_CH3N	-	-	-	-	-	-	-	-	-
	PF1	-	EVENT OUT	-	-	I2C2_SCL	SPI2_SCK/I2S2_CK	-	-	-	-	-	-	-	-	-	-
	PF2	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A2	-	-	-
	PF3	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A3	-	-	-
	PF4	-	EVENT OUT	COMP1_OUT	-	-	-	-	-	-	-	-	-	FMC_A4	-	-	-
	PF5	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A5	-	-	-
	PF6	-	EVENT OUT	TIM4_CH4	-	I2C2_SCL	-	-	USART3_RTS	-	-	-	-	FMC_NIORD	-	-	-
	PF7	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NREG	-	-	-

Table 14. STM32F302xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3//15/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port G	PG5	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A15	-	-	-
	PG6	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_INT2	-	-	-
	PG7	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_INT3	-	-	-
	PG8	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PG9	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NE2/FMC_NCE3	-	-	-
	PG10	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NCE4_1/FMC_NE3	-	-	-
	PG11	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NCE4_2	-	-	-
	PG12	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_NE4	-	-	-
	PG13	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A24	-	-	-
	PG14	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A25	-	-	-
	PG15	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Table 14. STM32F302xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM1/2/3/4/8/20/15/GPCOMP1	I2C3//15/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port H	PH0	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A0	-	-	-
	PH1	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	FMC_A1	-	-	-
	PH2	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- all I/O pins are in analog input configuration
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature at 25°C and $V_{DD} = V_{DDA} = 3.3$ V.

Table 33. Peripheral current consumption

Peripheral	Typical consumption(1)	Unit
	I_{DD}	
BusMatrix (2)	8.3	µA/MHz
DMA1	7.0	
DMA2	5.4	
FSMC	35.0	
CRC	1.5	
GPIOH	1.3	
GPIOA	5.4	
GPIOB	5.3	
GPIOC	5.4	
GPIOD	5.0	
GPIOE	5.4	
GPIOF	5.2	
GPIOG	5.0	
TSC	5.2	
ADC1&2	15.4	
APB2-Bridge (3)	3.1	
SYSCFG	4.0	
TIM1	26.0	
USART1	17.7	
SPI4	6.2	
TIM15	11.9	
TIM16	8.0	
TIM17	8.5	

Table 50. Asynchronous multiplexed PSRAM/NOR read timings(1) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	ns
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	THCLK	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOE high setup time	THCLK+1	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. Based on characterization, not tested in production.

Figure 23. Asynchronous multiplexed PSRAM/NOR write timings

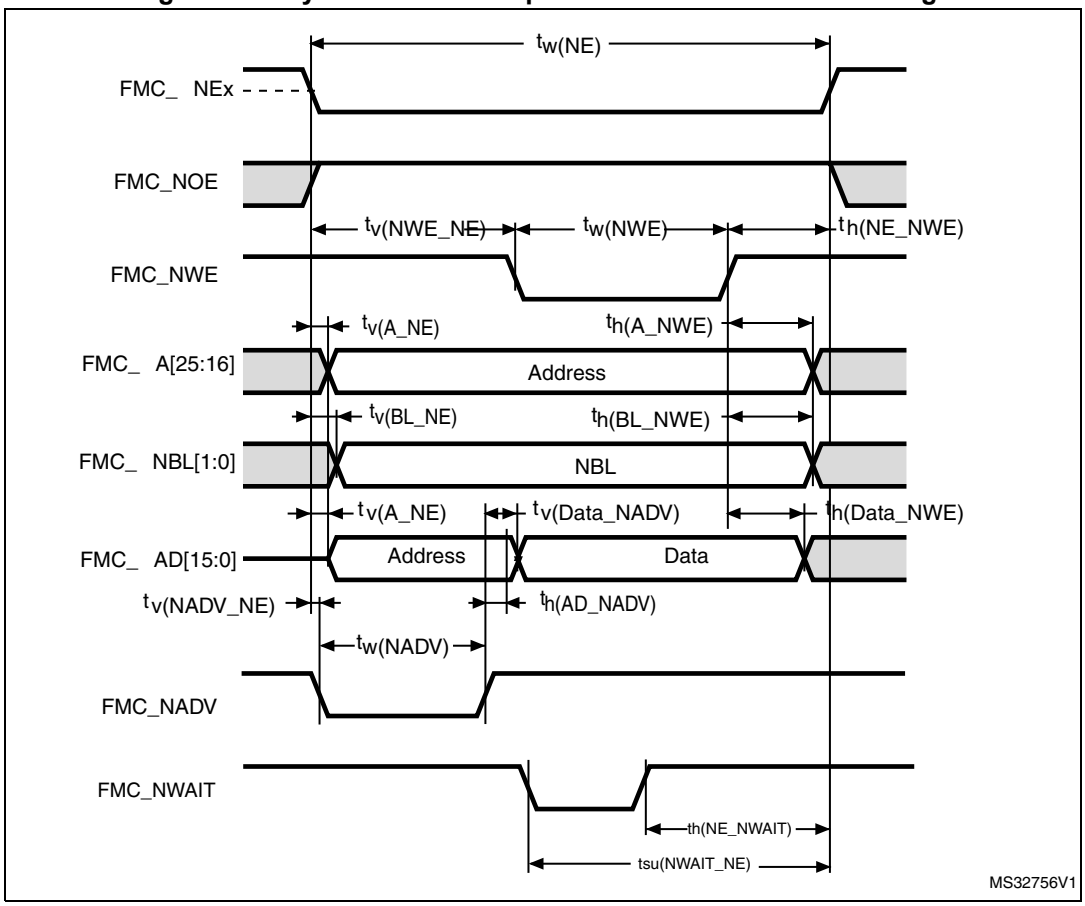


Table 55. Synchronous non-multiplexed NOR/PSRAM read timings(1) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	5	-	ns
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	4	-	

1. Based on characterization, not tested in production.

Figure 27. Synchronous non-multiplexed PSRAM write timings

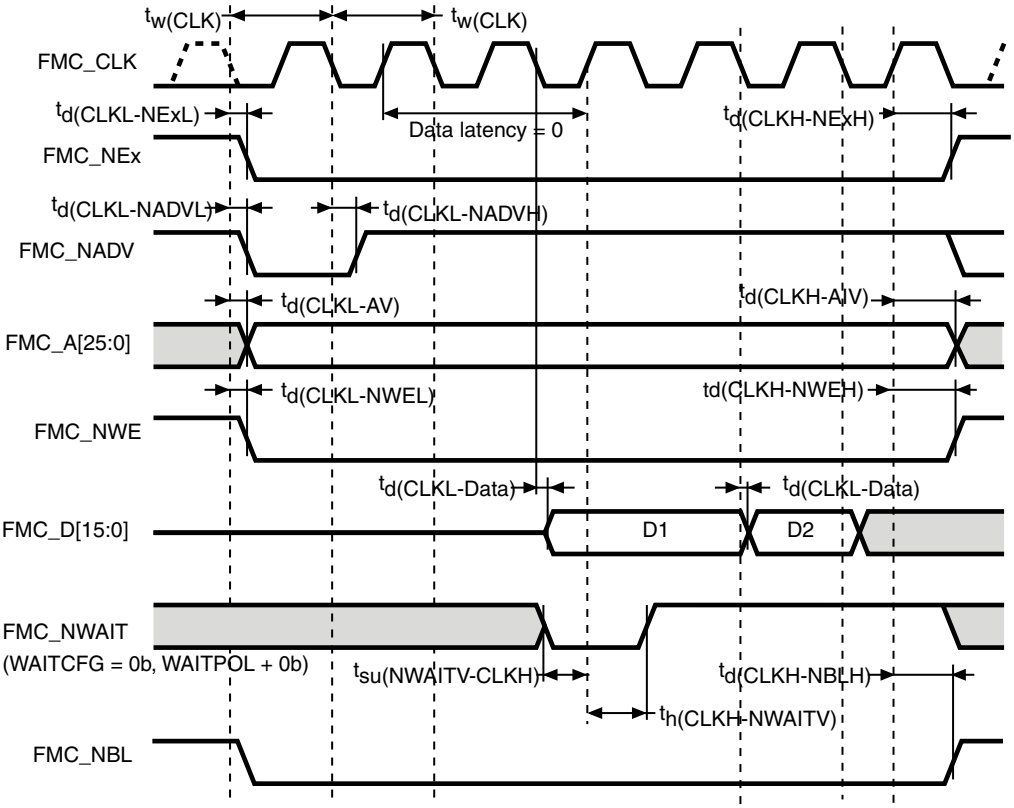
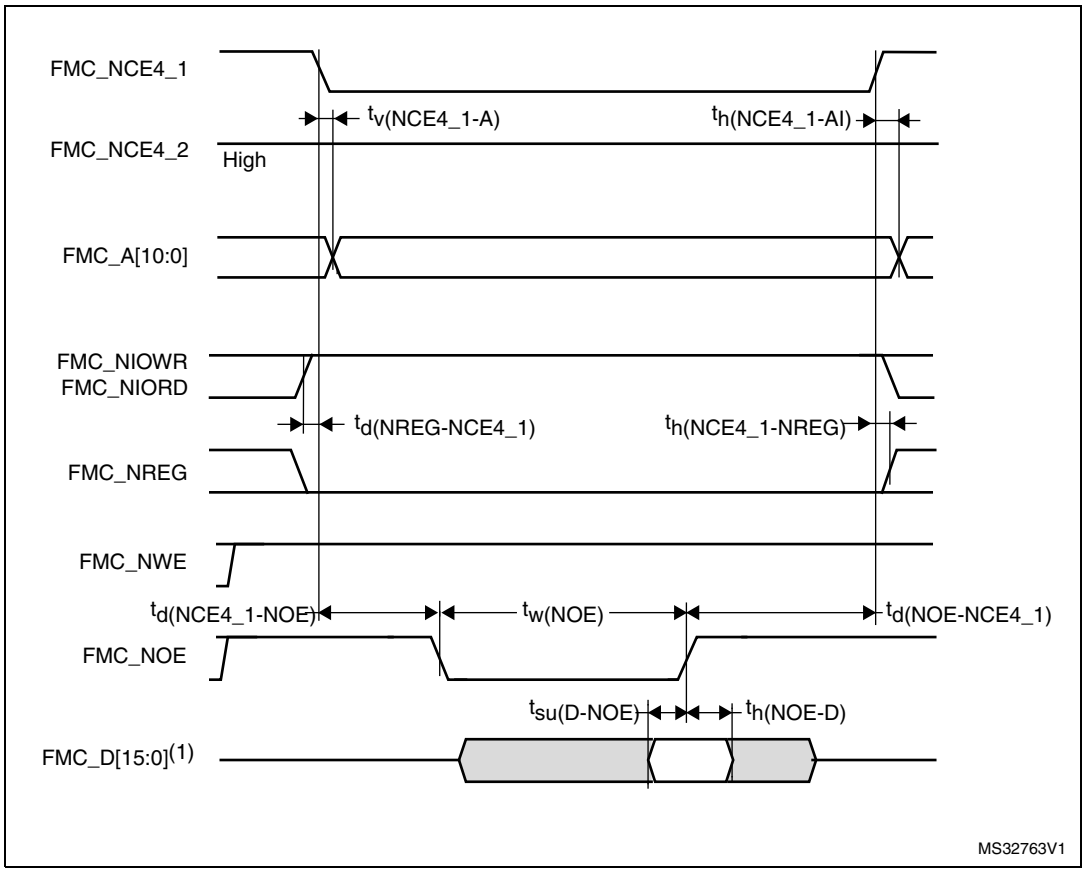


Figure 30. PC Card/CompactFlash controller waveforms for attribute memory read access



1. Only data bits 0...7 are read (bits 8...15 are disregarded).

6.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling two LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 61*. They are based on the EMS levels and classes defined in application note AN1709.

Table 61. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25°C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 64. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II Level A

6.3.14 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in *Table 65*.

Table 65. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	-0	NA	mA
	Injected current on PF3, PC1, PC2, PA1, PA2, PA3, PA4, PA5, PA6, PA7, PB0, PB1, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB13, PB14, PB15, PD8, PD9, PD10, PD11, PD12, PD13, PD14 pins with induced leakage current on adjacent pins less than -50 µA or more than +400 µA	-5	+5	
	Injected current on PF2, PF4, PC0, PC1, PC2, PC3, PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7, PC4, PC5, PB2, PB11 with induced leakage current on other pins from this group less than -50 µA or more than +400 µA	-5	+5	

Table 88. Operational amplifier characteristics(1) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
PGA gain	Non inverting gain value	-	-	2	-	-
			-	4	-	-
			-	8	-	-
			-	16	-	-
$R_{network}$	R2/R1 internal resistance values in PGA mode (3)	Gain=2	-	5.4/5.4	-	kΩ
		Gain=4	-	16.2/5.4	-	
		Gain=8	-	37.8/5.4	-	
		Gain=16	-	40.5/2.7	-	
PGA gain error	PGA gain error	-	-1%	-	1%	-
I_{bias}	OPAMP input bias current	-	-	-	±0.2(4)	µA
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, Cload = 50pF, Rload = 4 KΩ	-	4	-	MHz
		PGA Gain = 4, Cload = 50pF, Rload = 4 KΩ	-	2	-	
		PGA Gain = 8, Cload = 50pF, Rload = 4 KΩ	-	1	-	
		PGA Gain = 16, Cload = 50pF, Rload = 4 KΩ	-	0.5	-	
en	Voltage noise density	@ 1KHz, Output loaded with 4 KΩ	-	109	-	$\frac{nV}{\sqrt{Hz}}$
		@ 10KHz, Output loaded with 4 KΩ	-	43	-	

1. Guaranteed by design, not tested in production.
2. The saturation voltage can be also limited by the Iload (drive current).
3. R2 is the internal resistance between OPAMP output and OPAMP inverting input.
   R1 is the internal resistance between OPAMP inverting input and ground.
   The PGA gain =1+R2/R1
4. Mostly TTa I/O leakage, when used in analog mode.

7.7 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 19: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum temperature in °C,
- Θ_{JA} is the package junction-to- thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 99. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-** LQFP144 - 20 × 20 mm	33	°C/W
	Thermal resistance junction- UFBGA100 - 7 × 7 mm	59	
	Thermal resistance junction- LQFP100 - 14 × 14 mm	42	
	Thermal resistance junction- WLCSP100 - 0.4 mm pitch	44	
	Thermal resistance junction- LQFP64 - 10 × 10 mm / 0.5 mm pitch	46	

7.7.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.7.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed temperature at maximum dissipation and to a specific maximum junction temperature.

As applications do not commonly use the STM32F302xD/E at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range is best suited to the application.

9 Revision history

Table 101. Document revision history

Date	Revision	Changes
20-Jan-2015	1	Initial release.
09-Apr-2015	2	Added USB_DM and USB_DP as additional function to PA11 and PA12 description, respectively in *Table 13: STM32F302xD/E pin definitions*. Updated: – *Figure 56: LQFP144 marking example (package top view)*, – *Figure 59: UFBGA100 marking example (package top view)*, – *Figure 62: LQFP100 marking example (package top view)*.
08-Mar-2016	3	Renamed: – FMC as FSMC, – CCM RAM as CCM SRAM. Removed: – *table: I2C timings specification* and *Figure: I2C bus AC waveforms and measurement circuit* in *Section : I2C interface characteristics*. Added: – Package information for WLCSP100 in *Section 7: Package information*.
18-Oct-2016	4	Updated: *Table 2: STM32F302xD/E family device features and peripheral counts*, *Section 3.17: Ultra-fast comparators (COMP)*, *Table 66: DAC characteristics*, *Table 61: ADC characteristics*, *Table 13: STM32F302xD/E pin definitions*, *Table 14: STM32F302xD/E alternate function mapping*, *Figure 41: Recommended NRST pin protection* Added: *Table 37: Wakeup time using USART*.