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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	86
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 17x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302vet6

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F302xD/E microcontrollers.

This STM32F302xD/E datasheet should be read in conjunction with the reference manual of STM32F302xB/C/D/E, STM32F302x6/8 devices (RM0365) available on STMicroelectronics website at *www.st.com*.

For information on the ARM® Cortex®-M4 core with FPU, refer to the following documents:

- *Cortex® -M4 with FPU Technical Reference Manual*, available from the www.arm.com website
- *STM32F3 and STM32F4 Series Cortex® -M4 programming manual* (PM0214) available on STMicroelectronics website at *www.st.com*.

3.7.4 Low-power modes

The STM32F302xD/E supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- Sleep mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and wake up the CPU when an interrupt/event occurs.

- Stop mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the USB wakeup, the RTC alarm, COMPx, I2Cx or U(S)ARTx.

- Standby mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin or an RTC alarm occurs.

Note: The RTC, the IWDG and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.8 Interconnect matrix

Several peripherals have direct connections between them. This allows autonomous communication between peripherals, saving CPU resources thus power supply consumption. In addition, these hardware connections allow fast and predictable latency.

Table 4. STM32F302xD/E peripheral interconnect matrix

Interconnect source	Interconnect destination	Interconnect action
TIMx	TIMx	Timers synchronization or chaining
	ADCx DAC1	Conversion triggers
	DMA	Memory to memory transfer trigger
	Compx	Comparator output blanking
COMPx	TIMx	Timer input: OCREF_CLR input, input capture
ADCx	TIMx	Timer triggered by analog watchdog

4 Pinout and pin description

Figure 4. STM32F302xD/E LQFP64 pinout

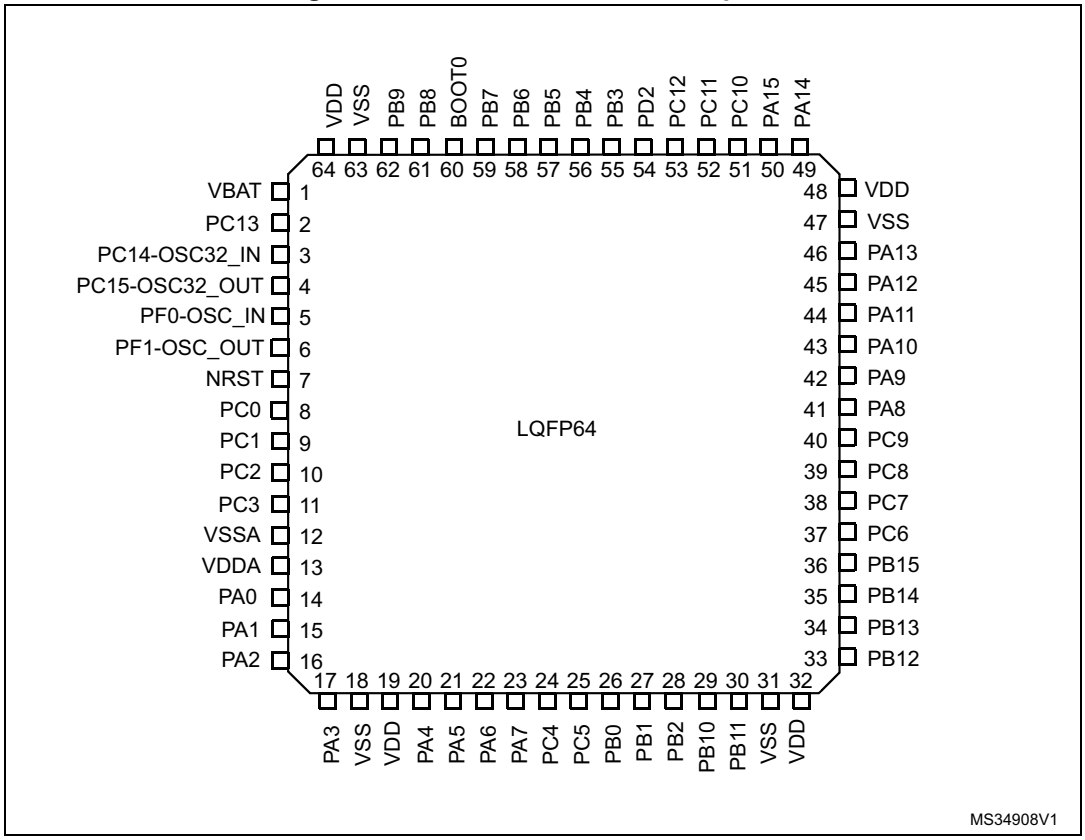
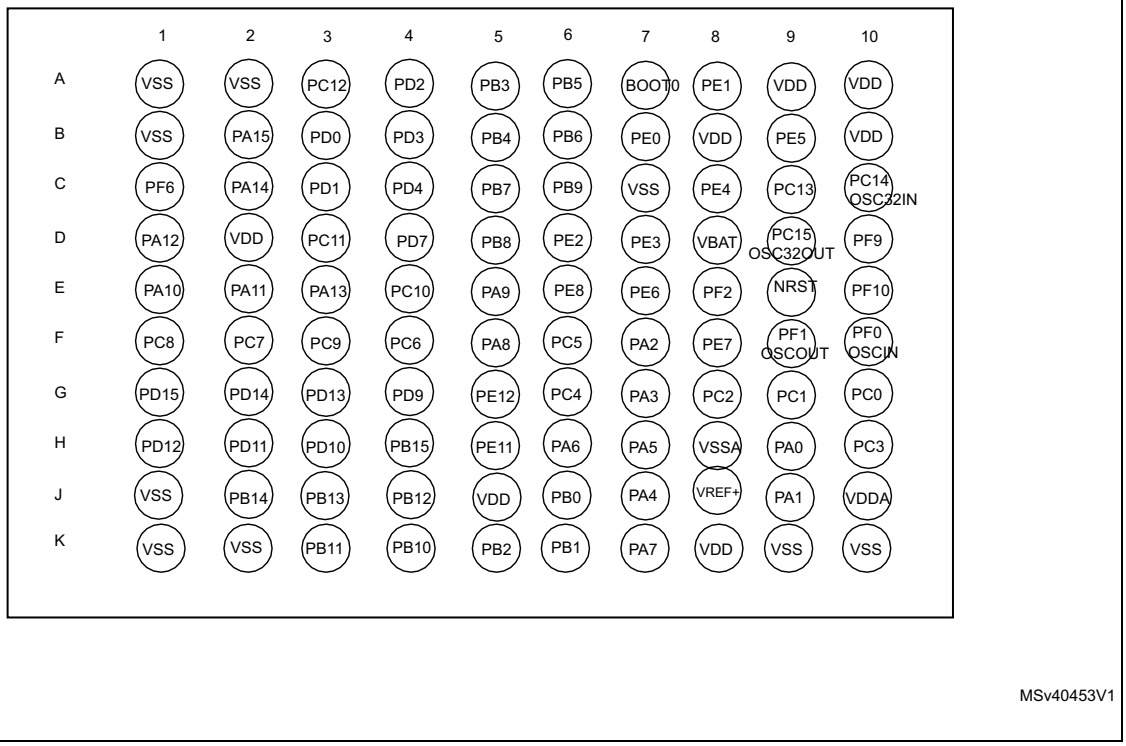


Figure 7. STM32F302xD/E WLCSP100 ballout



MSv40453V1

Table 13. STM32F302xD/E pin definitions (continued)

Pin number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP64	LQFP100	WLCSP100	LQFP144						
-	-	-	90	PG5	I/O	FT	(1)	EVENTOUT, FMC_A15	-
-	-	-	91	PG6	I/O	FT	(1)	EVENTOUT, FMC_INT2	-
-	-	-	92	PG7	I/O	FT	(1)	EVENTOUT, FMC_INT3	-
-	-	-	93	PG8	I/O	FT	(1)	EVENTOUT	-
-	-	-	94	VSS	S	-	(1)	-	-
-	-	-	95	VDD	S	-	(1)	-	-
37	63	F4	96	PC6	I/O	FT	-	EVENTOUT, TIM3_CH1, I2S2_MCK, COMP6_OUT	-
38	64	F2	97	PC7	I/O	FT	-	EVENTOUT, TIM3_CH2, I2S3_MCK	-
39	65	F1	98	PC8	I/O	FT	-	EVENTOUT, TIM3_CH3	-
40	66	F3	99	PC9	I/O	FTf	-	EVENTOUT, TIM3_CH4, I2C3_SDA, I2SCKIN	-
41	67	F5	100	PA8	I/O	FTf	-	MCO, I2C3_SCL, I2C2_SMBAL, I2S2_MCK, TIM1_CH1, USART1_CK, TIM4_ETR, EVENTOUT	-
42	68	E5	101	PA9	I/O	FTf	-	I2C3_SMBAL, TSC_G4_IO1, I2C2_SCL, I2S3_MCK, TIM1_CH2, USART1_TX, TIM15_BKIN, TIM2_CH3, EVENTOUT	-
43	69	E1	102	PA10	I/O	FTf	-	TIM17_BKIN, TSC_G4_IO2, I2C2_SDA, SPI2_MISO/I2S2ext_SD, TIM1_CH3, USART1_RX, COMP6_OUT, TIM2_CH4, EVENTOUT	-
44	70	E2	103	PA11	I/O	FT	-	SPI2_MOSI/I2S2_SD, TIM1_CH1N, USART1_CTS, COMP1_OUT, CAN_RX, TIM4_CH1, TIM1_CH4, TIM1_BKIN2, EVENTOUT	USB_DM

Table 14. STM32F302xD/E alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM2/15/16/17/EVENT	I2C3/TIM12/3/4/8/20/15/GPCOMP1	I2C3//15/TSC	I2C1/2/TIM1/8/16/17	SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/Infrared	SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared	USART1/2/3/CAN/GPCOMP6	I2C3/GPCOMP1/2/3/4/5/6	CAN/TIM1/8/15	TIM2/3/4/8/17	TIM1/8	FSMC/TIM1	-	-	EVENT
Port C	PC10	-	EVENT OUT	-	-	-	UART4_TX	SPI3_SCK/I2S3_CK	USART3_TX	-	-	-	-	-	-	-	-
	PC11	-	EVENT OUT	-	-	-	UART4_RX	SPI3_MISO/I2S3ext_SD	USART3_RX	-	-	-	-	-	-	-	-
	PC12	-	EVENT OUT	-	-	-	UART5_TX	SPI3_MOSI/I2S3_SD	USART3_CK	-	-	-	-	-	-	-	-
	PC13	-	EVENT OUT	-	-	TIM1_CH1N	-	-	-	-	-	-	-	-	-	-	-
	PC14	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC15	-	EVENT OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Port D	PD0	-	EVENT OUT	-	-	-	-	-	CAN_RX	-	-	-	-	FMC_D2	-	-	-
	PD1	-	EVENT OUT	-	-	-		-	CAN_TX	-	-	-	-	FMC_D3	-	-	-
	PD2	-	EVENT OUT	TIM3_ETR	-	-	UART5_RX	-	-	-	-	-	-	-	-	-	-
	PD3	-	EVENT OUT	TIM2_CH1/TIM2_ETR	-	-	-	-	USART2_CTS	-	-	-	-	FMC_CLK	-	-	-
	PD4	-	EVENT OUT	TIM2_CH2	-	-	-	-	USART2_RTS	-	-	-	-	FMC_NOE	-	-	-

Table 15. Memory map, peripheral register boundary addresses (continued)

Bus	Boundary address	Size (bytes)	Peripheral
APB2	0x4001 2C00 - 0x4001 2FFF	1 K	TIM1
	0x4001 0800 - 0x4001 2BFF	9 K	Reserved
	0x4001 0400 - 0x4001 07FF	1 K	EXTI
	0x4001 0000 - 0x4001 03FF	1 K	SYSCFG + COMP + OPAMP
-	0x4000 7C00 - 0x4000 FFFF	32 K	Reserved
APB1	0x4000 7800 - 0x4000 7BFF	1 K	I2C3
	0x4000 7400 - 0x4000 77FF	1 K	DAC
	0x4000 7000 - 0x4000 73FF	1 K	PWR
	0x4000 6800 - 0x4000 6FFF	2 K	Reserved
	0x4000 6400 - 0x4000 67FF	1 K	bxCAN
	0x4000 6000 - 0x4000 63FF	1 K	USB/CAN SRAM
	0x4000 5C00 - 0x4000 5FFF	1 K	USB device FS
	0x4000 5800 - 0x4000 5BFF	1 K	I2C2
	0x4000 5400 - 0x4000 57FF	1 K	I2C1
	0x4000 5000 - 0x4000 53FF	1 K	UART5
	0x4000 4C00 - 0x4000 4FFF	1 K	UART4
	0x4000 4800 - 0x4000 4BFF	1 K	USART3
	0x4000 4400 - 0x4000 47FF	1 K	USART2
	0x4000 4000 - 0x4000 43FF	1 K	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	1 K	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	1 K	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 K	I2S2ext
	0x4000 3000 - 0x4000 33FF	1 K	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 K	WWDG
	0x4000 2800 - 0x4000 2BFF	1 K	RTC
	0x4000 1800 - 0x4000 27FF	4 K	Reserved
	0x4000 1000 - 0x4000 13FF	1 K	TIM6
	0x4000 0C00 - 0x4000 0FFF	1 K	Reserved
	0x4000 0800 - 0x4000 0BFF	1 K	TIM4
	0x4000 0400 - 0x4000 07FF	1 K	TIM3
	0x4000 0000 - 0x4000 03FF	1 K	TIM2

Table 17. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD_x power lines (source)	160	mA
ΣI_{VSS}	Total current out of sum of all VSS_x ground lines (sink)	-160	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	80	
	Total output current sourced by sum of all IOs and control pins(2)	-80	
$I_{INJ(PIN)}$	Injected current on FT, FTf, and B pins(3)	-5/+0	
	Injected current on TC and RST pin(4)	±5	
	Injected current on TTa pins(5)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS} and V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 16: Voltage characteristics* for the maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. I_{INJ}(PIN) must never be exceeded. Refer also to *Table 16: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note (2) below *Table 81*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 18. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	°C

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 38*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 38. HSE oscillator characteristics

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
I_{DD}	HSE current consumption	During startup(3)	-	-	8.5	mA
		V_{DD}= 3.3 V, Rm= 30Ω, CL=10 pF@8 MHz	-	0.4	-	
		V_{DD}= 3.3 V, Rm= 45Ω, CL=10 pF@8 MHz	-	0.5	-	
		V_{DD}= 3.3 V, Rm= 30Ω, CL=5 pF@32 MHz	-	0.8	-	
		V_{DD}= 3.3 V, Rm= 30Ω, CL=10 pF@32 MHz	-	1	-	
		V_{DD}= 3.3 V, Rm= 30Ω, CL=20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 17*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Table 50. Asynchronous multiplexed PSRAM/NOR read timings(1) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	2	ns
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	THCLK	-	
$t_{su(Data\_NOE)}$	Data to FMC_NOE high setup time	THCLK+1	-	
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. Based on characterization, not tested in production.

Figure 23. Asynchronous multiplexed PSRAM/NOR write timings

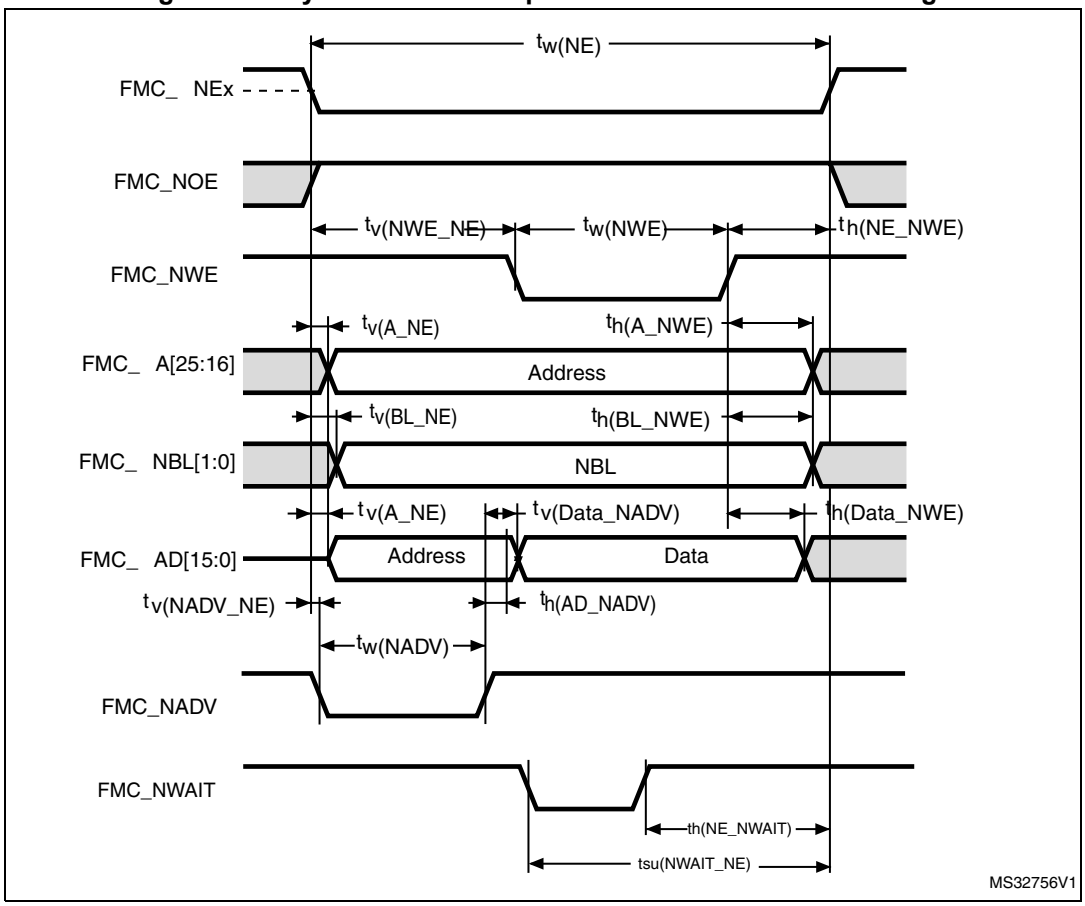


Table 51. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	4THCLK-1	4THCLK+1	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	THCLK	THCLK+0.5	
$t_{w(NWE)}$	FMC_NWE low time	2THCLK-0.5	2THCLK+1	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	THCLK-0.5	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	5	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	1	2.5	
$t_{w(NADV)}$	FMC_NADV low time	THCLK-2	THCLK+2	
$t_{h(AD\_NADV)}$	FMC_AD(adress) valid hold time after FMC_NADV high)	THCLK-2	-	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	THCLK-1	-	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	THCLK-0.5	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	1	
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	THCLK +3.5	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	THCLK +0.5	-	

1. Based on characterization, not tested in production.

Table 52. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	9THCLK	9THCLK+0.5	ns
$t_{w(NWE)}$	FMC_NWE low time	6THCLK	6THCLK+2	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	5THCLK+6	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	5THCLK-5	-	

1. Based on characterization, not tested in production.

Synchronous waveforms and timings

Figure 24 and *Figure 27* present the synchronous waveforms and *Table 53* to *Table 56* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable;
- MemoryType = FMC_MemoryType_CRAM;
- WriteBurst = FMC_WriteBurst_Enable;
- CLKDivision = 1;
- DataLatency = 2 for NOR Flash; DataLatency = 0 for PSRAM

In all timing tables, the THCLK is the HCLK clock period (with maximum FMC_CLK = 36 MHz).

Table 59. Switching characteristics for NAND Flash read cycles(1) (2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NOE)}$	FMC_NOE low width	6THCLK	6THCLK + 2	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	THCLK+5	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	6THCLK -0.5	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	6THCLK-1	-	

1. Based on characterization, not tested in production.
2. CL = 30 pF

Figure 35. NAND controller write timings

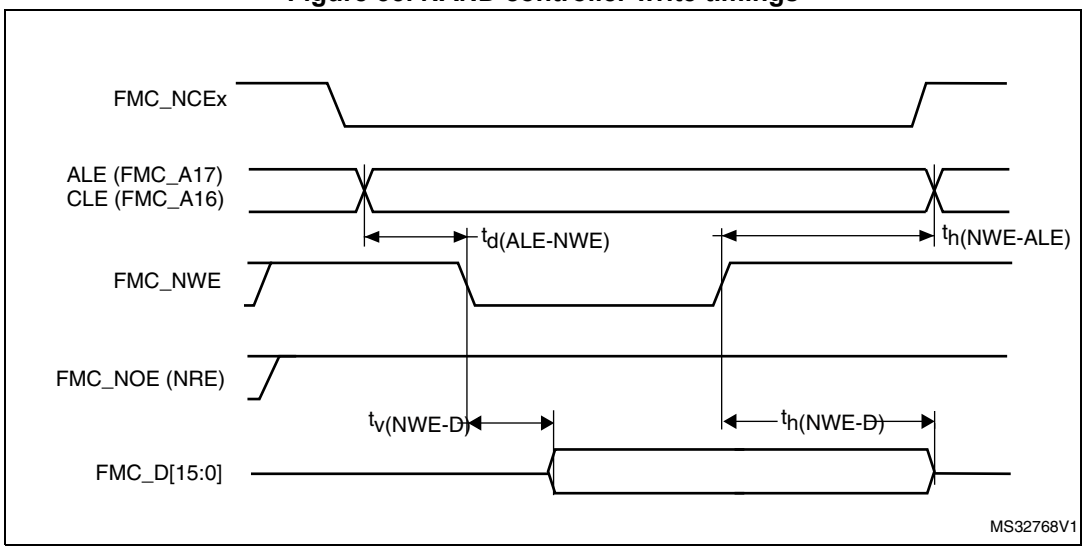


Table 60. Switching characteristics for NAND Flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	4THCLK-0.5	4THCLK + 1.5	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	-	3.5	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	3THCLK -1.5	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	5THCLK – 3	-	
$t_{d(ALE\_NWE)}$	FMC_ALE valid before FMC_NWE low	-	4THCLK+2	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	2THCLK-1	-	

1. Based on characterization, not tested in production.

Table 66. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{lkg}	Input leakage current (3)	TC, FT and FTf I/O TTa I/O in digital mode $V_{SS} \le V_{IN} \le V_{DD}$	-	-	±0.1	µA
		TTa I/O in digital mode $V_{DD} \le V_{IN} \le V_{DDA}$	-	-	1	
		TTa I/O in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$	-	-	±0.2	
		FT and FTf I/O(4) $V_{DD} \le V_{IN} \le 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation.
2. Tested in production.
3. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 65: I/O current injection susceptibility*.
4. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up/pull-down resistors must be disabled.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 36* and *Figure 37* for standard I/Os.

Figure 36. TC and TTa I/O input characteristics - CMOS port

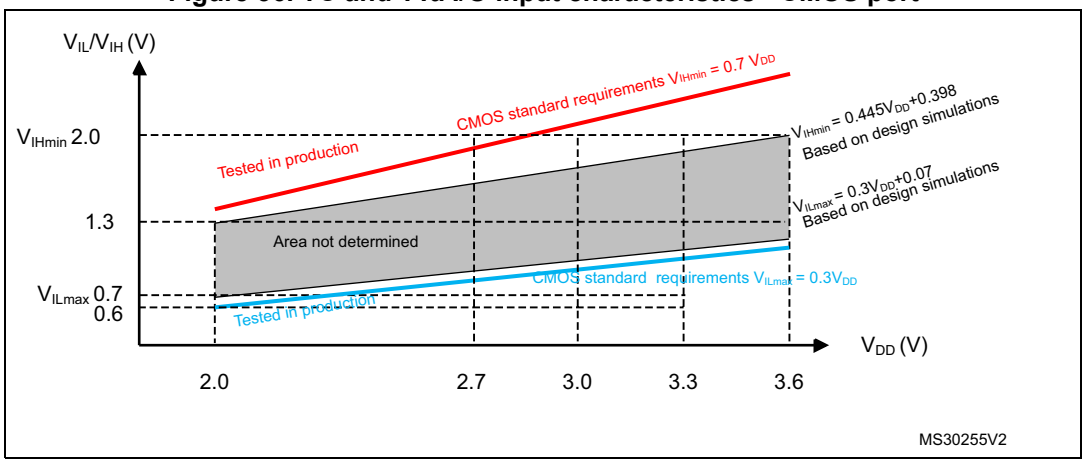
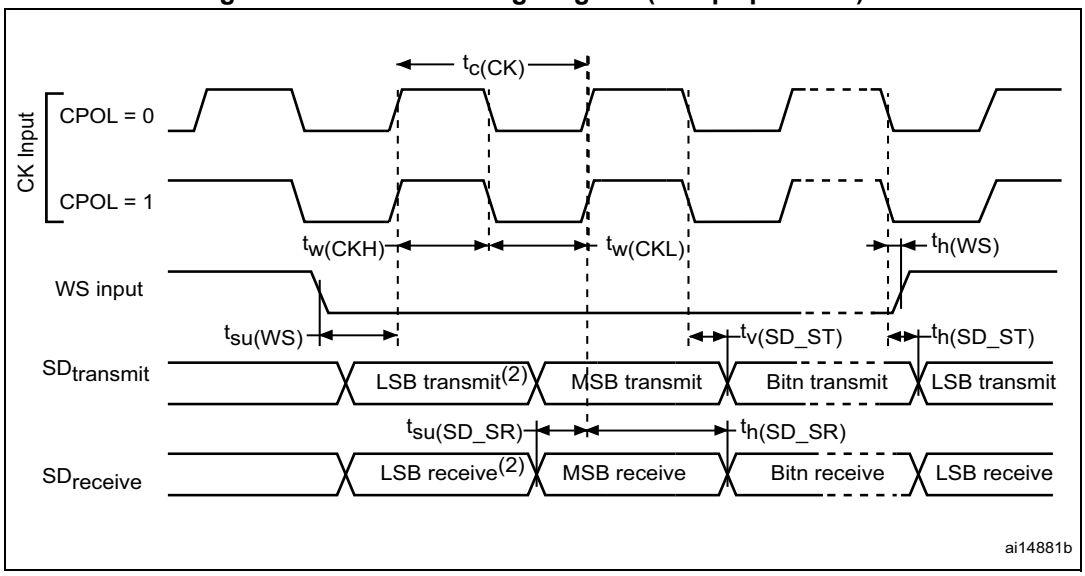
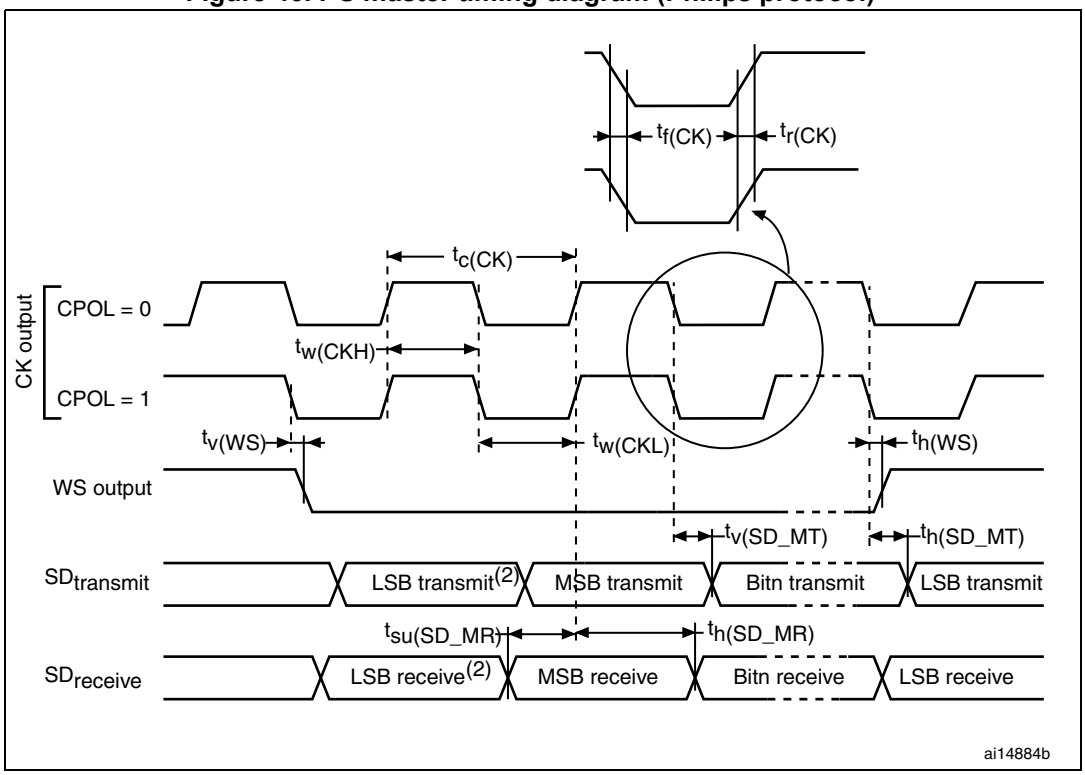


Figure 45. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at $0.5V_{DD}$ and with external C_L=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 46. I²S master timing diagram (Philips protocol)(1)

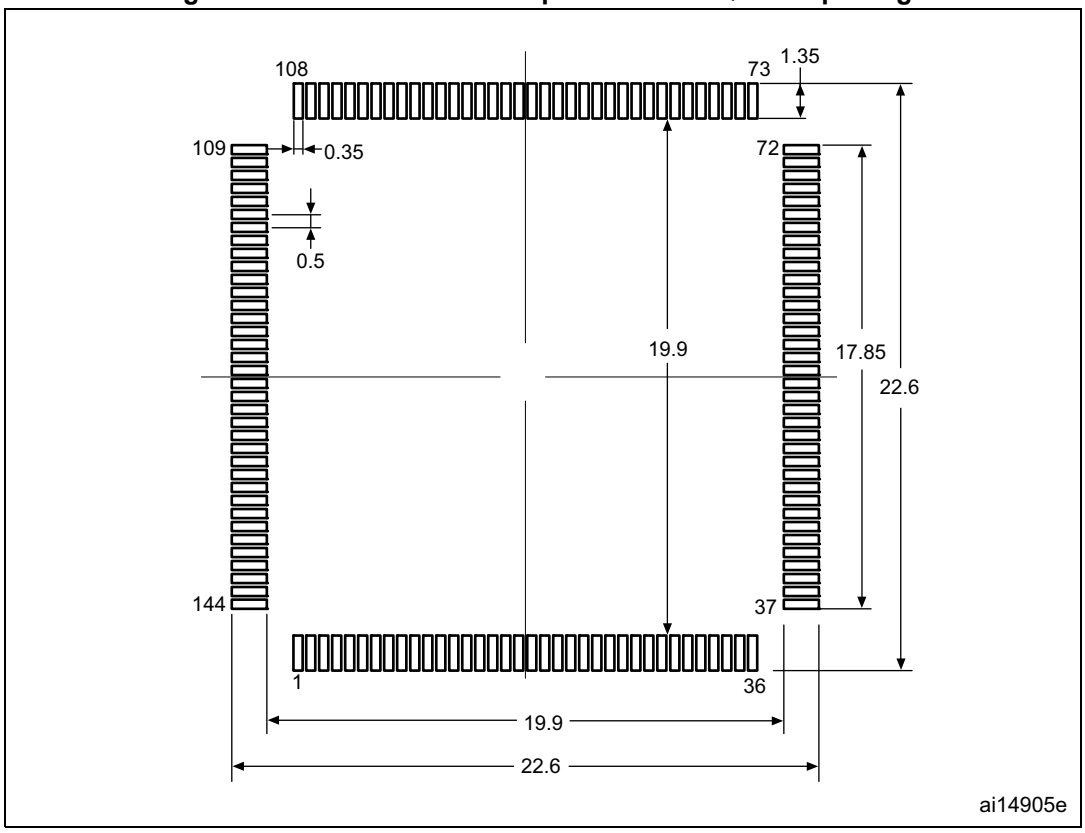


1. Measurement points are done at $0.5V_{DD}$ and with external C_L=30 pF.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Table 79. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{REF}	Current on VREF+ pin (see *Figure 49*)	Single-ended mode, 5 MSPS	-	104	139	µA
		Single-ended mode, 1 MSPS	-	20.4	37	
		Single-ended mode, 200 KSPS	-	3.3	11.3	
		Differential mode, 5 MSPS	-	174	235	
		Differential mode, 1 MSPS	-	34.6	52.6	
		Differential mode, 200 KSPS	-	6	13.6	
V_{REF+}	Positive reference voltage	-	2	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	-	0.14	-	72	MHz
f_S(1)	Sampling rate	Resolution = 12 bits, Fast Channel	0.01	-	5.14	MSPS
		Resolution = 10 bits, Fast Channel	0.012	-	6	
		Resolution = 8 bits, Fast Channel	0.014	-	7.2	
		Resolution = 6 bits, Fast Channel	0.0175	-	9	
f_{TRIG}(1)	External trigger frequency	f_{ADC} = 72 MHz Resolution = 12 bits	-	-	5.14	MHz
		Resolution = 12 bits	-	-	14	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(2)	-	0	-	V_{REF+}	V
R_{AIN}(1)	External input impedance	-	-	-	100	kΩ
C_{ADC}(1)	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}(1)	Power-up time	-	0	0	1	µs
t_{CAL}(1)	Calibration time	f_{ADC} = 72 MHz	1.56			µs
		-	112			$1/f_{ADC}$
t_{latr}(1)	Trigger conversion latency Regular and injected channels without conversion abort	CKMODE = 00	1.5	2	2.5	$1/f_{ADC}$
		CKMODE = 01	-	-	2	$1/f_{ADC}$
		CKMODE = 10	-	-	2.25	$1/f_{ADC}$
		CKMODE = 11	-	-	2.125	$1/f_{ADC}$
$t_{latrinj}$(1)	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3	$1/f_{ADC}$
		CKMODE = 10	-	-	3.25	$1/f_{ADC}$
		CKMODE = 11	-	-	3.125	$1/f_{ADC}$

Figure 55. Recommended footprint for the LQFP144 package



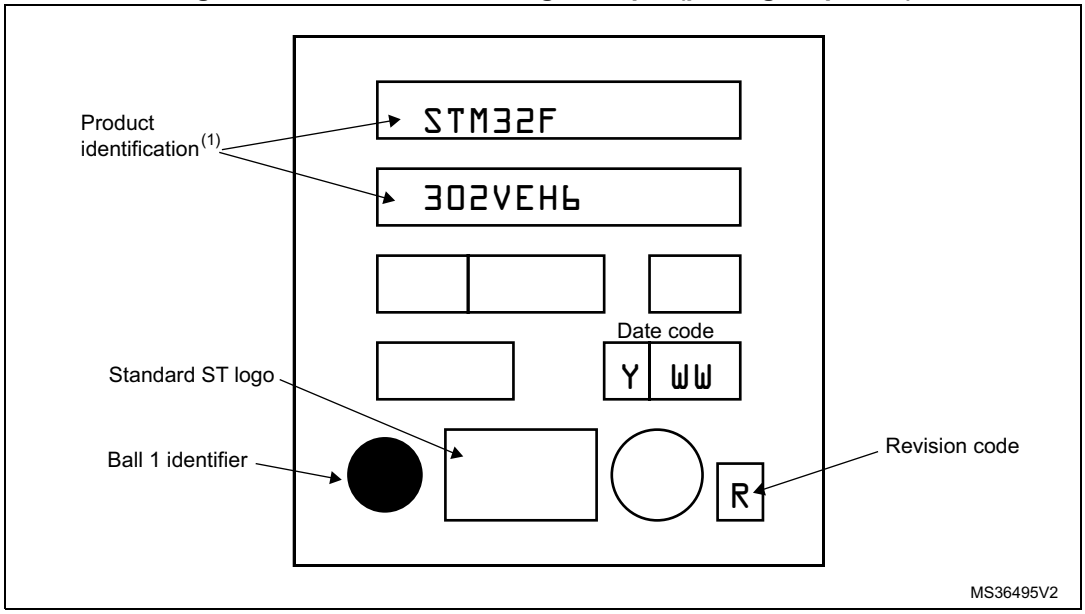
1. Drawing is not to scale.
2. Dimensions are expressed in millimeters.

Device marking for UFBGA100

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 59. UFBGA100 marking example (package top view)



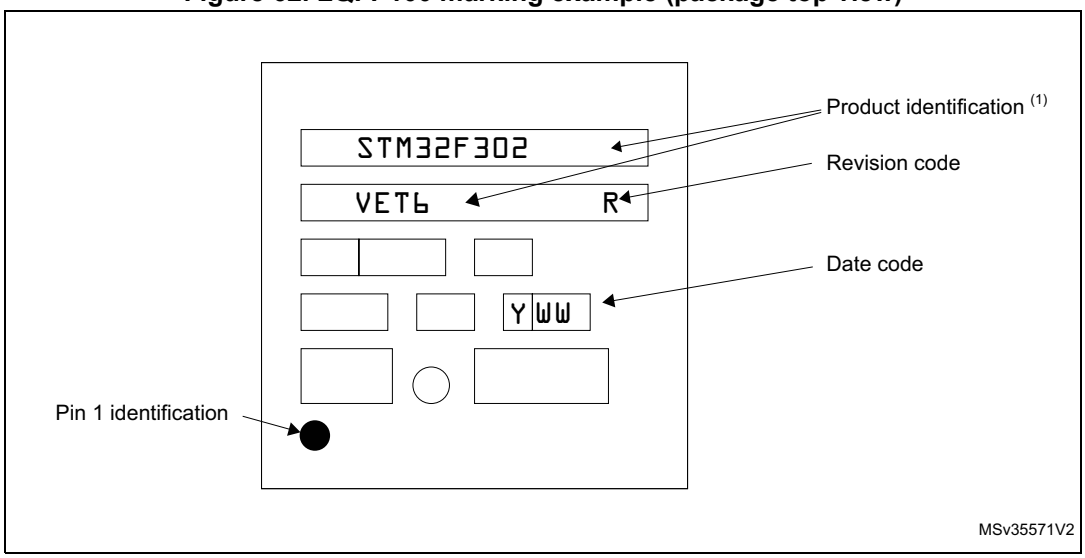
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Device marking for LQFP100

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 62. LQFP100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

8 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, contact the nearest ST sales office.

Table 100. Ordering information scheme

Example: STM32 F 302 V E T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

302 = STM32F302xx

Pin count

R = 64 pins

V = 100 pins

Z = 144 pins

Code size

D = 384 Kbytes of Flash memory

E = 512 Kbytes of Flash memory

Package

H = UFBGA

T = LQFP

Y = WLCSP

Temperature range

6 = –40 to 85 °C

7 = –40 to 105 °C

Options

xxx = programmed parts

TR = tape and reel