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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 86 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 17x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f302vet6tr |

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### 3.18.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

## 3.19 Real-time clock (RTC) and backup registers

The RTC and the 16 backup registers are supplied through a switch that takes power from either the $V_{DD}$ supply when present or the $V_{BAT}$ pin. The backup registers are sixteen 32-bit registers used to store 64 bytes of user application data when $V_{DD}$ power is not present.

They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Automatic correction for 28, 29 (leap year), 30 and 31 days of the month.
- Two programmable alarms with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.
- 17-bit Auto-reload counter for periodic interrupt with wakeup from STOP/STANDBY capability.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

## 3.20 Inter-integrated circuit interface ($I^2C$)

Up to three $I^2C$ bus interfaces can operate in multimaster and slave modes. They can support standard (up to 100 kHz), fast (up to 400 kHz) and fast mode + (up to 1 MHz) modes.

communication mode and have LIN Master/Slave capability. The USART interfaces can be served by the DMA controller.

## 3.22 Universal asynchronous receiver transmitter (UART)

The STM32F302xD/E devices have 2 embedded universal asynchronous receiver transmitters (UART4, and UART5). The UART interfaces support IrDA SIR ENDEC, multiprocessor communication mode and single-wire half-duplex communication mode. The UART4 interface can be served by the DMA controller.

Refer to *Table 8* for the features available in all U(S)ART interfaces.

**Table 8. USART features**

| USART modes/features(1) | USART1 | USART2 | USART3 | UART4 | UART5 |
|---|---|---|---|---|---|
| Hardware flow control for modem | X | X | X | - | - |
| Continuous communication using DMA | X | X | X | X | - |
| Multiprocessor communication | X | X | X | X | X |
| Synchronous mode | X | X | X | - | - |
| Smartcard mode | X | X | X | - | - |
| Single-wire half-duplex communication | X | X | X | X | X |
| IrDA SIR ENDEC block | X | X | X | X | X |
| LIN mode | X | X | X | X | X |
| Dual clock domain and wakeup from Stop mode | X | X | X | X | X |
| Receiver timeout interrupt | X | X | X | X | X |
| Modbus communication | X | X | X | X | X |
| Auto baud rate detection | X | X | X | - | - |
| Driver Enable | X | X | X | - | - |

1. X = supported.

## 3.23 Serial peripheral interface (SPI)/Inter-integrated sound interfaces ($I^2S$)

Up to four SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Two standard $I^2S$ interfaces (multiplexed with SPI2 and SPI3) supporting four different audio standards can operate as master or slave at half-duplex and full duplex communication modes. They can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

Refer to *Table 9* for the features available in SPI1, SPI2, SPI3 and SPI4.

Table 13. STM32F302xD/E pin definitions (continued)

| Pin number | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | WLCSP100 | LQFP144 | | | | | | |
| - | 82 | C3 | 115 | PD1 | I/O | FT | (1) | EVENTOUT, CAN_TX, FMC_D3 | - |
| 54 | 83 | A4 | 116 | PD2 | I/O | FT | - | EVENTOUT, TIM3_ETR, UART5_RX | - |
| - | 84 | B4 | 117 | PD3 | I/O | FT | (1) | EVENTOUT, TIM2_CH1/TIM2_ETR, USART2_CTS, FMC_CLK | - |
| - | 85 | C4 | 118 | PD4 | I/O | FT | (1) | EVENTOUT, TIM2_CH2, USART2_RTS, FMC_NOE | - |
| - | 86 | - | 119 | PD5 | I/O | FT | (1) | EVENTOUT, USART2_TX, FMC_NWE | - |
| - | - | - | 120 | VSS | S | - | (1) | - | - |
| - | - | - | 121 | VDD | S | - | (1) | - | - |
| - | 87 | - | 122 | PD6 | I/O | FT | (1) | EVENTOUT, TIM2_CH4, USART2_RX, FMC_NWAIT | - |
| - | 88 | D4 | 123 | PD7 | I/O | FT | (1) | EVENTOUT, TIM2_CH3, USART2_CK, FMC_NE1/FMC_NCE2 | - |
| - | - | - | 124 | PG9 | I/O | FT | (1) | EVENTOUT, FMC_NE2/FMC_NCE3 | - |
| - | - | - | 125 | PG10 | I/O | FT | (1) | EVENTOUT, FMC_NCE4_1/FMC_NE3 | - |
| - | - | - | 126 | PG11 | I/O | FT | (1) | EVENTOUT, FMC_NCE4_2 | - |
| - | - | - | 127 | PG12 | I/O | FT | (1) | EVENTOUT, FMC_NE4 | - |
| - | - | - | 128 | PG13 | I/O | FT | (1) | EVENTOUT, FMC_A24 | - |
| - | - | - | 129 | PG14 | I/O | FT | (1) | EVENTOUT, FMC_A25 | - |
| - | - | - | 130 | VSS | S | - | (1) | - | - |
| - | - | - | 131 | VDD | S | - | (1) | - | - |
| - | - | - | 132 | PG15 | I/O | FT | (1) | EVENTOUT | - |

**Table 14. STM32F302xD/E alternate function mapping (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS_AF | TIM2/15/16/17/EVENT | I2C3/TIM1/2/3/4/8/20/15/GPCOMP1 | I2C3//15/TSC | I2C1/2/TIM1/8/16/17 | SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/Infrared | SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared | USART1/2/3/CAN/GPCOMP6 | I2C3/GPCOMP1/2/3/4/5/6 | CAN/TIM1/8/15 | TIM2/3/4/8/17 | TIM1/8 | FSMC/TIM1 | - | - | EVENT |
| Port E | PE12 | - | EVENT OUT | TIM1_CH3N | - | - | SPI4_SCK | - | - | - | - | - | - | FMC_D9 | - | - | - |
| | PE13 | - | EVENT OUT | TIM1_CH3 | - | - | SPI4_MISO | - | - | - | - | - | - | FMC_D10 | - | - | - |
| | PE14 | - | EVENT OUT | TIM1_CH4 | - | - | SPI4_MOSI | TIM1_BKIN2 | - | - | - | - | - | FMC_D11 | - | - | - |
| | PE15 | - | EVENT OUT | TIM1_BKIN | - | - | - | - | USART3_RX | - | - | - | - | FMC_D12 | - | - | - |
| Port F | PF0 | - | EVENT OUT | - | - | I2C2_SDA | SPI2_NSS/I2S2_WS | TIM1_CH3N | - | - | - | - | - | - | - | - | - |
| | PF1 | - | EVENT OUT | - | - | I2C2_SCL | SPI2_SCK/I2S2_CK | - | - | - | - | - | - | - | - | - | - |
| | PF2 | - | EVENT OUT | - | - | - | - | - | - | - | - | - | - | FMC_A2 | - | - | - |
| | PF3 | - | EVENT OUT | - | - | - | - | - | - | - | - | - | - | FMC_A3 | - | - | - |
| | PF4 | - | EVENT OUT | COMP1_OUT | - | - | - | - | - | - | - | - | - | FMC_A4 | - | - | - |
| | PF5 | - | EVENT OUT | - | - | - | - | - | - | - | - | - | - | FMC_A5 | - | - | - |
| | PF6 | - | EVENT OUT | TIM4_CH4 | - | I2C2_SCL | - | - | USART3_RTS | - | - | - | - | FMC_NIORD | - | - | - |
| | PF7 | - | EVENT OUT | - | - | - | - | - | - | - | - | - | - | FMC_NREG | - | - | - |

**Table 14. STM32F302xD/E alternate function mapping (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS_AF | TIM2/15/16/17/EVENT | I2C3/TIM1/2/3/4/8/20/15/GPCOMP1 | I2C3//15/TSC | I2C1/2/TIM1/8/16/17 | SPI1/SPI2/I2S2/SPI3/I2S3/SPI4/UART4/5/Infrared | SPI2/I2S2/SPI3/I2S3/TIM1/8/20/Infrared | USART1/2/3/CAN/GPCOMP6 | I2C3/GPCOMP1/2/3/4/5/6 | CAN/TIM1/8/15 | TIM2/3/4/8/17 | TIM1/8 | FSMC/TIM1 | - | - | EVENT |
| Port G | PG5 | - | EVENT OUT | - | - | - | - | - | - | - | - | - | - | FMC_A15 | - | - | - |
| | PG6 | - | EVENT OUT | - | - | - | - | - | - | - | - | - | - | FMC_INT2 | - | - | - |
| | PG7 | - | EVENT OUT | - | - | - | - | - | - | - | - | - | - | FMC_INT3 | - | - | - |
| | PG8 | - | EVENT OUT | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| | PG9 | - | EVENT OUT | - | - | - | - | - | - | - | - | - | - | FMC_NE2/FMC_NCE3 | - | - | - |
| | PG10 | - | EVENT OUT | - | - | - | - | - | - | - | - | - | - | FMC_NCE4_1/FMC_NE3 | - | - | - |
| | PG11 | - | EVENT OUT | - | - | - | - | - | - | - | - | - | - | FMC_NCE4_2 | - | - | - |
| | PG12 | - | EVENT OUT | - | - | - | - | - | - | - | - | - | - | FMC_NE4 | - | - | - |
| | PG13 | - | EVENT OUT | - | - | - | - | - | - | - | - | - | - | FMC_A24 | - | - | - |
| | PG14 | - | EVENT OUT | - | - | - | - | - | - | - | - | - | - | FMC_A25 | - | - | - |
| | PG15 | - | EVENT OUT | - | - | - | - | - | - | - | - | - | - | - | - | - | - |

**Table 32. Switching output I/O current consumption**

| Symbol | Parameter | Conditions[1] | I/O toggling frequency ($f_{SW}$) | Typ | Unit |
|---|---|---|---|---|---|
| $I_{SW}$ | I/O current consumption | $V_{DD}$ = 3.3 V<br>$C_{ext}$ = 0 pF<br>$C = C_{INT} + C_{EXT} + C_S$ | 2 MHz | 0.90 | mA |
| | | | 4 MHz | 0.93 | |
| | | | 8 MHz | 1.16 | |
| | | | 18 MHz | 1.60 | |
| | | | 36 MHz | 2.51 | |
| | | | 48 MHz | 2.97 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{ext}$ = 10 pF<br>$C = C_{INT} + C_{EXT} + C_S$ | 2 MHz | 0.93 | |
| | | | 4 MHz | 1.06 | |
| | | | 8 MHz | 1.47 | |
| | | | 18 MHz | 2.26 | |
| | | | 36 MHz | 3.39 | |
| | | | 48 MHz | 5.99 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{ext}$ = 22 pF<br>$C = C_{INT} + C_{EXT} + C_S$ | 2 MHz | 1.03 | |
| | | | 4 MHz | 1.30 | |
| | | | 8 MHz | 1.79 | |
| | | | 18 MHz | 3.01 | |
| | | | 36 MHz | 5.99 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{ext}$ = 33 pF<br>$C = C_{INT} + C_{EXT} + C_S$ | 2 MHz | 1.10 | |
| | | | 4 MHz | 1.31 | |
| | | | 8 MHz | 2.06 | |
| | | | 18 MHz | 3.47 | |
| | | | 36 MHz | 8.35 | |
| | | $V_{DD}$ = 3.3 V<br>$C_{ext}$ = 47 pF<br>$C = C_{INT} + C_{EXT} + C_S$ | 2 MHz | 1.20 | |
| | | | 4 MHz | 1.54 | |
| | | | 8 MHz | 2.46 | |
| | | | 18 MHz | 4.51 | |
| | | | 36 MHz | 9.98 | |

1. CS = 5 pF (estimated value).

**Table 50. Asynchronous multiplexed PSRAM/NOR read timings(1) (continued)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{v(BL\_NE)}$ | FMC_NEx low to FMC_BL valid | - | 2 | ns |
| $t_{su(Data\_NE)}$ | Data to FMC_NEx high setup time | THCLK | - | |
| $t_{su(Data\_NOE)}$ | Data to FMC_NOE high setup time | THCLK+1 | - | |
| $t_{h(Data\_NE)}$ | Data hold time after FMC_NEx high | 0 | - | |
| $t_{h(Data\_NOE)}$ | Data hold time after FMC_NOE high | 0 | - | |

1. Based on characterization, not tested in production.

**Figure 23. Asynchronous multiplexed PSRAM/NOR write timings**

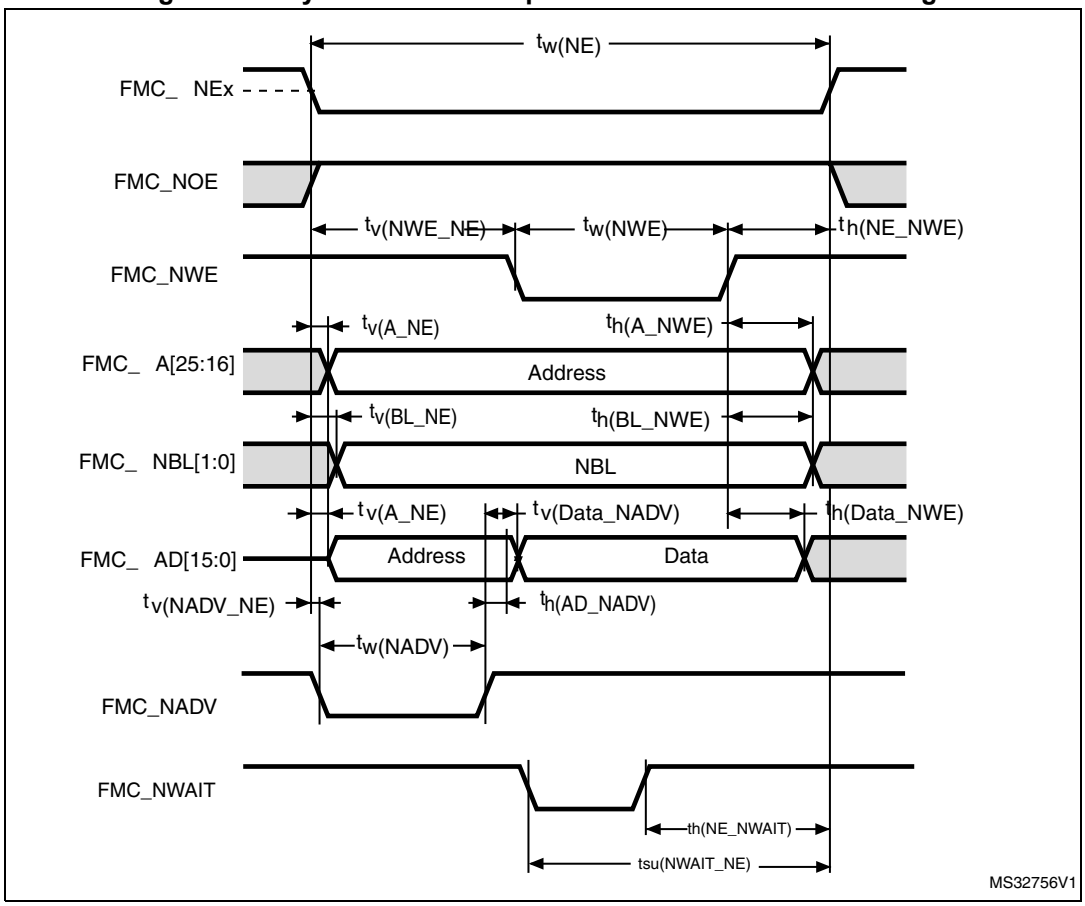


**Figure 26. Synchronous non-multiplexed NOR/PSRAM read timings**

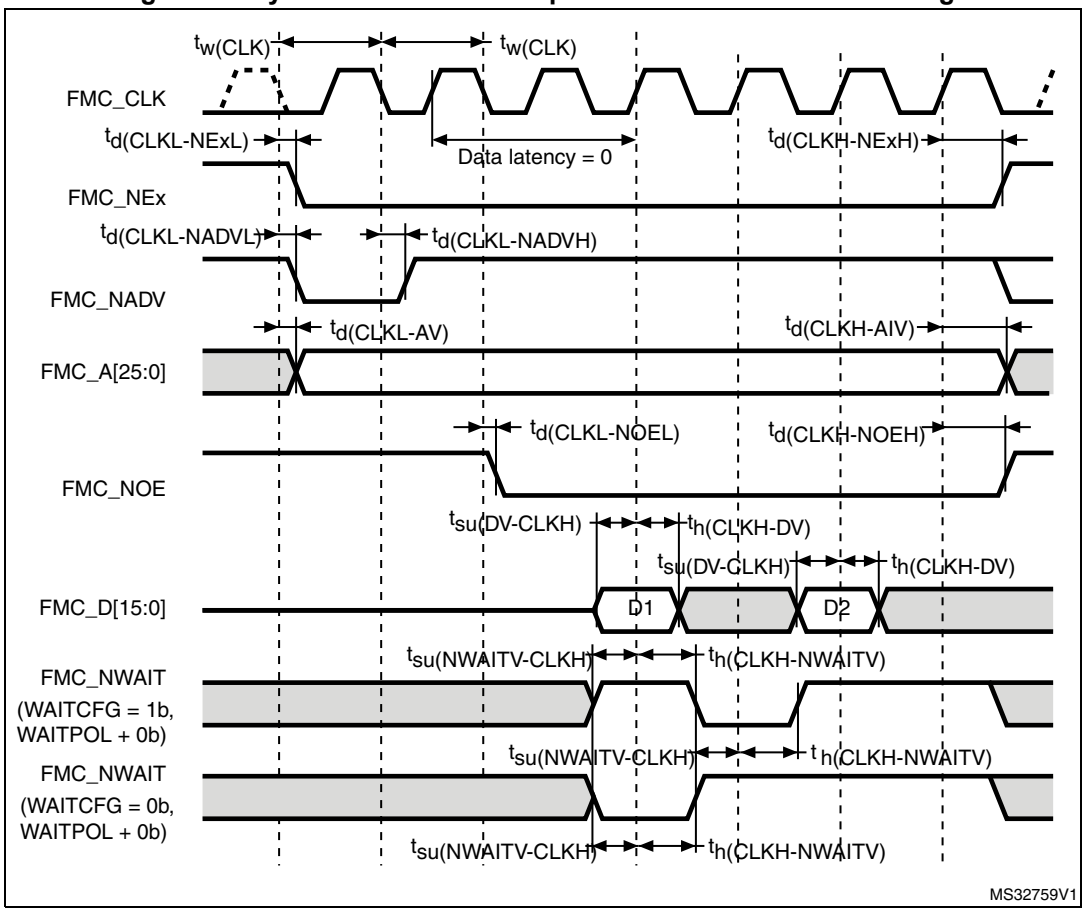
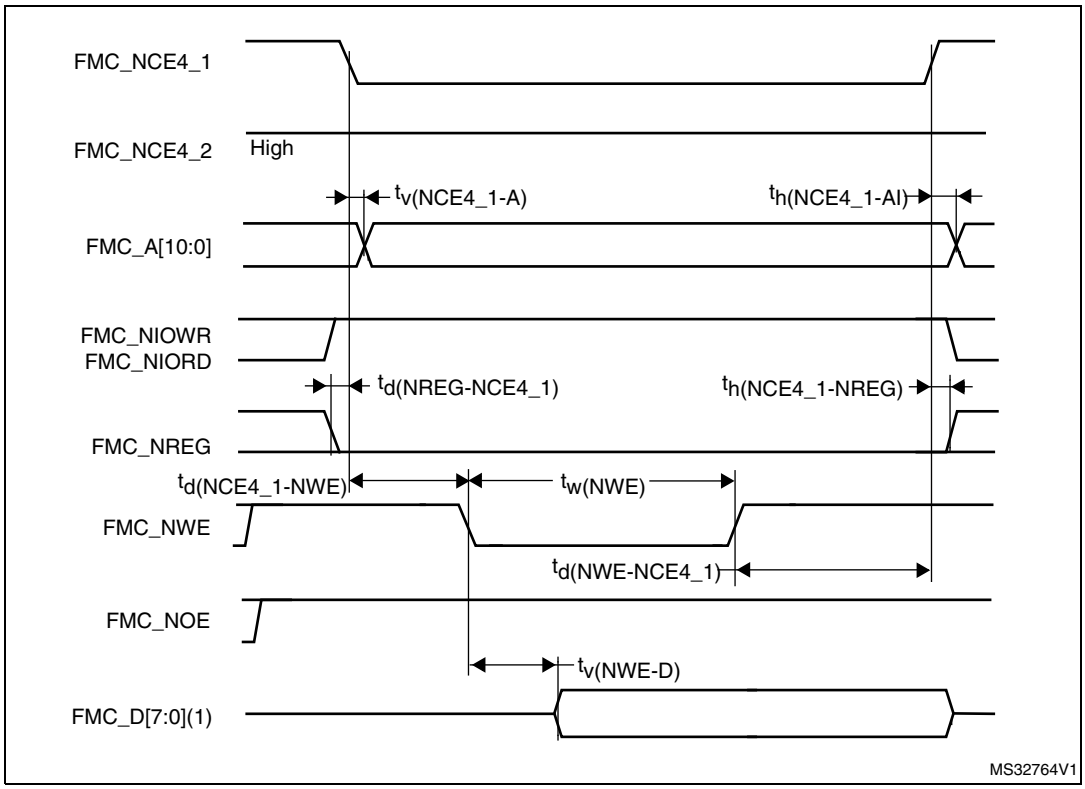



**Table 55. Synchronous non-multiplexed NOR/PSRAM read timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | FMC_CLK period | 2THCLK-1 | - | ns |
| $t_{d(CLKL-NExL)}$ | FMC_CLK low to FMC_NEx low (x=0..2) | - | 5 | |
| $t_{d(CLKH-NExH)}$ | FMC_CLK high to FMC_NEx high (x= 0…2) | THCLK+1 | - | |
| $t_{d(CLKL-NADVL)}$ | FMC_CLK low to FMC_NADV low | - | 7 | |
| $t_{d(CLKL-NADVH)}$ | FMC_CLK low to FMC_NADV high | 2.5 | - | |
| $t_{d(CLKL-AV)}$ | FMC_CLK low to FMC_Ax valid (x=16…25) | - | 7 | |
| $t_{d(CLKH-AIV)}$ | FMC_CLK high to FMC_Ax invalid (x=16…25) | THCLK | - | |
| $t_{d(CLKL-NOEL)}$ | FMC_CLK low to FMC_NOE low | - | 6 | |
| $t_{d(CLKH-NOEH)}$ | FMC_CLK high to FMC_NOE high | THCLK+1 | - | |
| $t_{su(DV-CLKH)}$ | FMC_D[15:0] valid data before FMC_CLK high | 3.5 | - | |

**Figure 31. PC Card/CompactFlash controller waveforms for attribute memory write access**




1. Only data bits 0...7 are driven (bits 8...15 remains Hi-Z).

**Table 58. Switching characteristics for PC Card/CF read and write cycles in I/O space(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NIOWR)}$ | FMC_NIOWR low width | 8THCLK-0.5 | - | ns |
| $t_{v(NIOWR-D)}$ | FMC_NIOWR low to FMC_D[15:0] valid | - | 5.5 | |
| $t_{h(NIOWR-D)}$ | FMC_NIOWR high to FMC_D[15:0] invalid | 4THCLK-0.5 | - | |
| $t_{d(NCE4\_1-NIOWR)}$ | FMC_NCE4_1 low to FMC_NIOWR valid | - | 5THCLK+1 | |
| $t_{h(NCEx-NIOWR)}$ | FMC_NCEx high to FMC_NIOWR invalid | 4THCLK+0.5 | - | |
| $t_{d(NIORD-NCEx)}$ | FMC_NCEx low to FMC_NIORD valid | - | 5THCLK | |
| $t_{h(NCEx-NIORD)}$ | FMC_NCEx high to FMC_NIORD) valid | 6THCLK+2 | - | |
| $t_{w(NIORD)}$ | FMC_NIORD low width | 8THCLK-1 | 8THCLK+1 | |
| $t_{su(D-NIORD)}$ | FMC_D[15:0] valid before FMC_NIORD high | THCLK+2 | - | |
| $t_{d(NIORD-D)}$ | FMC_D[15:0] valid after FMC_NIORD high | 0 | - | |

1. Based on characterization, not tested in production.

**Table 65. I/O current injection susceptibility (continued)**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on PB0, PB1, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15, PB12, PB13, PB14, P15, PD8, PD9, PD10, PD11, PD12, PD13, PD14 with induced leakage current on other pins from this group less than -50 µA or more than +400 µA | -5 | +5 | mA |
| | Injected current on any other FT and FTf pins | -5 | NA | |
| | Injected current on any other pins | -5 | +5 | |

*Note: It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*

## 6.3.15 I/O port characteristics

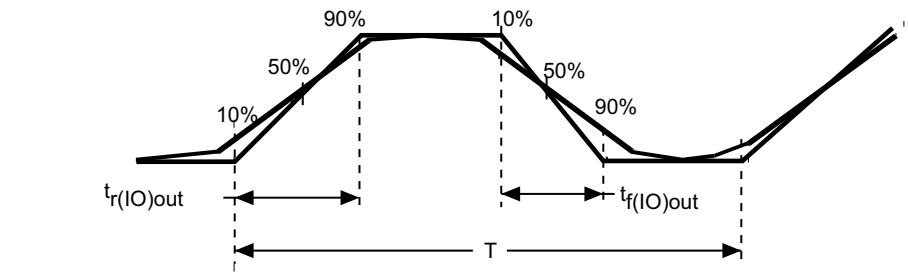
### General input/output characteristics

Unless otherwise specified, the parameters given in *Table 66* are derived from tests performed under the conditions summarized in *Table 19*. All I/Os are CMOS and TTL compliant.

**Table 66. I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low level input voltage | TC and TTa I/O | - | - | $0.3\ V_{DD}+0.07$ (1) | V |
| | | FT and FTf I/O | - | - | $0.475\ V_{DD}-0.2$ (1) | |
| | | BOOT0 | - | - | $0.3\ V_{DD}-0.3$ (1) | |
| | | All I/Os except BOOT0 | - | - | $0.3\ V_{DD}$ (2) | |
| $V_{IH}$ | High level input voltage | TC and TTa I/O | $0.445\ V_{DD}+0.398$ (1) | - | - | V |
| | | FT and FTf I/O | $0.5\ V_{DD}+0.2$ (1) | - | - | |
| | | BOOT0 | $0.2\ V_{DD}+0.95$ (1) | - | - | |
| | | All I/Os except BOOT0 | $0.7\ V_{DD}$ (2) | - | - | |
| $V_{hys}$ | Schmitt trigger hysteresis | TC and TTa I/O | - | 200 (1) | - | mV |
| | | FT and FTf I/O | - | 100 (1) | - | |
| | | BOOT0 | - | 300 (1) | - | |

**Figure 40. I/O AC characteristics definition**




Maximum frequency is achieved if $(t_r + t_f) \le 2/3)T$ and if the duty cycle is (45-55%) when loaded by $C_L$ (1)

MS36445V1

1. See *Table 68: I/O AC characteristics*.

## 6.3.16 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see *Table 66*).

Unless otherwise specified, the parameters given in *Table 69* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 19*.

**Table 69. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$ (1) | NRST Input low level voltage | - | - | - | $0.3V_{DD}+0.07$ (1) | V |
| $V_{IH(NRST)}$ (1) | NRST Input high level voltage | - | $0.445V_{DD}+0.398$ (1) | - | - | |
| $V_{hys(NRST)}$ | NRST Schmitt trigger voltage hysteresis | - | - | 200 | - | mV |
| $R_{PU}$ | Weak pull-up equivalent resistor (2) | $V_{IN} = V_{SS}$ | 25 | 40 | 55 | kΩ |
| $V_{F(NRST)}$ (1) | NRST Input filtered pulse | - | - | - | 100 (1) | ns |
| $V_{NF(NRST)}$ (1) | NRST Input not filtered pulse | - | 500 (1) | - | - | ns |

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

**Table 71. IWDG min/max timeout period at 40 kHz (LSI) (1)**

| Prescaler divider | PR[2:0] bits | Min timeout (ms) RL[11:0]= 0x000 | Max timeout (ms) RL[11:0]= 0xFFF |
|---|---|---|---|
| /4 | 0 | 0.1 | 409.6 |
| /8 | 1 | 0.2 | 819.2 |
| /16 | 2 | 0.4 | 1638.4 |
| /32 | 3 | 0.8 | 3276.8 |
| /64 | 4 | 1.6 | 6553.6 |
| /128 | 5 | 3.2 | 13107.2 |
| /256 | 7 | 6.4 | 26214.4 |

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

**Table 72. WWDG min-max timeout value @72 MHz (PCLK)(1)**

| Prescaler | WDGTB | Min timeout value | Max timeout value |
|---|---|---|---|
| 1 | 0 | 0.05687 | 3.6409 |
| 2 | 1 | 0.1137 | 7.2817 |
| 4 | 2 | 0.2275 | 14.564 |
| 8 | 3 | 0.4551 | 29.127 |

1. Guaranteed by design, not tested in production.

## 6.3.18 Communications interfaces

### I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev.03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1Mbits/s

The I²C timings requirements are guaranteed by design when the I²C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.15: I/O port characteristics*.

All I²C I/Os embed an analog filter, refer to the *Table 73: I2C analog filter characteristics*.

**Table 74. SPI characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{v(SO)}$ | Data output valid time | Slave mode 2.7 V<$V_{DD}$<3.6 V | - | 15 | 22 | |
| | | Slave mode 2 V<$V_{DD}$<3.6 V | - | 15 | 30 | |
| $t_{v(MO)}$ | | Master mode | - | 2 | 4.5 | |
| $t_{h(SO)}$ | Data output hold time | Slave mode | 9 | - | - | |
| $t_{h(MO)}$ | | Master mode | 0 | - | - | |

1. Data based on characterization results, not tested in production.
2. The maximum frequency in Slave transmitter mode is determined by the sum of tv(SO) and tsu(MI) which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having tsu(MI) = 0 while $Duty_{(SCK)}$ = 50%.

**Figure 42. SPI timing diagram - slave mode and CPHA = 0**

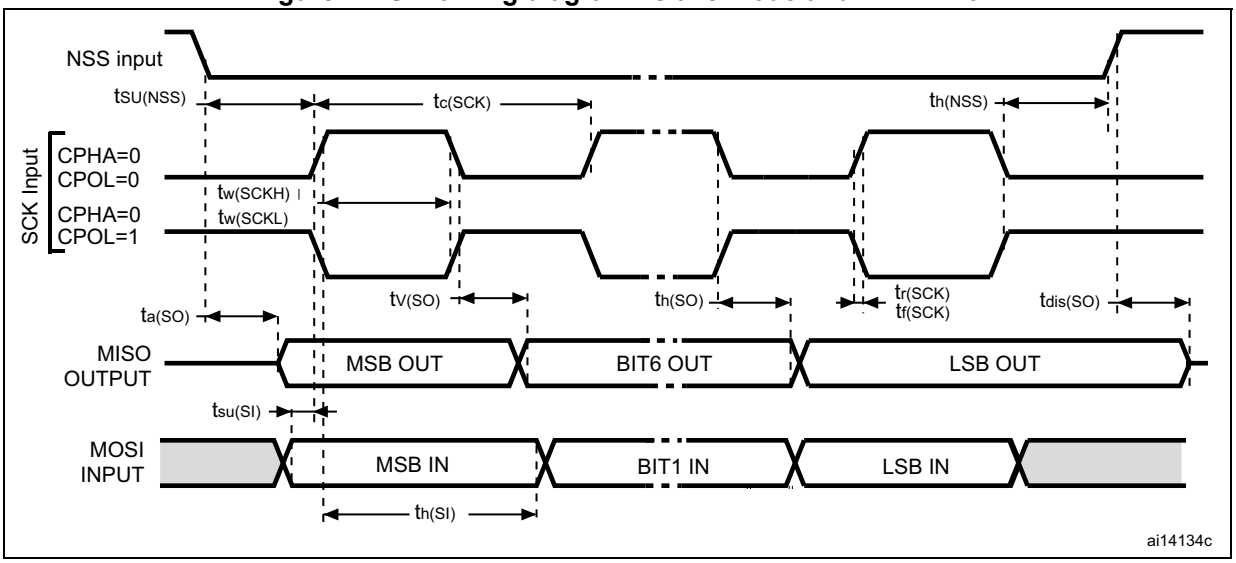


**Table 79. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_S$(1) | Sampling time | $f_{ADC}$ = 72 MHz | 0.021 | - | 8.35 | µs |
| | | - | 1.5 | - | 601.5 | $1/f_{ADC}$ |
| $T_{ADCVREG\_STUP}$(1) | ADC Voltage Regulator Start-up time | - | - | - | 10 | µs |
| $t_{CONV}$(1) | Total conversion time (including sampling time) | $f_{ADC}$ = 72 MHz Resolution = 12 bits | 0.19 | - | 8.52 | µs |
| | | Resolution = 12 bits | 14 to 614 ($t_S$ for sampling + 12.5 for successive approximation) | | | $1/f_{ADC}$ |
| CMIR | Common Mode Input signal range | ADC differential mode | ($V_{SSA}$ + $V_{REF}$+)/2 – 0.18 | ($V_{SSA}$ + $V_{REF}$+)/2 | ($V_{SSA}$ + $V_{REF}$+)/2 + 0.18 | V |

1. Data guaranteed by design, not tested in Production.
2. $V_{REF+}$ can be internally connected to $V_{DDA}$ and $V_{REF-}$ can be internally connected to $V_{SSA}$, depending on the package. Refer to *Section 4: Pinout and pin description* for further details.

**Figure 48. ADC typical current consumption on VDDA pin**

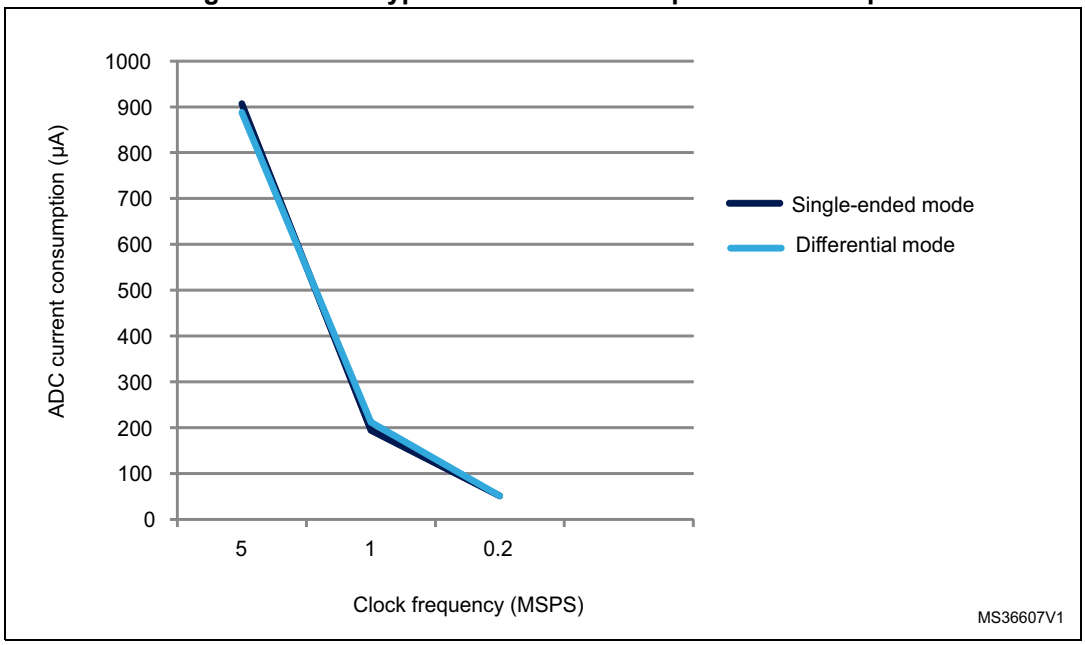


**Table 83. ADC accuracy - limited test conditions, 64-pin packages(1)(2)**

| Symbol | Parameter | Conditions | | | Min (3) | Typ | Max (3) | Unit |
|---|---|---|---|---|---|---|---|---|
| ET | Total unadjusted error | ADC clock freq. ≤ 72 MHz<br>Sampling freq. ≤ 5 Msps<br>$V_{DDA}$ = 3.3 V<br>25°C<br>64-pin package | Single ended | Fast channel 5.1 Ms | - | ±4 | ±4.5 | LSB |
| | | | | Slow channel 4.8 Ms | - | ±5.5 | ±6 | |
| | | | Differential | Fast channel 5.1 Ms | - | ±3.5 | ±4 | |
| | | | | Slow channel 4.8 Ms | - | ±3.5 | ±4 | |
| EO | Offset error | | Single ended | Fast channel 5.1 Ms | - | ±2 | ±2 | |
| | | | | Slow channel 4.8 Ms | - | ±1.5 | ±2 | |
| | | | Differential | Fast channel 5.1 Ms | - | ±1.5 | ±2 | |
| | | | | Slow channel 4.8 Ms | - | ±1.5 | ±2 | |
| EG | Gain error | | Single ended | Fast channel 5.1 Ms | - | ±3 | ±4 | |
| | | | | Slow channel 4.8 Ms | - | ±5 | ±5.5 | |
| | | | Differential | Fast channel 5.1 Ms | - | ±3 | ±3 | |
| | | | | Slow channel 4.8 Ms | - | ±3 | ±3.5 | |
| ED | Differential linearity error | | Single ended | Fast channel 5.1 Ms | - | ±1 | ±1 | |
| | | | | Slow channel 4.8 Ms | - | ±1 | ±1 | |
| | | | Differential | Fast channel 5.1 Ms | - | ±1 | ±1 | |
| | | | | Slow channel 4.8 Ms | - | ±1 | ±1 | |
| EL | Integral linearity error | | Single ended | Fast channel 5.1 Ms | - | ±1.5 | ±2 | |
| | | | | Slow channel 4.8 Ms | - | ±2 | ±3 | |
| | | | Differential | Fast channel 5.1 Ms | - | ±1.5 | ±1.5 | |
| | | | | Slow channel 4.8 Ms | - | ±1.5 | ±2 | |
| ENOB (4) | Effective number of bits | | Single ended | Fast channel 5.1 Ms | 10.8 | 10.8 | - | bit |
| | | | | Slow channel 4.8 Ms | 10.8 | 10.8 | - | |
| | | | Differential | Fast channel 5.1 Ms | 11.2 | 11.3 | - | |
| | | | | Slow channel 4.8 Ms | 11.2 | 11.3 | - | |
| SINAD (4) | Signal-to-noise and distortion ratio | | Single ended | Fast channel 5.1 Ms | 66 | 67 | - | dB |
| | | | | Slow channel 4.8 Ms | 66 | 67 | - | |
| | | | Differential | Fast channel 5.1 Ms | 69 | 70 | - | |
| | | | | Slow channel 4.8 Ms | 69 | 70 | - | |

**Table 87. Comparator characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $TV_{OFFSET}$ | Total offset variation | Full temperature range | - | - | 3 | mV |
| $I_{DDA}$ | COMP current consumption | - | - | 400 | 600 | µA |

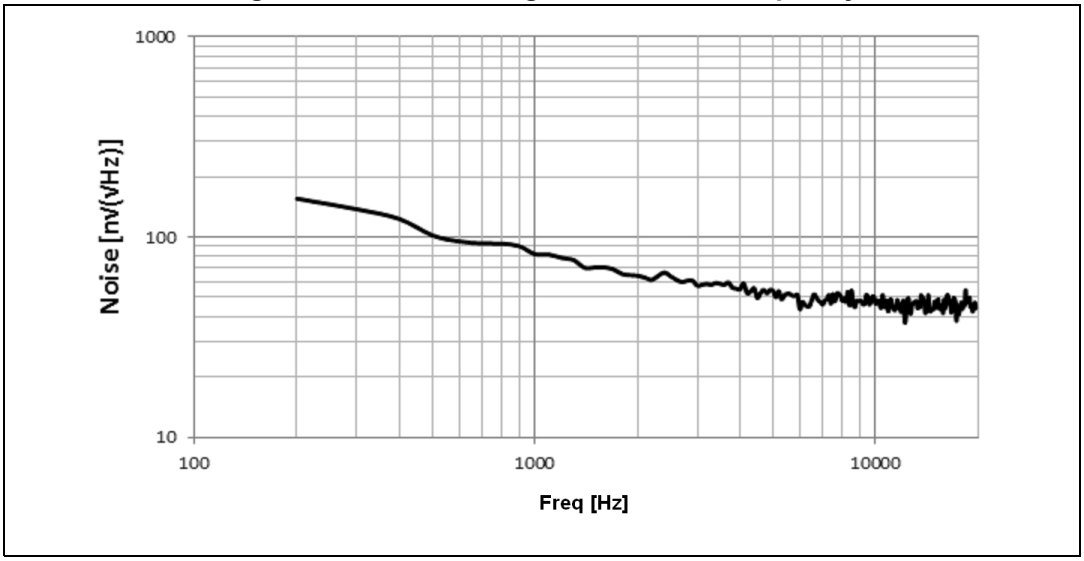
1. Guaranteed by design, not tested in production.

**Table 88. Operational amplifier characteristics(1) (continued)**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| PGA gain | Non inverting gain value | - | - | 2 | - | - |
| | | | - | 4 | - | - |
| | | | - | 8 | - | - |
| | | | - | 16 | - | - |
| $R_{network}$ | R2/R1 internal resistance values in PGA mode (3) | Gain=2 | - | 5.4/5.4 | - | kΩ |
| | | Gain=4 | - | 16.2/5.4 | - | |
| | | Gain=8 | - | 37.8/5.4 | - | |
| | | Gain=16 | - | 40.5/2.7 | - | |
| PGA gain error | PGA gain error | - | -1% | - | 1% | - |
| $I_{bias}$ | OPAMP input bias current | - | - | - | ±0.2(4) | µA |
| PGA BW | PGA bandwidth for different non inverting gain | PGA Gain = 2, Cload = 50pF, Rload = 4 KΩ | - | 4 | - | MHz |
| | | PGA Gain = 4, Cload = 50pF, Rload = 4 KΩ | - | 2 | - | |
| | | PGA Gain = 8, Cload = 50pF, Rload = 4 KΩ | - | 1 | - | |
| | | PGA Gain = 16, Cload = 50pF, Rload = 4 KΩ | - | 0.5 | - | |
| en | Voltage noise density | @ 1KHz, Output loaded with 4 KΩ | - | 109 | - | $\frac{nV}{\sqrt{Hz}}$ |
| | | @ 10KHz, Output loaded with 4 KΩ | - | 43 | - | |

1. Guaranteed by design, not tested in production.
2. The saturation voltage can be also limited by the Iload (drive current).
3. R2 is the internal resistance between OPAMP output and OPAMP inverting input.
   R1 is the internal resistance between OPAMP inverting input and ground.
   The PGA gain =1+R2/R1
4. Mostly TTa I/O leakage, when used in analog mode.

Figure 53. OPAMP voltage noise versus frequency




## 6.3.23 Temperature sensor characteristics

Table 89. TS characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_L$(1) | $V_{SENSE}$ linearity with temperature | - | ±1 | ±2 | °C |
| Avg_Slope(1) | Average slope | 4.0 | 4.3 | 4.6 | mV/°C |
| $V_{25}$ | Voltage at 25 °C | 1.34 | 1.43 | 1.52 | V |
| $t_{START}$(1) | Startup time | 4 | - | 10 | µs |
| $T_{S\_temp}$(1)(2) | ADC sampling time when reading the temperature | 2.2 | - | - | µs |

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

Table 90. Temperature sensor calibration values

| Calibration value name | Description | Memory address |
|---|---|---|
| TS_CAL1 | TS ADC raw data acquired at temperature of 30 °C, $V_{DDA}$= 3.3 V | 0x1FFF F7B8 - 0x1FFF F7B9 |
| TS_CAL2 | TS ADC raw data acquired at temperature of 110 °C $V_{DDA}$= 3.3 V | 0x1FFF F7C2 - 0x1FFF F7C3 |

**Table 93. UFBGA100 package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| ddd | - | - | 0.100 | - | - | 0.0039 |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 58. Recommended footprint for the UFBGA100 package**

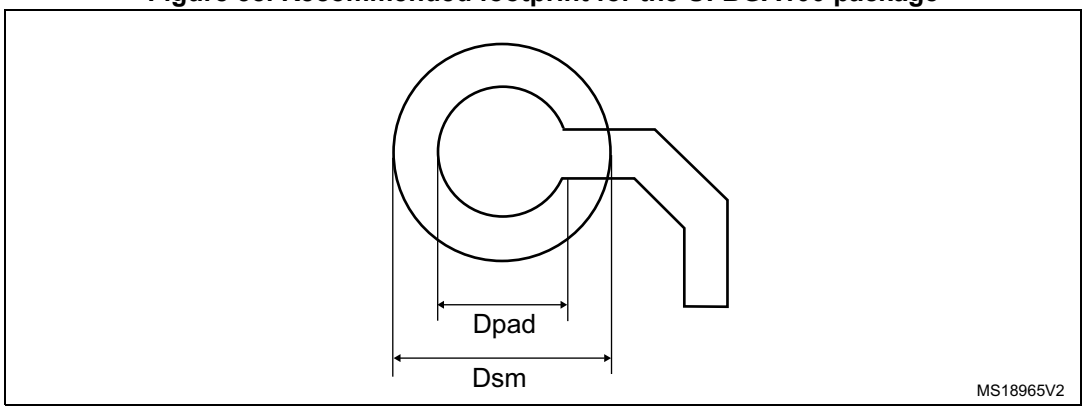



**Table 94. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.5 |
| Dpad | 0.27 mm |
| Dsm | 0.35 mm typ. (depends on the soldermask registration tolerance) |
| Solder paste | 0.27 mm aperture diameter. |

*Note: Non-solder mask defined (NSMD) pads are recommended.*

*Note: 4 to 6 mils solder paste screen printing process.*